

# DATA SHEET

For a complete data sheet, please also download:

- The IC06 74HC/HCT/HCU/HCMOS Logic Family Specifications
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Information
- The IC06 74HC/HCT/HCU/HCMOS Logic Package Outlines

## **74HC/HCT640**

### Octal bus transceiver; 3-state; inverting

Product specification  
File under Integrated Circuits, IC06

March 1988

## Octal bus transceiver; 3-state; inverting

## 74HC/HCT640

## FEATURES

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver
- $I_{CC}$  category: MSI

## GENERAL DESCRIPTION

The 74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable ( $\overline{OE}$ ) input for easy cascading and a send/receive (DIR) for direction control. OE controls the outputs so that the buses are effectively isolated. The "640" is similar to the "245" but has inverting outputs.

## QUICK REFERENCE DATA

GND = 0 V;  $T_{amb}$  = 25 °C;  $t_r = t_f = 6$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL		UNIT
			HC	HCT	
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$	$C_L = 15$ pF; $V_{CC} = 5$ V	9	9	ns
$C_I$	input capacitance		3.5	3.5	pF
$C_{I/O}$	input/output capacitance		10	10	pF
$C_{PD}$	power dissipation capacitance per transceiver	notes 1 and 2	35	35	pF

## Notes

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu$ W):  

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$$
 where:  
 $f_i$  = input frequency in MHz  
 $f_o$  = output frequency in MHz  
 $\sum (C_L \times V_{CC}^2 \times f_o)$  = sum of outputs  
 $C_L$  = output load capacitance in pF  
 $V_{CC}$  = supply voltage in V
- For HC the condition is  $V_I = GND$  to  $V_{CC}$   
For HCT the condition is  $V_I = GND$  to  $V_{CC} - 1.5$  V

## ORDERING INFORMATION

See "74HC/HCT/HCU/HCMOS Logic Package Information".

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## PIN DESCRIPTION

PIN NO.	SYMBOL	NAME AND FUNCTION
1	DIR	direction control
2, 3, 4, 5, 6, 7, 8, 9	$A_0$ to $A_7$	data inputs/outputs
10	GND	ground (0 V)
18, 17, 16, 15, 14, 13, 12, 11	$B_0$ to $B_7$	data inputs/outputs
19	$\overline{OE}$	output enable input (active LOW)
20	$V_{CC}$	positive supply voltage

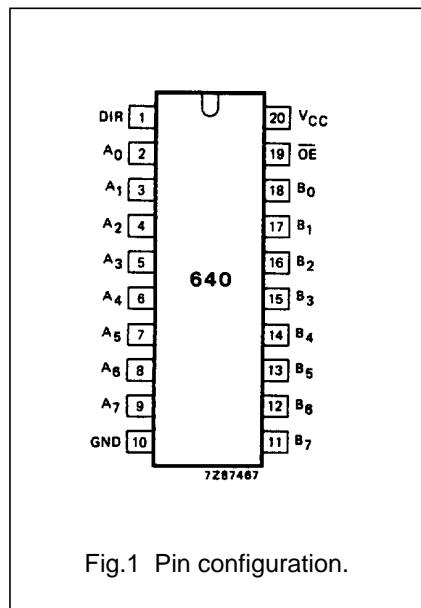


Fig.1 Pin configuration.

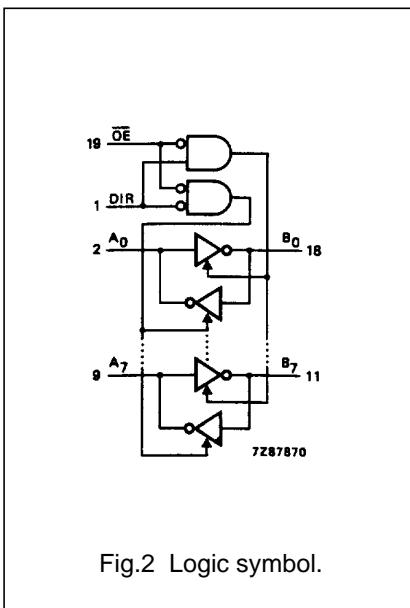


Fig.2 Logic symbol.

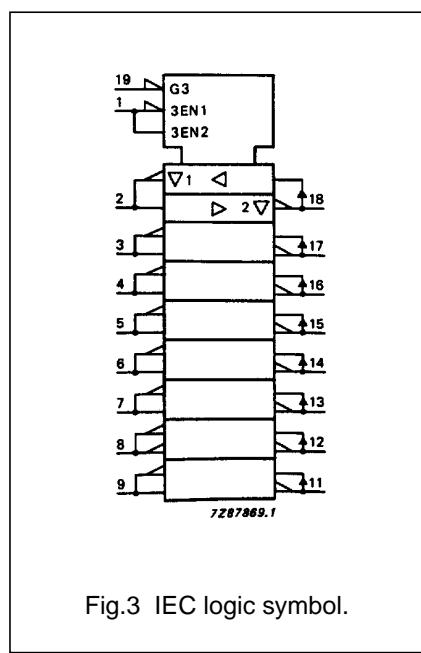


Fig.3 IEC logic symbol.

## FUNCTION TABLE

inputs		inputs/outputs	
$\overline{OE}$	DIR	$A_n$	$B_n$
L	L	$A = \overline{B}$	inputs
L	H	inputs	$B = \overline{A}$
H	X	Z	Z

## Note

1. H = HIGH voltage level
- L = LOW voltage level
- X = don't care
- Z = high impedance OFF-state

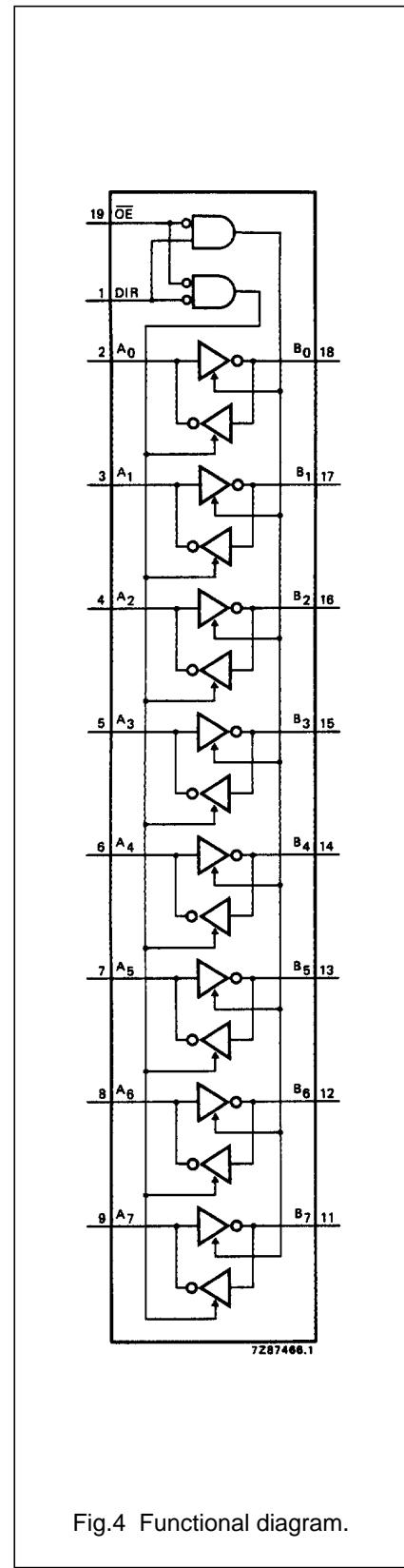


Fig.4 Functional diagram.

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## DC CHARACTERISTICS FOR 74HC

For the DC characteristics see "*74HC/HCT/HCU/HCMOS Logic Family Specifications*".

Output capability: bus driver

I<sub>CC</sub> category: MSI

## AC CHARACTERISTICS FOR 74HC

GND = 0 V; t<sub>r</sub> = t<sub>f</sub> = 6 ns; C<sub>L</sub> = 50 pF

SYMBOL	PARAMETER	T <sub>amb</sub> (°C)						UNIT	TEST CONDITIONS			
		74HC							V <sub>CC</sub> (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
t <sub>PHL</sub> / t <sub>PLH</sub>	propagation delay A <sub>n</sub> to B <sub>n</sub> ; B <sub>n</sub> to A <sub>n</sub>	30 11 9	90 18 15		115 23 20		135 27 23	ns	2.0 4.5 6.0	Fig.5		
t <sub>PZH</sub> / t <sub>PZL</sub>	3-state output enable time OE, DIR to A <sub>n</sub> ; OE, DIR to B <sub>n</sub>	44 16 13	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6		
t <sub>PHZ</sub> / t <sub>PLZ</sub>	3-state output disable time OE, DIR to A <sub>n</sub> ; OE, DIR to B <sub>n</sub>	50 18 14	150 30 26		190 38 33		225 45 38	ns	2.0 4.5 6.0	Fig.6		
t <sub>THL</sub> / t <sub>TLH</sub>	output transition time	14 5 4	60 12 10		75 15 13		90 18 15	ns	2.0 4.5 6.0	Fig.5		

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## DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see "[74HC/HCT/HCU/HCMOS Logic Family Specifications](#)".

Output capability: bus driver

 $I_{CC}$  category: MSI

## Note to HCT types

The value of additional quiescent supply current ( $\Delta I_{CC}$ ) for a unit load of 1 is given in the family specifications.To determine  $\Delta I_{CC}$  per input, multiply this value by the unit load coefficient shown in the table below.

INPUT	UNIT LOAD COEFFICIENT
$A_n$	1.50
$B_n$	1.50
$\overline{OE}$	1.50
DIR	0.90

## AC CHARACTERISTICS FOR 74HCT

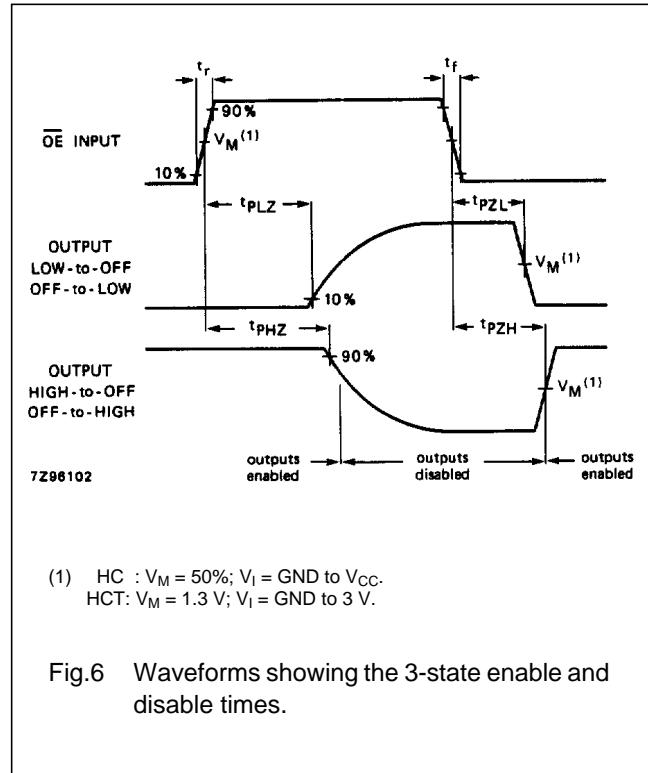
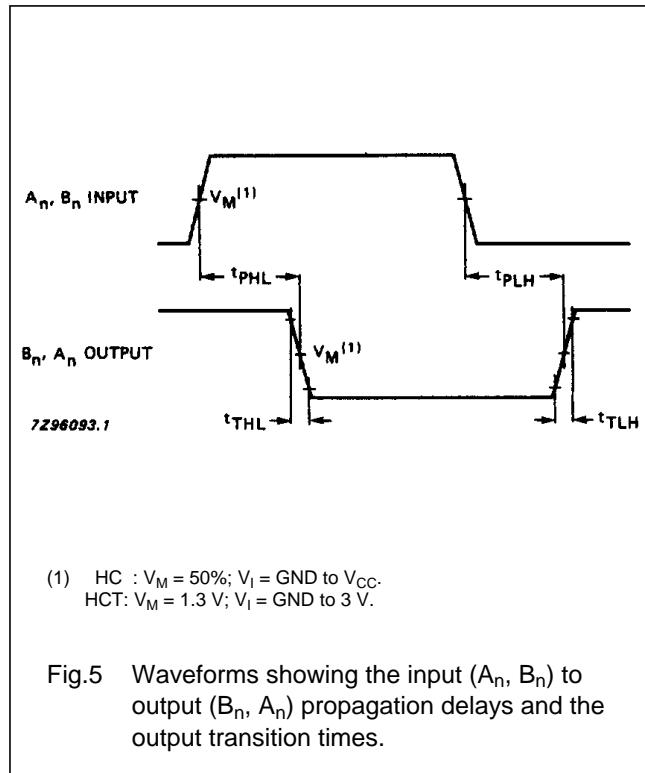
GND = 0 V;  $t_r = t_f = 6$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	$T_{amb}$ (°C)						UNIT	TEST CONDITIONS			
		74HCT							$V_{CC}$ (V)	WAVEFORMS		
		+25			−40 to +85		−40 to +125					
		min.	typ.	max.	min.	max.	min.	max.				
$t_{PHL}/t_{PLH}$	propagation delay $A_n$ to $B_n$ ; $B_n$ to $A_n$		11	22		28		33	ns	4.5	Fig.5	
$t_{PZH}/t_{PZL}$	3-state output enable time $\overline{OE}$ , DIR to $A_n$ ; $\overline{OE}$ , DIR to $B_n$		18	30		38		45	ns	4.5	Fig.6	
$t_{PHZ}/t_{PLZ}$	3-state output disable time $\overline{OE}$ , DIR to $A_n$ ; $\overline{OE}$ , DIR to $B_n$		19	30		38		45	ns	4.5	Fig.6	
$t_{THL}/t_{TLH}$	output transition time		5	12		15		18	ns	4.5	Fig.5	

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## AC WAVEFORMS



## PACKAGE OUTLINES

See ["74HC/HCT/HCU/HCMOS Logic Package Outlines"](#).

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