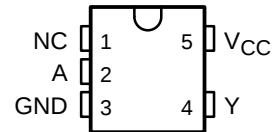


SN74LVC1G06 SINGLE INVERTER BUFFER/DRIVER WITH OPEN-DRAIN OUTPUT

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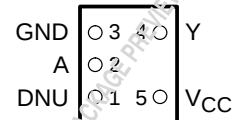
- Available in the Texas Instruments NanoStar™ and NanoFree™ Packages
- Supports 5-V V_{CC} Operation
- Input and Open-Drain Output Accept Voltages up to 5.5 V
- Max t_{pd} of 4 ns at 3.3 V
- Low Power Consumption, 10 μ A Max I_{CC}
- ± 24 -mA Output Drive at 3.3 V
- I_{off} Supports Partial-Power-Down Mode Operation
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DBV OR DCK PACKAGE
(TOP VIEW)



NC – No internal connection

YEA OR YZA PACKAGE
(BOTTOM VIEW)



DNU – Do not use

description/ordering information

This single inverter buffer/driver is designed for 1.65-V to 5.5-V V_{CC} operation.

NanoStar™ and NanoFree™ package technology is a major breakthrough in IC packaging concepts, using the die as the package.

The output of the SN74LVC1G06 device is open drain and can be connected to other open-drain outputs to implement active-low wired-OR or active-high wired-AND functions. The maximum sink current is 32 mA.

This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING‡
–40°C to 85°C	NanoStar™ WCSP (DSBGA) – YEA (Lead)	Tape and reel	SN74LVC1G06YEAR	---CT_
	NanoFree™ WCSP (DSBGA) – YZA (Lead-free)	Tape and reel	SN74LVC1G06YZAR	
	SOT (SOT-23) – DBV	Tape and reel	SN74LVC1G06DBVR	C06_
	SOT (SC-70) – DCK	Tape and reel	SN74LVC1G06DCKR	CT_

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

‡ DBV/DCK: The actual top-side marking has one additional character that designates the assembly/test site.

YEA/YZA: The actual top-side marking has three preceding characters to denote year, month, and sequence code, and one following character to designate the assembly/test site.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

NanoStar and NanoFree are trademarks of Texas Instruments.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.



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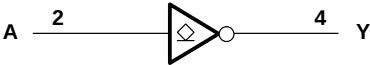
SN74LVC1G06
SINGLE INVERTER BUFFER/DRIVER
WITH OPEN-DRAIN OUTPUT

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FUNCTION TABLE

INPUT A	OUTPUT Y
H	L
L	H

logic diagram (positive logic)



absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 6.5 V
Input voltage range, V_I (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high-impedance or power-off state, V_O (see Note 1)	–0.5 V to 6.5 V
Voltage range applied to any output in the high or low state, V_O (see Notes 1 and 2)	–0.5 V to 6.5 V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through V_{CC} or GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DBV package	206°C/W
DCK package	252°C/W
YEA/YZA package	154°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input negative-voltage and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The value of V_{CC} is provided in the recommended operating conditions table.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Note 4)

		MIN	MAX	UNIT
V _{CC} Supply voltage	Operating	1.65	5.5	V
	Data retention only	1.5		
V _{IH} High-level input voltage	V _{CC} = 1.65 V to 1.95 V	0.65 × V _{CC}		V
	V _{CC} = 2.3 V to 2.7 V	1.7		
	V _{CC} = 3 V to 3.6 V	2		
	V _{CC} = 4.5 V to 5.5 V	0.7 × V _{CC}		
V _{IL} Low-level input voltage	V _{CC} = 1.65 V to 1.95 V		0.35 × V _{CC}	V
	V _{CC} = 2.3 V to 2.7 V		0.7	
	V _{CC} = 3 V to 3.6 V		0.8	
	V _{CC} = 4.5 V to 5.5 V		0.3 × V _{CC}	
V _I Input voltage		0	5.5	V
V _O Output voltage		0	5.5	V
I _{OL} Low-level output current	V _{CC} = 1.65 V		4	mA
	V _{CC} = 2.3 V		8	
	V _{CC} = 3 V		16	
			24	
	V _{CC} = 4.5 V		32	
Δt/Δv Input transition rise or fall rate	V _{CC} = 1.8 V ± 0.15 V, 2.5 V ± 0.2 V		20	ns/V
	V _{CC} = 3.3 V ± 0.3 V		10	
	V _{CC} = 5 V ± 0.5 V		5	
T _A Operating free-air temperature		–40	85	°C

NOTE 4: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V _{CC}	MIN	TYP [†]	MAX	UNIT
V _{OL}		I _{OL} = 100 μA	1.65 V to 5.5 V			0.1	V
		I _{OL} = 4 mA	1.65 V			0.45	
		I _{OL} = 8 mA	2.3 V			0.3	
		I _{OL} = 16 mA	3 V			0.4	
		I _{OL} = 24 mA				0.55	
		I _{OL} = 32 mA	4.5 V			0.55	
I _I	A input	V _I = 5.5 V or GND	0 to 5.5 V			±5	μA
I _{off}		V _I or V _O = 5.5 V	0			±10	μA
I _{CC}		V _I = 5.5 V or GND, I _O = 0	1.65 V to 5.5 V			10	μA
ΔI _{CC}		One input at V _{CC} – 0.6 V, Other inputs at V _{CC} or GND	3 V to 5.5 V			500	μA
C _i		V _I = V _{CC} or GND	3.3 V			4	pF
C _o		V _O = V _{CC} or GND	3.3 V			5	pF

[†] All typical values are at V_{CC} = 3.3 V, T_A = 25°C.



SN74LVC1G06

SINGLE INVERTER BUFFER/DRIVER

WITH OPEN-DRAIN OUTPUT

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switching characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CC} = 1.8 V ± 0.15 V		V _{CC} = 2.5 V ± 0.2 V		V _{CC} = 3.3 V ± 0.3 V		V _{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t _{pd}	A	Y	2.2	5.6	1.1	4	1.2	4	1	3	ns

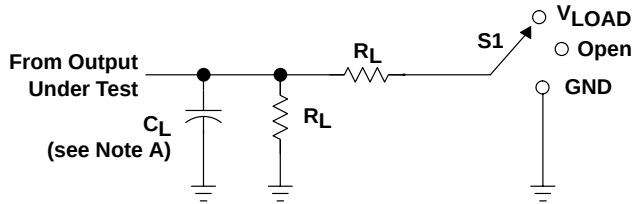
operating characteristics, T_A = 25°C

PARAMETER	TEST CONDITIONS	V _{CC} = 1.8 V	V _{CC} = 2.5 V	V _{CC} = 3.3 V	V _{CC} = 5 V	UNIT
		TYP	TYP	TYP	TYP	
C _{pd} Power dissipation capacitance	f = 10 MHz	3	3	4	6	pF



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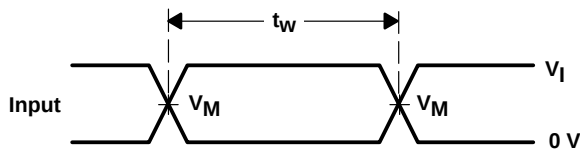
PARAMETER MEASUREMENT INFORMATION (OPEN DRAIN)



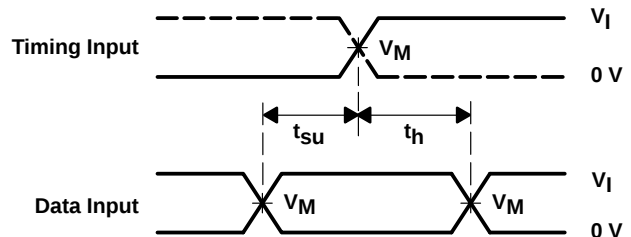
LOAD CIRCUIT

TEST	S1
t_{pZL} (see Notes E and F)	V_{LOAD}
t_{pLZ} (see Notes E and G)	V_{LOAD}
t_{PHZ}/t_{PZH}	V_{LOAD}

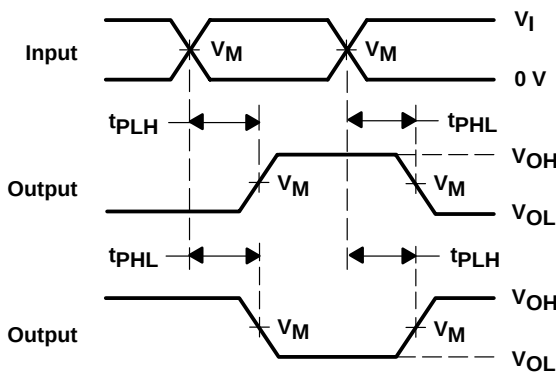
V_{CC}	INPUT		V_M	V_{LOAD}	C_L	R_L	V_{Δ}
	V_I	t_r/t_f					
$1.8\text{ V} \pm 0.15\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	1 k Ω	0.15 V
$2.5\text{ V} \pm 0.2\text{ V}$	V_{CC}	$\leq 2\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	30 pF	500 Ω	0.15 V
$3.3\text{ V} \pm 0.3\text{ V}$	3 V	$\leq 2.5\text{ ns}$	1.5 V	6 V	50 pF	500 Ω	0.3 V
$5\text{ V} \pm 0.5\text{ V}$	V_{CC}	$\leq 2.5\text{ ns}$	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



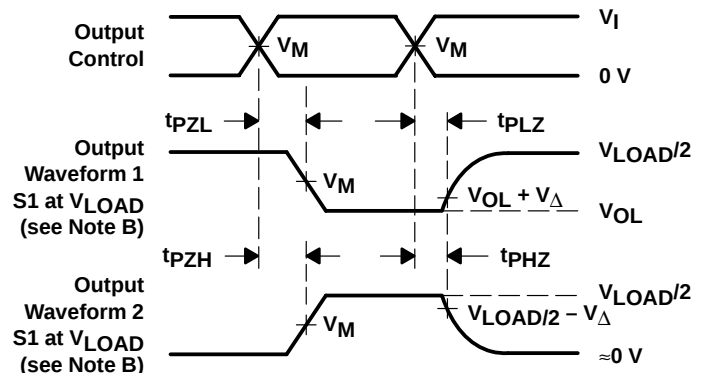
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
 - C. All input pulses are supplied by generators having the following characteristics: PRR $\leq 10\text{ MHz}$, $Z_O = 50\text{ }\Omega$.
 - D. The outputs are measured one at a time with one transition per measurement.
 - E. Since this device has open-drain outputs, t_{pLZ} and t_{pZL} are the same as t_{pd} .
 - F. t_{pZL} is measured at V_M .
 - G. t_{pLZ} is measured at $V_{OL} + V_{\Delta}$.
 - H. All parameters and waveforms are not applicable to all devices.

Figure 1. Load Circuit and Voltage Waveforms

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