# Field Programmable Blank Oscillator

**Series CPP**

- ***Programmed with the PG-3000, PG-3100 field oscillator programming instrument within seconds***
- ***Can be programmed twice***
- ***Standard Package Options***
- ***Also available in 2.7 V***

RoHS COMPLIANT 2002 / 95 / EC

## Part Numbering Example: CPP C 1 L Z - A5 B6 - XX.XXXX TS

| CPP | C | 1 | L | Z | A5 | B6 | XX.XXXX | TS |
|---|---|---|---|---|---|---|---|---|
| SERIES | OUTPUT | PACKAGE STYLE | VOLTAGE | ADDED FEATURES | OPERATING TEMP. | STABILITY | FREQUENCY | TRI-STATE |
| CPP | C = CMOS<br>T = TTL | 1 = Full Size<br>4 = Half Size<br>5 = 3.2X5 Ceramic<br>7 = 5X7 Ceramic<br>8 = PLASTIC SMD<br>8B = PLASTIC SMD | Blank = 5V<br>L = 3.3 V<br>R = 2.7 | Blank = Bulk<br>T = Tube<br>Z = Tape and Reel | Blank = 0°C +70°C<br>A3 = -55°C+155°C<br>A5 = -20°C +70°C<br>A7 = -40°C +85°C | B6 = ±100 ppm<br>BP = ±50 ppm<br>BR = ±25 ppm | 0.500 ~133.000 MHz | TS = Tri-State<br>PD=PowerDwn |

## Specifications:

| Description | Min | Typ | Max | Unit |
|---|---|---|---|---|
| **Frequency Range:** Programmable to Any Discrete Frequency | 0.5 | | 133.000 | MHz |
| **Available Stability Options:** | -100<br>-50<br>-25 | | 100<br>50<br>25 | ppm<br>ppm<br>ppm |
| **Programmable Supply Voltage:** | | | | |
| (1–133 MHz) | 4.5 | 5.0 | 5.5 | V |
| (1–100 MHz) | 3.0 | 3.3 | 3.6 | V |
| **Operating Temperature Range Options:** | 0<br>-20<br>-40 | | +70<br>+70<br>+85 | °C<br>°C<br>°C |
| **Storage Temperature:** | -55 | | +125 | °C |
| Aging (PPM/Year) Ta=25C, Vdd=5/3.3V | | | ±5 | |
| **Programmable Output Level:** | TTL/CMOS | | | |
| **Packaging:** | Tape and Reel (1K per Reel)<br>Tube | | | |

## Operating Conditions:

| | Description | Min | Max | Unit |
|---|---|---|---|---|
| Vdd | Supply Voltage | 3.0 | 5.5 | V |
| $C_{TTL}$ | Max Capacitive Load on outputs for TTL levels | | | |
| | 4.5V–5.5V Vdd ≤ 40 MHz | | 50 | pF |
| | 4.5V–5.5V Vdd > 40–133 MHz | | 25 | pF |
| $C_{CMOS}$ | Max Capacitive Load on outputs for CMOS levels | | | |
| | 4.5V–5.5V Vdd, ≤ 66 MHz | | 50 | pF |
| | 4.5V–5.5V Vdd, >66–133 MHz | | 25 | pF |
| | 3.0V–3.6V Vdd, ≤ 40 MHz | | 30 | pF |
| | 3.0V–3.6V Vdd, >40–100 MHz | | 15 | pF |

Cardinal Components, Inc.
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Rev: C-090414-11



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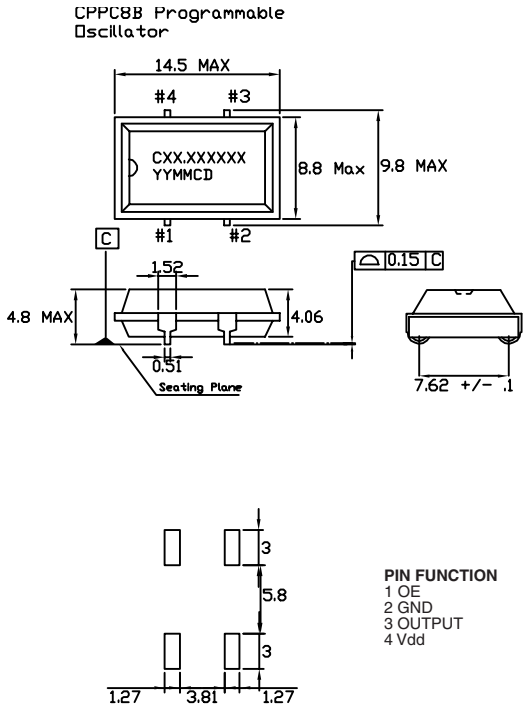
# Field Programmable Blank Oscillator

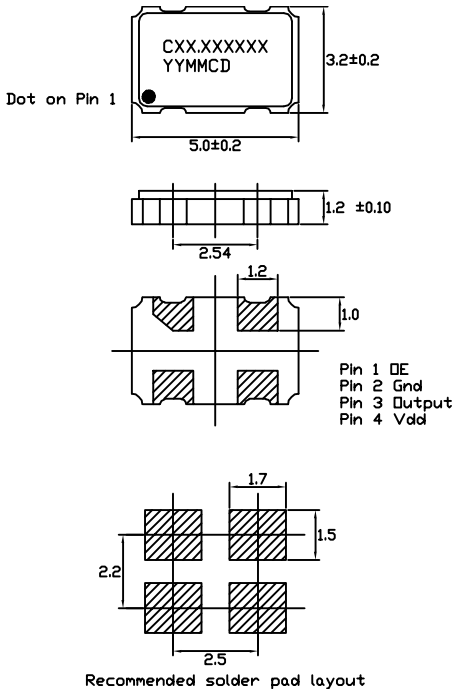
***Note:*** ***Bypass*** Vdd ***to GND with a 0.01 µF capacitor***

## Style 8B Plastic SMD




**PIN FUNCTION**
1 OE
2 GND
3 OUTPUT
4 Vdd

## Style 5 3.2x5 Ceramic SMD




Recommended solder pad layout

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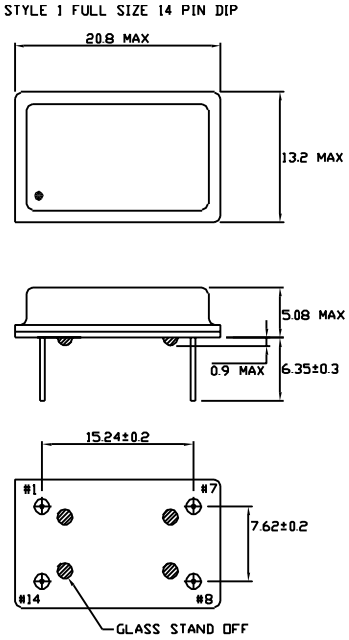
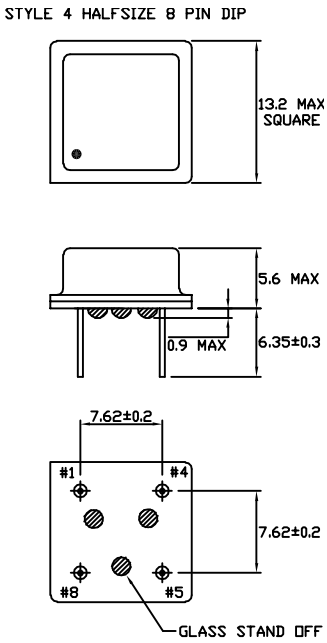
***Note:*** ***Bypass*** Vdd ***to GND with a 0.01 µF capacitor***

## Style 1 Full Size 14 Pin Dip



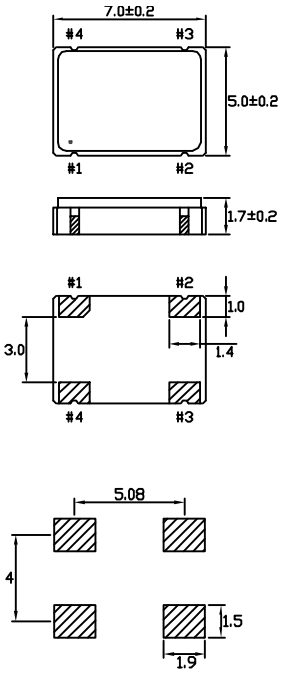

**PIN FUNCTION**
1 CONTROL
7 GND
8 OUTPUT
14 Vdd

## Style 4 Half Size 8 Pin Dip



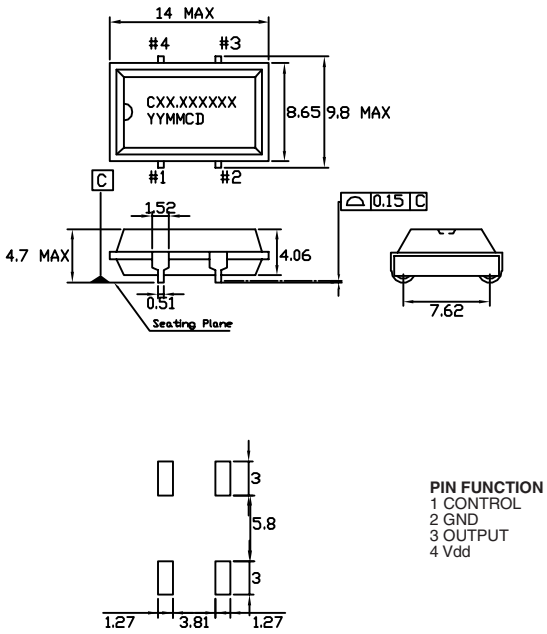

**PIN FUNCTION**
1 CONTROL
4 GND
5 OUTPUT
8 Vdd

## Style 7 5x7 Ceramic SMD




**PIN FUNCTION**
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

## Style 8 Plastic SMD







**PIN FUNCTION**
1 CONTROL
2 GND
3 OUTPUT
4 Vdd

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## Output Clock Switching Characteristics

| Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Duty Cycle:** | | | | | |
| TTL @ 1.4 V | ≤ 50 MHz, $C_L$ = 50 pF | 45 | | 55 | % |
| 4.5-5.5 Vdd | 50–66 MHz, $C_L$ = 15 pF | 45 | | 55 | % |
| | 66–125 MHz, $C_L$ = 25 pF | 40 | | 60 | % |
| | 125–133 MHz, $C_L$ = 15 pF | 40 | | 60 | % |
| **Duty Cycle:** | ≤ 66 MHz, $C_L$ ≤ 25 pF | 45 | | 55 | % |
| CMOS @ Vdd/2 | 66–125 MHz, $C_L$ ≤ 25 pF | 40 | | 60 | % |
| 4.5-5.5 Vdd | 125–133 MHz, $C_L$ ≤ 15 pF | 40 | | 60 | % |
| 3.0–3.6 Vdd | ≤ 40 MHz, $C_L$ ≤ 30 pF | 45 | | 55 | % |
| | 40-100 MHz, $C_L$ ≤ 15 pF | 40 | | 60 | % |
| **Output Clock Rise/Fall** | | | | | |
| | 0.8V–2.0V, 4.5-5.5 Vdd, $C_L$ = 50 | | | 1.8 | ns |
| | 0.8V–2.0V, 4.5-5.5 Vdd, $C_L$ = 25 | | | 1.2 | ns |
| | 0.8V–2.0V, 4.5-5.5 Vdd, $C_L$ = 15 | | | 0.9 | ns |
| | 0.2–0.8Vdd, 4.5-5.5 Vdd, $C_L$ = 50 | | | 3.4 | ns |
| | 0.2–0.8Vdd, 3.0–3.6 Vdd, $C_L$ = 30 | | | 4.0 | ns |
| | 0.2–0.8Vdd, 3.0–3.6 Vdd, $C_L$ = 15 | | | 2.4 | ns |
| **Start Up Time** | From power on | | | 2 | ms |
| **Power Down Delay Time** | | | | | |
| Synchronous | PWR_DWN pin LOW to output Hi-Z | | T/2 | T+10 | ns |
| Asynchronous | | | 10 | 15 | ns |
| **Output Disable Time** | | | | | |
| Synchronous | OE pin LOW to output Hi-Z | | T/2 | T+10 | ns |
| Asynchronous | T = Frequency oscillator period | | 10 | 15 | ns |
| **Output Enable Time** | | | | 100 | ns |
| | ≤ 33.000 MHz | | 40 | 50 | ps |
| **RMS Period Jitter:** | > 33.000, MHz | | 30 | 40 | ps |
| Peak to Peak * | ≤ 33.000 MHz | | 100 | 250 | ps |
| | > 33.000 MHz | | 75 | 175 | ps |

* Jitter tested at > 1,000,000 samples, exceeding JEDEC std JESD65.

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## Electrical Characteristics

| Description | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|
| **Input Characteristics (Pin 1):** | | | | | |
| $V_{IL}$, Low–Level Input Voltage | 4.5–5.5V Vdd | | | 0.8 | V |
| TO DISABLE OUTPUT | 3.0–3.6V Vdd | | | 0.2Vdd | V |
| $V_{IH}$, High–Level Input Voltage | 4.5–5.5V Vdd | 2.0 | | | V |
| TO ENABLE OUTPUT OPEN | 3.0–3.6V Vdd | 0.7VddV | | | |
| $I_{IL}$, Input Low Current | $V_{IN}$ = 0V | | | 10 | µA |
| $I_{IH}$, Input High Current | $V_{IN}$ =Vdd | | | 5 | µA |
| **Output Characteristics:** | | | | | |
| $V_{OL}$, Low–Level Output Voltage | 4.5V–5.5V Vdd, 16 mA $I_{OL}$ | | | 0.4 | V |
| | 3.0V–3.6V Vdd, 8 mA $I_{OL}$ | | | 0.4 | V |
| $V_{OHTTL}$, High-level Output Voltage TTL | 4.5V–5.5V Vdd, -16 mA $I_{OL}$ | 2.4 | | | V |
| $V_{OHCMOS}$, | 4.5V–5.5V Vdd, -16 mA $I_{OL}$ | Vdd-0.4 | | | V |
| High-level CMOS Voltage | 3.0V–3.6V Vdd, -8 mA $I_{OL}$ | Vdd-0.4 | | | V |
| **Power Supply Current:** | 4.5–5.5 Vdd, Output Freq ≤ 133 MHz | | | 45 | mA |
| **(unloaded)** | 3.0–3.6 Vdd, Output Freq ≤ 100 MHz | | | 25 | mA |
| **Standby Current:** | | | 10 | 50 | µA |
| **Pull-Up (Pin 1)** | 4.5–5.5 Vdd, $V_{IN}$ = 0V | 1.1 | 3.0 | 8.0 | MΩ |
| | 4.5–5.5 Vdd, $V_{IN}$ = 0.7V | 50 | 100 | 200 | KΩ |
| **Tri-State Leakage Current** | 5.0 Vdd | | 20 | | µA |
| **Output Enable Mode:** | Output is Tri-Stated | | | | |
| **Power Down Mode:** | Output is Tri-Stated. | | | | |