

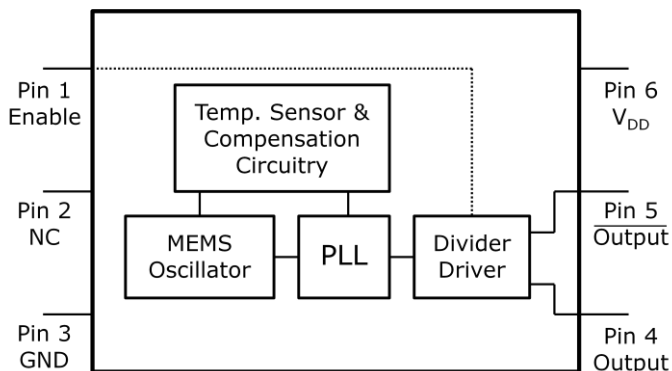


## General Description

The DSC1104 & DSC1124 series of high performance oscillators utilizes a proven silicon MEMS technology to provide excellent jitter and stability over a wide range of supply voltages and temperatures. By eliminating the need for quartz or SAW technology, MEMS oscillators significantly enhance reliability and accelerate product development, while meeting stringent clock performance criteria for a variety of communications, storage, and networking applications.

DSC1104 has a standby feature allowing it to completely power-down when EN pin is pulled low; whereas for DSC1124, only the outputs are disabled when EN is low. Both oscillators are available in industry standard packages, including the small 3.2x2.5 mm<sup>2</sup>, and are “drop-in” replacements for standard 6-pin HCSL quartz crystal oscillators.

## Block Diagram



## Output Enable Modes

EN Pin	DSC1104	DSC1124
High	Outputs Active	Outputs Active
NC	Outputs Active	Outputs Active
Low	Standby	Outputs Disabled

## Features

- **Low RMS Phase Jitter: <1 ps (typ)**
- **High Stability: ±10, ±25, ±50 ppm**
- **Wide Temperature Range**
  - Industrial: -40° to 85° C
  - Ext. commercial: -20° to 70° C
- **High Supply Noise Rejection: -50 dBc**
- **Short Lead Time: 2 Weeks**
- **Wide Freq. Range: 2.3 to 460 MHz**
- **Small Industry Standard Footprints**
  - 2.5x2.0, 3.2x2.5, 5.0x3.2, & 7.0x5.0 mm
- **Excellent Shock & Vibration Immunity**
  - Qualified to MIL-STD-883
- **High Reliability**
  - 20x better MTF than quartz oscillators
- **Low Current Consumption**
- **Supply Range of 2.25 to 3.6 V**
- **Standby & Output Enable Function**
- **Lead Free & RoHS Compliant**
- **LVPECL & LVDS Versions Available**

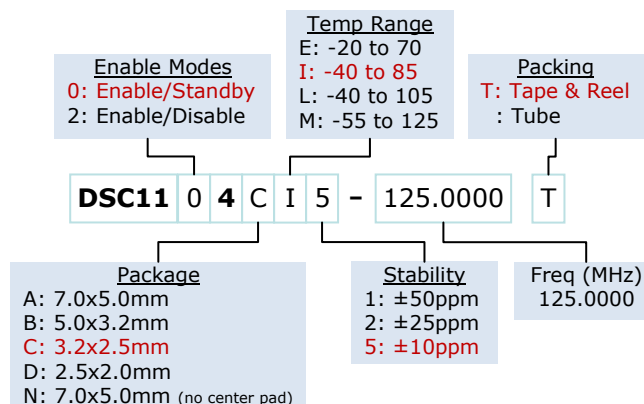
## Applications

- **Storage Area Networks**
  - SATA, SAS, Fibre Channel
- **Passive Optical Networks**
  - EPON, 10G-EPON, GPON, 10G-PON
- **Ethernet**
  - 1G, 10GBASE-T/KR/LR/SR, and FCoE
- **HD/SD/SDI Video & Surveillance**
- **PCI Express: Gen 1 & Gen 2**
- **DisplayPort**

## Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	$V_{DD}+0.3$	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

## Ordering Code



Note: 1000+ years of data retention on internal memory

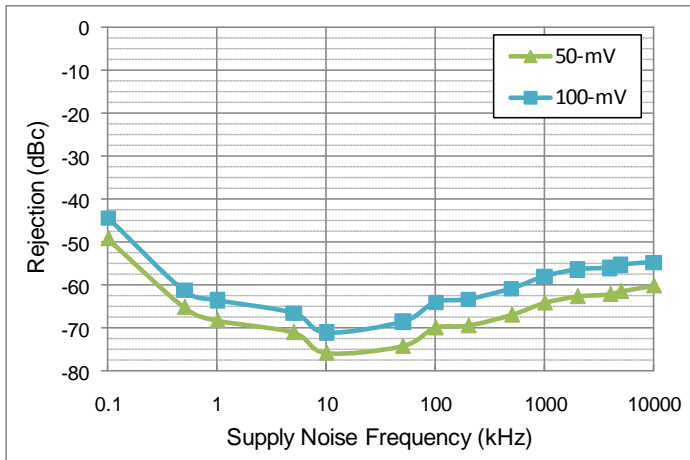
## Specifications

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage <sup>1</sup>	$V_{DD}$		2.25		3.6	V
Supply Current	$I_{DD}$	EN pin low – outputs are disabled DSC1104 DSC1124		20	0.095 22	mA
Frequency Stability	$\Delta f$	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	$\Delta f$	1 year @25°C			±5	ppm
Startup Time <sup>2</sup>	$t_{SU}$	T=25°C			5	ms
Input Logic Levels						
Input logic high	$V_{IH}$		0.75x $V_{DD}$		-	V
Input logic low	$V_{IL}$		-		0.25x $V_{DD}$	
Output Disable Time <sup>3</sup>	$t_{DA}$				5	ns
Output Enable Time	$t_{EN}$	DSC1104 DSC1124			5 20	ms ns
Enable Pull-Up Resistor <sup>4</sup>		Pull-up resistor exist		40		kΩ
<b>HCSL Outputs</b>						
Supply Current	$I_{DD}$	Output Enabled, $R_L=50\Omega$		40	42	mA
Output Logic Levels						
Output logic high	$V_{OH}$	$R_L=50\Omega$	0.725		-	V
Output logic low	$V_{OL}$		-		0.1	
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time <sup>3</sup>						
Rise Time	$t_R$	20% to 80% $R_L=50\Omega$ , $C_L=2pF$	200		400	ps
Fall Time	$t_F$					
Frequency	$f_0$	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter	$J_{PER}$			2.5		ps <sub>RMS</sub>
Integrated Phase Noise	$J_{PH}$	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.37 1.7	2	ps <sub>RMS</sub>

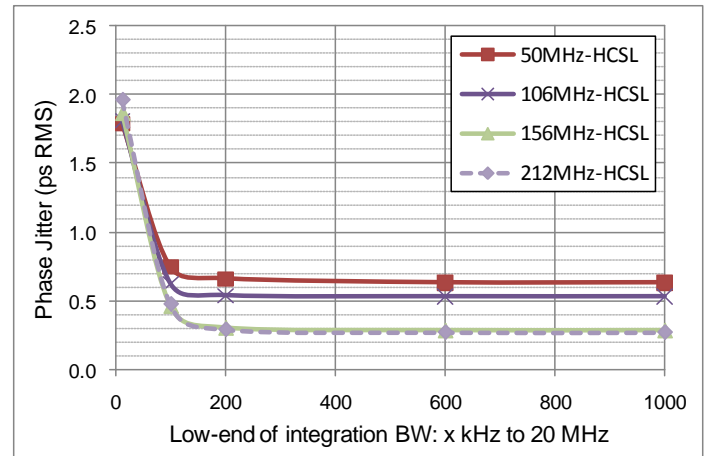
### Notes:

- Pin 6  $V_{DD}$  should be filtered with 0.1uF capacitor.
- $t_{su}$  is time to 100ppm of output frequency after  $V_{DD}$  is applied and outputs are enabled.
- Output Waveform and Test Circuit figures below define the parameters.
- Output is enabled if pad is floated or not connected.

**Nominal Performance Parameters** (Unless specified otherwise:  $T=25^{\circ}C$ ,  $V_{DD}=3.3V$ )

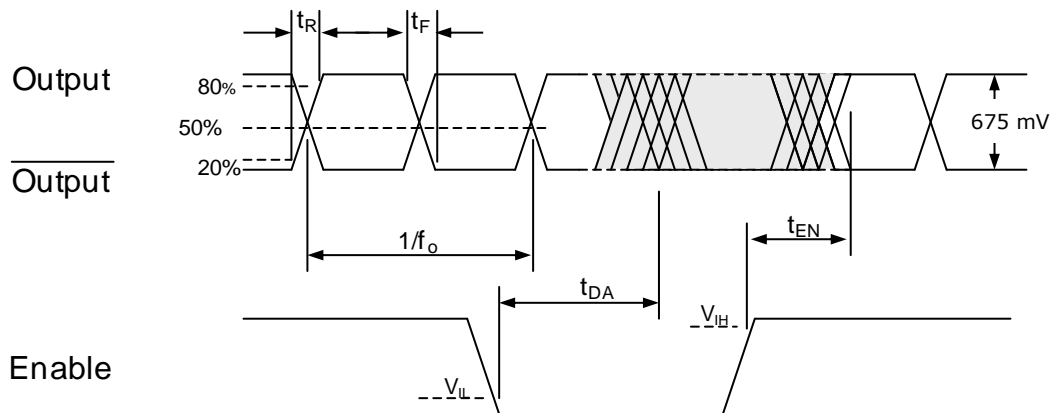


Power supply rejection ratio

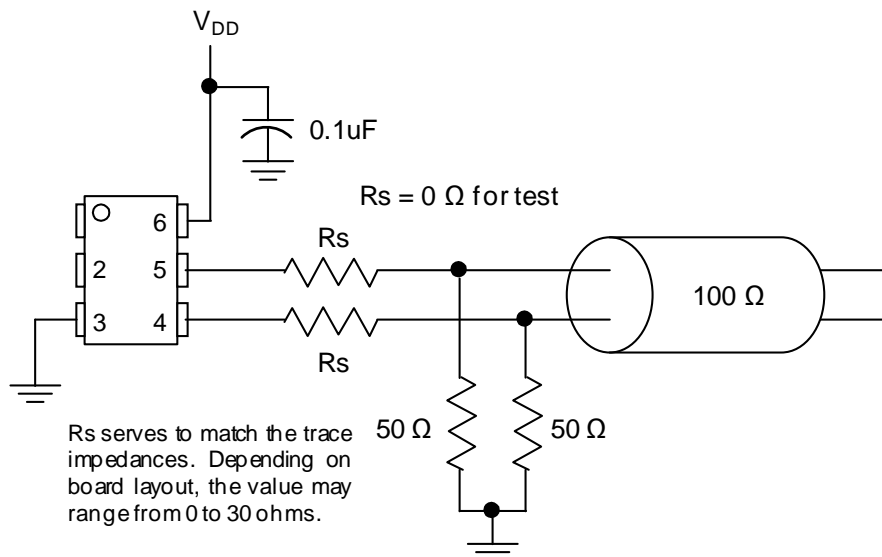


Phase jitter (integrated phase noise)

**Output Waveform**

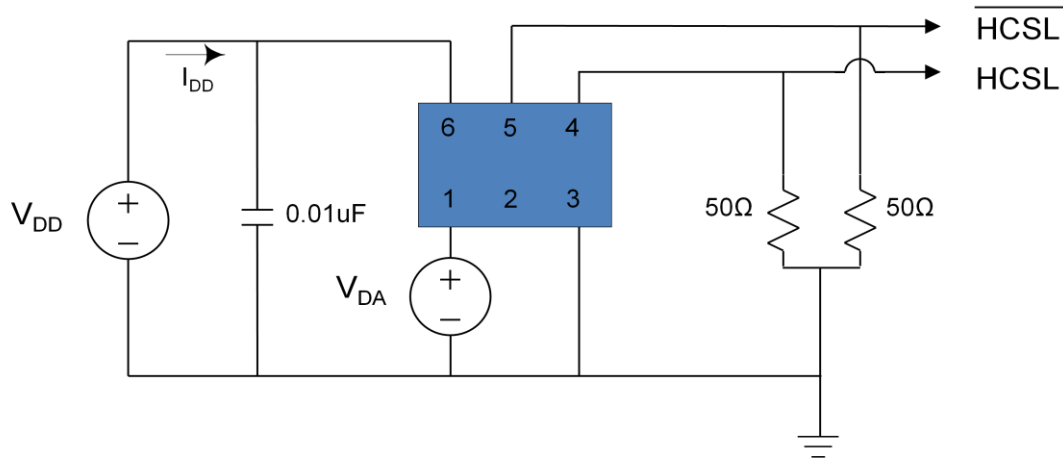


**Typical Termination Scheme**

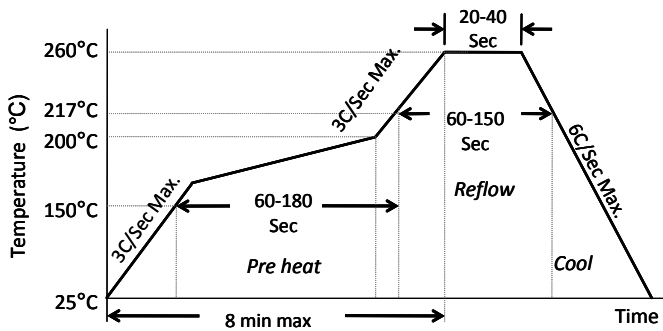


$R_s$  serves to match the trace impedances. Depending on board layout, the value may range from 0 to 30 ohms.

## Test Circuit



## Solder Reflow Profile



### MSL 1 @ 260°C refer to JSTD-020C

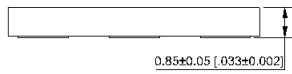
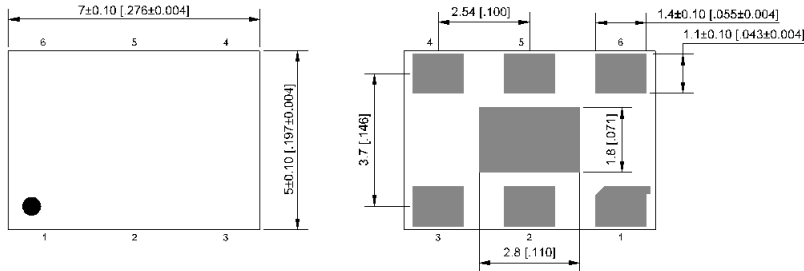
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

## Package Dimensions

### 7.0 x 5.0 mm Plastic Package

External Dimensions

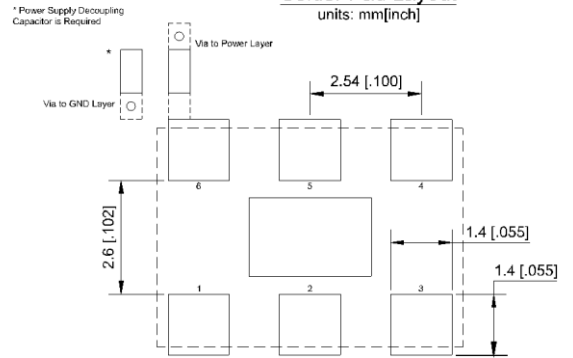
units: mm[inch]



No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	Output
6	VDD

Recommended Solder Pad Layout

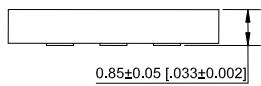
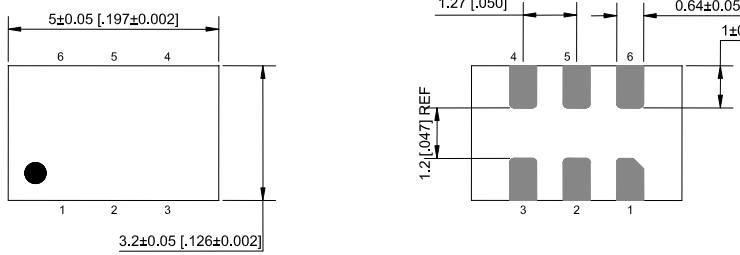
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### 5.0 x 3.2 mm Plastic Package

External Dimensions

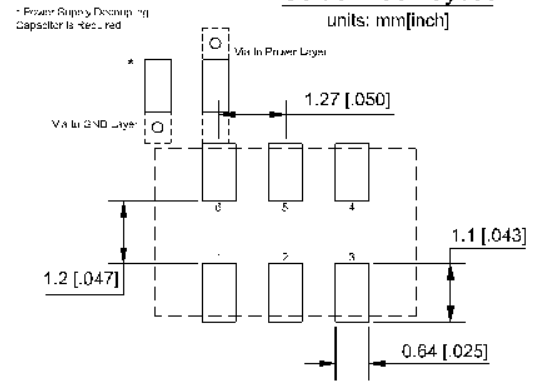
units: mm[inch]



No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	Output
6	VDD

Recommended Solder Pad Layout

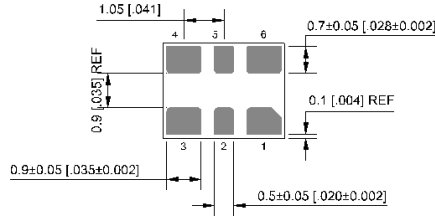
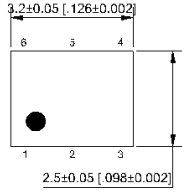
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### 3.2 x 2.5 mm Plastic Package

External Dimensions

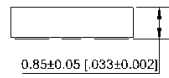
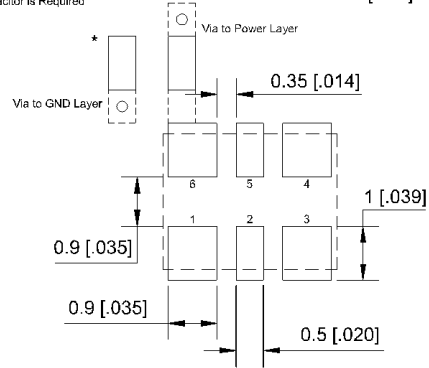
units: mm[inch]



\* Power Supply Decoupling Capacitor is Required

Recommended Solder Pad Layout

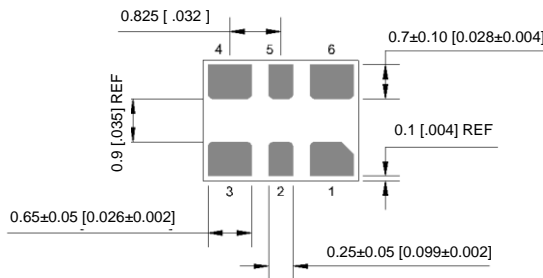
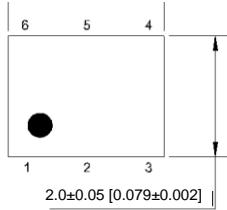
units: mm[inch]



No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	Output
6	VDD

### 2.5 x 2.0 mm Plastic Package

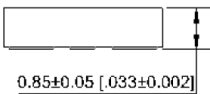
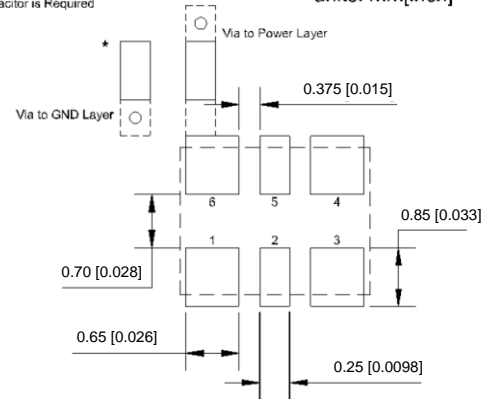
2.5±0.05 [0.098±0.002]



\* Power Supply Decoupling Capacitor is Required

Recommended Solder Pad Layout

units: mm[inch]

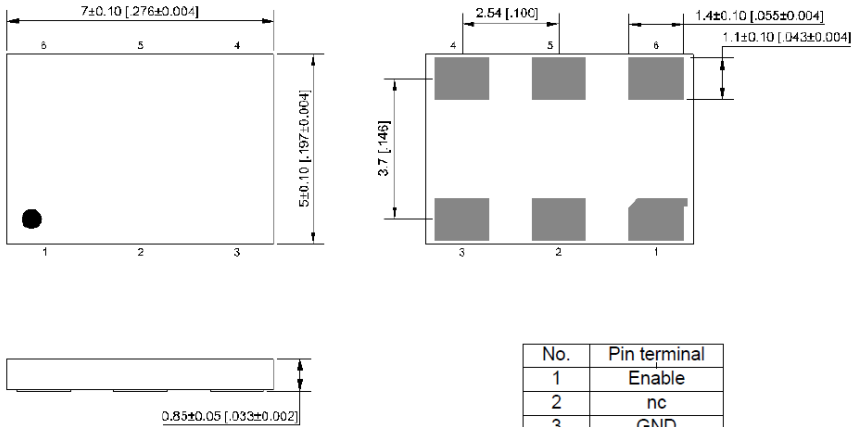


No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	Output
6	VDD

## 7.0 x 5.0 mm Plastic Package

### External Dimensions

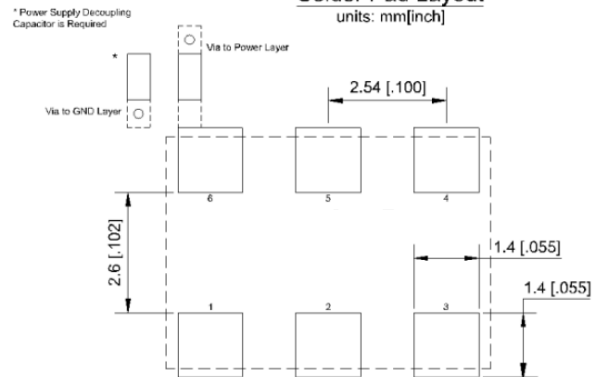
units: mm[inch]



No.	Pin terminal
1	Enable
2	nc
3	GND
4	Output
5	Output
6	VDD

### Recommended Solder Pad Layout

units: mm[inch]



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