

FEATURES

- Lowest auto-zero amplifier noise
- Low offset voltage: 1 μV typical
- Input offset drift: 0.002 $\mu\text{V}/^\circ\text{C}$ typical
- Rail-to-rail input and output swing
- 5 V single-supply operation
- High gain, CMRR, and PSRR: 130 dB
- Very low input bias current: 100 pA maximum
- Low supply current: 1.0 mA
- Overload recovery time: 50 μs
- No external components required

ENHANCED PRODUCT FEATURES

- Supports defense and aerospace applications (AQEC standard)
- Extended temperature range: -55°C to $+125^\circ\text{C}$
- Controlled manufacturing baseline
- One assembly/test site
- One fabrication site
- Enhanced product change notification
- Qualification data available on request

APPLICATIONS

- Pressure and position sensors
- Strain gage amplifiers
- Medical instrumentation
- Thermocouple amplifiers
- Precision current sensing
- Photodiode amplifiers

PIN CONFIGURATION

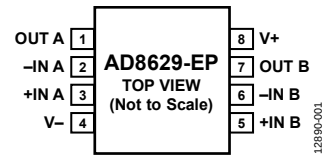


Figure 1. 8-Lead SOIC_N (R-8)

GENERAL DESCRIPTION

The **AD8629-EP** amplifier has ultralow offset, drift, and bias current. The device is a wide bandwidth auto-zero amplifier featuring rail-to-rail input and output swing and low noise. Operation is fully specified from 2.7 V to 5 V single supply (± 1.35 V to ± 2.5 V dual supply).

The **AD8629-EP** provides benefits previously found only in expensive auto-zeroing or chopper-stabilized amplifiers. Using Analog Devices, Inc., topology, this zero-drift amplifier combines low cost with high accuracy and low noise. No external capacitor is required. In addition, the **AD8629-EP** greatly reduces the digital switching noise found in most chopper-stabilized amplifiers.

With an offset voltage of only 1 μV , drift of less than 0.05 $\mu\text{V}/^\circ\text{C}$, and noise of only 0.5 μV p-p (0 Hz to 10 Hz), the **AD8629-EP** is suited for applications where error sources cannot be tolerated. Position and pressure sensors, medical equipment, and strain gage amplifiers benefit greatly from nearly zero drift over the operating temperature range. Many systems can take advantage of the rail-to-rail input and output swings provided by the **AD8629-EP** to reduce input biasing complexity and maximize SNR.

The **AD8629-EP** is specified for the extended industrial temperature range (-55°C to $+125^\circ\text{C}$). The **AD8629-EP** is available in a standard 8-lead narrow SOIC plastic package.

TABLE OF CONTENTS

Features	1	Electrical Characteristics— $V_S = 2.7\text{ V}$	4
Enhanced Product Features	1	Absolute Maximum Ratings	5
Applications	1	Thermal Characteristics	5
Pin Configuration	1	ESD Caution	5
General Description	1	Typical Performance Characteristics	6
Revision History	2	Outline Dimensions	8
Specifications	3	Ordering Guide	8
Electrical Characteristics— $V_S = 5.0\text{ V}$	3		

REVISION HISTORY

8/15—Rev. 0 to Rev. A	
Changes to Ordering Guide	8

6/15—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS— $V_S = 5.0\text{ V}$

$V_S = 5.0\text{ V}$, $V_{CM} = 2.5\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	5	μV
Input Bias Current	I_B	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		30	15	μV
Input Offset Current	I_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			100	pA
Input Voltage Range		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			1.5	nA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 5\text{ V}$		50	200	pA
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.3\text{ V to } 4.7\text{ V}$			250	pA
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$			5	V
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to ground	4.99	4.996		V
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.99	4.995		V
		$R_L = 10\text{ k}\Omega$ to ground	4.95	4.98		V
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	4.95	4.97		V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to V_+		1	5	mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2	5	mV
		$R_L = 10\text{ k}\Omega$ to V_+		10	20	mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		15	20	mV
Short-Circuit Limit	I_{SC}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	± 25	± 50		mA
Output Current	I_O	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 40		mA
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 30		mA
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 15		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	115	130		dB
Supply Current per Amplifier	I_{SY}	$V_O = V_S/2$		0.85	1.1	mA
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.0	1.2	mA
INPUT CAPACITANCE						
Differential	C_{IN}			1.5		pF
Common Mode				8.0		pF
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		1.0		$\text{V}/\mu\text{s}$
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			2.5		MHz
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	0.1 Hz to 10 Hz		0.5		$\mu\text{V p-p}$
		0.1 Hz to 1.0 Hz		0.16		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		22		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 10\text{ Hz}$		5		$\text{fA}/\sqrt{\text{Hz}}$

ELECTRICAL CHARACTERISTICS— $V_S = 2.7\text{ V}$

$V_S = 2.7\text{ V}$, $V_{CM} = 1.35\text{ V}$, $V_O = 1.4\text{ V}$, $T_A = 25^\circ\text{C}$, unless otherwise noted.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	5	μV
Input Bias Current	I_B	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		30	100	μV pA
Input Offset Current	I_{OS}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1.0	1.5	nA
Input Voltage Range		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		50	200	pA
Common-Mode Rejection Ratio	CMRR	$V_{CM} = 0\text{ V to } 2.7\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	0		250	pA V
Large Signal Voltage Gain	A_{VO}	$R_L = 10\text{ k}\Omega$, $V_O = 0.3\text{ V to } 2.4\text{ V}$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	115	130		dB
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	110	120		dB
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	$R_L = 100\text{ k}\Omega$ to ground $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.68	2.695		V
		$R_L = 10\text{ k}\Omega$ to ground $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.68	2.695		V
Output Voltage Low	V_{OL}	$R_L = 100\text{ k}\Omega$ to V_+ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.67	2.68		V
		$R_L = 10\text{ k}\Omega$ to V_+ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	2.67	2.675		V
Short-Circuit Limit	I_{SC}	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		1	5	mV
Output Current	I_O	$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		2	5	mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		10	20	mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		15	20	mV
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	± 10	± 15		mA
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 10		mA
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 10		mA
		$-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		± 5		mA
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	$V_S = 2.7\text{ V to } 5.5\text{ V}$, $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$	115	130		dB
Supply Current per Amplifier	I_{SY}	$V_O = V_S/2$ $-55^\circ\text{C} \leq T_A \leq +125^\circ\text{C}$		0.75	1.0	mA
				0.9	1.2	mA
INPUT CAPACITANCE						
Differential	C_{IN}			1.5		pF
Common Mode				8.0		pF
DYNAMIC PERFORMANCE						
Slew Rate	SR	$R_L = 10\text{ k}\Omega$		1		$\text{V}/\mu\text{s}$
Overload Recovery Time				0.05		ms
Gain Bandwidth Product	GBP			2		MHz
NOISE PERFORMANCE						
Voltage Noise	$e_n\text{ p-p}$	0.1 Hz to 10 Hz		0.5		$\mu\text{V p-p}$
Voltage Noise Density	e_n	$f = 1\text{ kHz}$		22		$\text{nV}/\sqrt{\text{Hz}}$
Current Noise Density	i_n	$f = 10\text{ Hz}$		5		$\text{fA}/\sqrt{\text{Hz}}$

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Supply Voltage	6 V
Input Voltage	GND – 0.3 V to $V_S + 0.3$ V
Differential Input Voltage ¹	±5.0 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	–65°C to +150°C
Operating Temperature Range	–55°C to +125°C
Junction Temperature Range	–65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C
ESD	
HBM 8-Lead SOIC_N	±4000 V
FICDM 8-Lead SOIC_N	±1250 V

¹ The differential input voltage is limited to ±5 V or the supply voltage, whichever is less.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL CHARACTERISTICS

θ_{JA} is specified for worst-case conditions, that is, θ_{JA} is specified for the device soldered in a circuit board for surface-mount packages. This was measured using a standard two-layer board.

Table 4.

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	158	43	°C/W

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

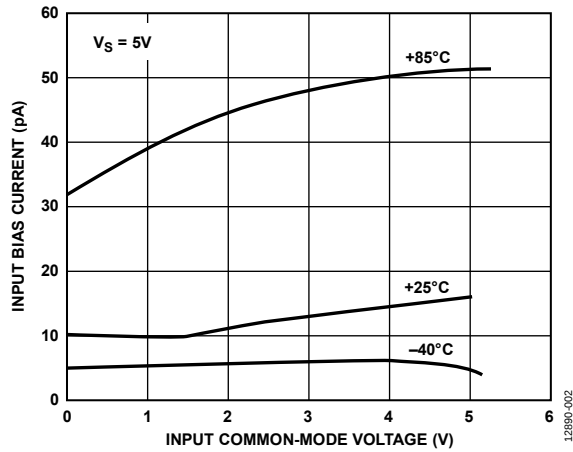


Figure 2. Input Bias Current vs. Input Common-Mode Voltage

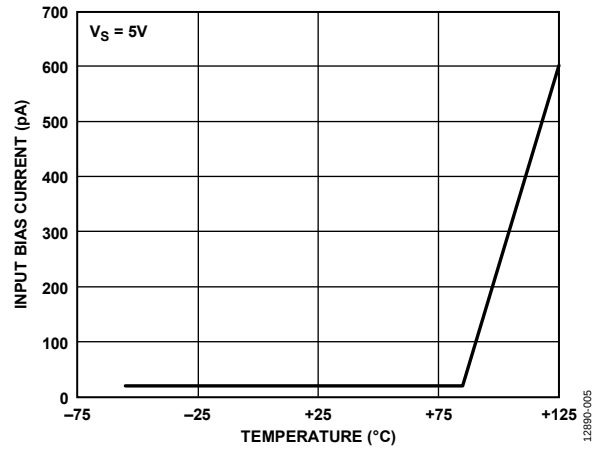


Figure 5. Input Bias Current vs. Temperature

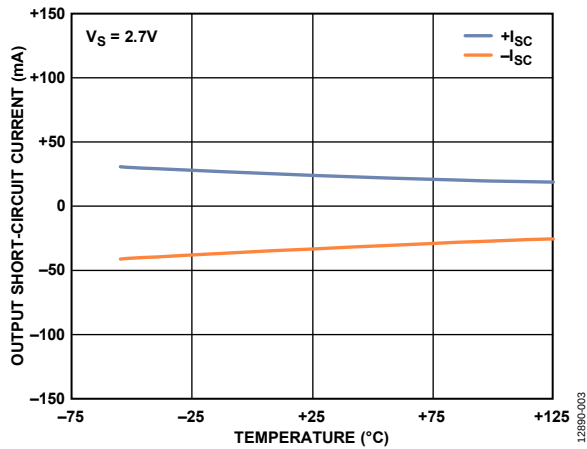


Figure 3. Output Short-Circuit Current vs. Temperature (2.7 V)

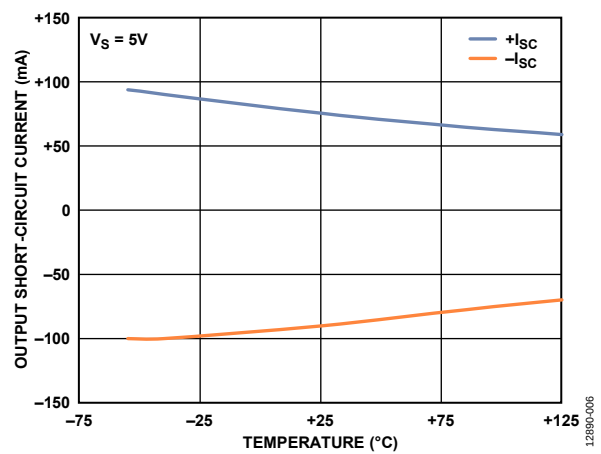


Figure 6. Output Short-Circuit Current vs. Temperature (5 V)

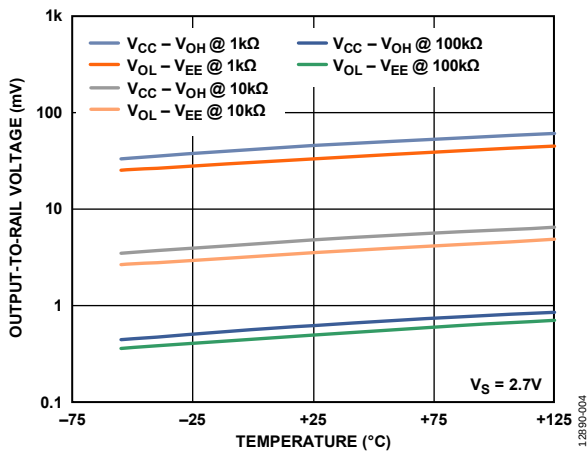


Figure 4. Output-to-Rail Voltage vs. Temperature (2.7 V)

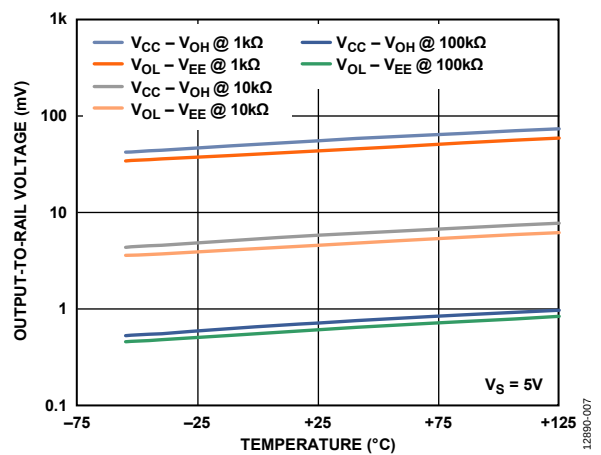


Figure 7. Output-to-Rail Voltage vs. Temperature (5 V)

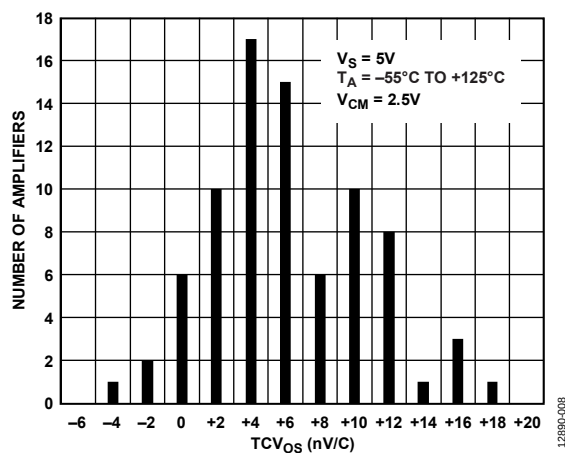


Figure 8. Input Offset Voltage Drift Distribution

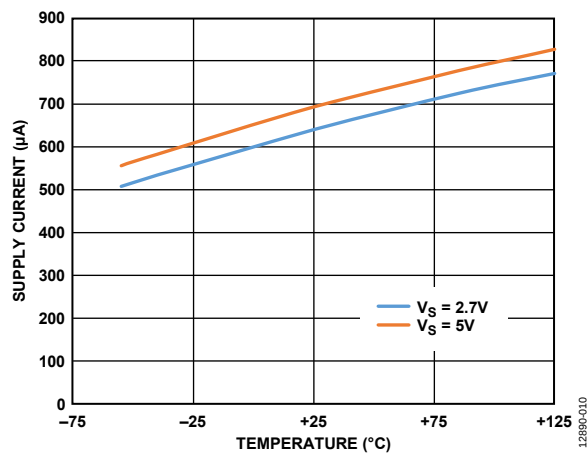


Figure 10. Supply Current vs. Temperature

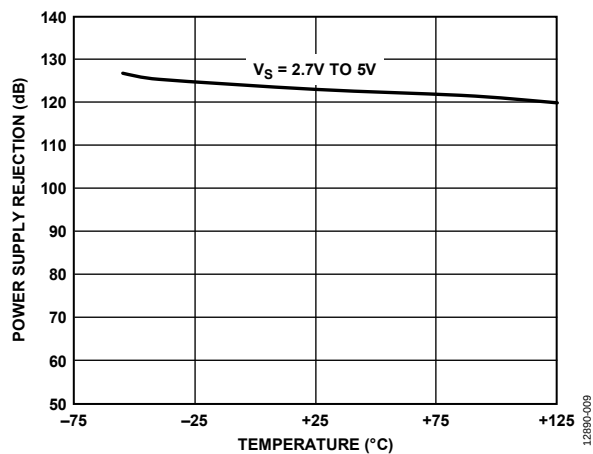
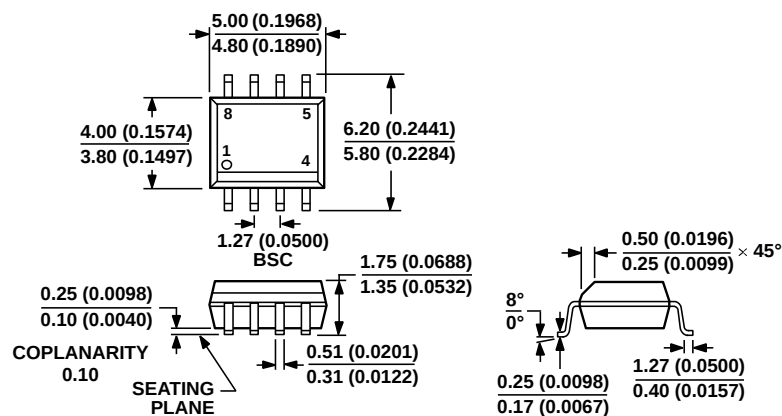


Figure 9. Power Supply Rejection vs. Temperature

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-012-AA
CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS
(IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR
REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

Figure 11. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)

Dimensions shown in millimeters and (inches)

012407-A

ORDERING GUIDE

Model ¹	Temperature Range	Package Description	Package Option
AD8629TRZ-EP	–55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8
AD8629TRZ-EP-R7	–55°C to +125°C	8-Lead Standard Small Outline Package [SOIC_N]	R-8

¹ Z = RoHS Compliant Part.