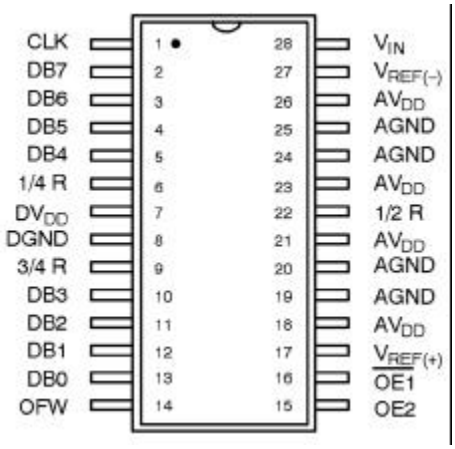
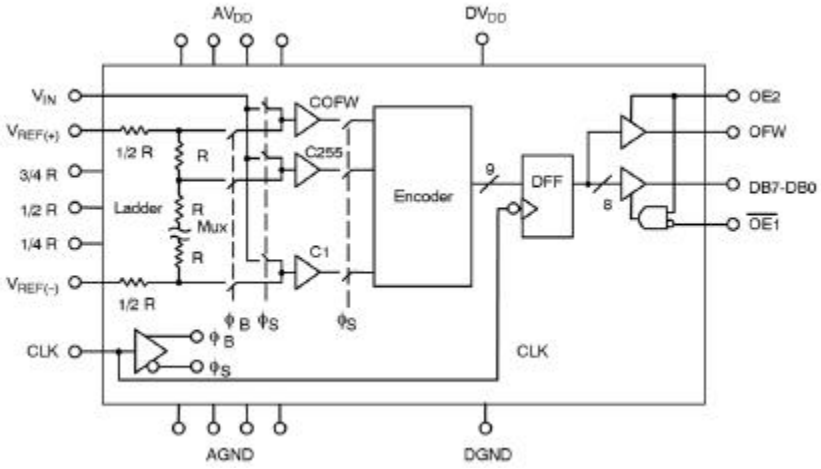
7684RP





FEATURES:

- Total dose hardness typical 100 krad (Si); dependent upon orbit
- Single event effects:
  - No single event latchup > 120 MeV/mg/cm^2
- Package:
  - 28 pin RAD-PAK® flat pack
  - 28 pin RAD-PAK® DIP
- High speed operation:
  - 0.001 to 15 MHz sampling rate
  - 1/2 LSB DNL to 10 MHz
- Monotonic; no missing codes
- High speed LC^{2}MOS technology
  - Latchup free
  - Single power supply:
    4 to 6 Volts
  - Interface to any input range between GND and V_{DD}
  - No sample/hold needed
  - Low operating power: I_{CC} (max) = 90 mA

DESCRIPTION:

Space Electronics' 7684RP (RP for RAD-PAK®) high speed 8-bit CMOS analog to digital converter features a typical 100 kilorad (Si) total dose tolerance. Using SEi's radiation-hardened RAD-PAK® packaging technology, the 7684RP is a 28 pin, 8-bit CMOS high speed analog to digital converter, which is designed for precision applications in video and data acquisition requiring conversion rates to 10 MHz with differential linearity error less than 1/2 LSB and low power consumption. One unique feature about the 7684RP is the input architecture which actually eliminates the need for an input track and hold and allows full scale input ranges from 1.2 to 5 Volts peak-to-peak, referred to ground or offset. To get the desired input range, the user needs to simply set V_{REF}(-) and V_{REF}(+). The 7684RP includes 256 clocked comparators, encoders, 3-state output buffers, a reference resistor ladder and associated timing circuitry. An overflow bit or flag is available to make it possible to achieve 9-bit resolution by connecting two devices in parallel. There is no effect on the data bits when the flag is in normal mode. Capable of surviving space environments, the 7684RP is ideal for satellite, spacecraft, and space probe missions. The patented radiation hardened RAD-PAK® technology incorporates radiation shielding in the microcircuit package. It eliminates box shielding while providing required lifetime in orbit. This product is available with packaging and screening up to Class S.

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TABLE 1. 7684RP PINOUT DESCRIPTION

PIN	SIGNAL	DESCRIPTION
1	CLK	Clock Input Pin
2	DB7	Data Bit 7 (MSB)
3	DB6	Data Bit 6
4	DB5	Data Bit 5
5	DB4	Data Bit 4
6	1/4 R	1/4 of Resistance Ladder
7	DV_{DD}	Power Supply of Digital Circuit
8	DGND	Digital Ground
9	3/4R	3/4 of Resistance Ladder
10	DB3	Data Bit 3
11	DB2	Data Bit 2
12	DB1	Data Bit 1
13	DB0	Data Bit 0 (LSB)
14	OFW	Digital Output Overflow
15	$\overline{OE2}$	Output Enable Control Pin
16	$\overline{OE1}$	Output Enable Control Pin
17	$V_{REF(+)}$	Positive Reference Voltage Pin
18	AV_{DD}	Power Supply of Analog Circuit
19	AGND	Analog Circuit Ground
20	AGND	Analog Circuit Ground
21	AV_{DD}	Power Supply of Analog Circuit
22	1/2 R	Center of Resistance Ladder
23	AV_{DD}	Power Supply of Analog Circuit
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Power Supply of Analog Circuit
27	$V_{REF(-)}$	Negative Reference Voltage Pin
28	V_{IN}	Analog Input

TABLE 2. 7684RP ABSOLUTE MAXIMUM RATINGS [1,2,3]

PARAMETER	SYMBOL	MIN	MAX	UNIT
V_{DD} to GND	V_{DD}	--	7	V
$V_{REF(+)}$ & $V_{REF(-)}$		GND - 0.5	V_{DD} + 0.5	V
All Inputs	V_{IN}	GND - 0.5	V_{DD} + 0.5	V
All Outputs	V_{OUT}	GND - 0.5	V_{DD} + 0.5	V

TABLE 2. 7684RP ABSOLUTE MAXIMUM RATINGS [1,2,3]

PARAMETER	SYMBOL	MIN	MAX	UNIT
Storage Temperature	T_{STG}	-65	150	°C
Operating Temperature	T_A	-55	125	°C

1. Operating at or beyond these limits may result in permanent damage to the device.
2. Normal operating is not guaranteed at these extremes.
3. V_{DD} refers to AV_{DD} and DV_{DD}. GND refers to AGND and DGND.

TABLE 3. 7684RP ELECTRICAL CHARACTERISTICS [1,2]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Resolution		8	--	--	Bits
Sampling Rate	F_S	0.1	--	10	MHz
Differential Non-Linearity @ 25 °C @ T_{MIN} to T_{MAX}	DNL	 0.4 0.6	 -- --	 1.6 2.1	LSB
Integral Non-Linearity, (Relative Accuracy) @ 25 °C @ T_{MIN} to T_{MAX}	INL	 -- --	 -- --	 ±1.6 ±2.1	LSB
Zero Scale Error	EZS	--	2	--	LSB
Full Scale Error	EFS	--	2	--	LSB
Dynamic Accuracy. Differential Non-Linearity	DNL	--	±0.3	--	LSB
Positive Ref. Voltage [3]	$V_{REF(+)}$	--	--	AV_{DD}	V
Negative Ref. Voltage	$V_{REF(-)}$	AGND	--	--	V
Ladder Resistance @ 25 °C @ T_{MIN} to T_{MAX}	R_L	 120 90	 -- --	 400 430	W
Ladder Temperature Coefficient [4]	R_{TCO}	--	--	3000	ppm/°C
Input Voltage Range	V_{IN}	$V_{REF(-)}$	--	$V_{REF(+)}$	V_{P-P}
Input Capacitance Sample [5,6]	C_{IN}	--	50	--	pF
Input Impedance [5]	Z_{IN}	--	10	--	mΩ
Aperture Delay [5]	t_{AP}	--	25	--	ns
Aperture Uncertainty (Jitter) [5]	t_{AJ}	--	--	66	ps
Logical "1" Voltage	V_{IH}	3.5	--	--	V
Logical "0" Voltage	V_{IL}	--	--	1.5	V

TABLE 3. 7684RP ELECTRICAL CHARACTERISTICS [1,2]

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT
Leakage Current [7] V_{IN} = DGND to DV_{DD}	I_{IN}				µA
CLK		--	--	±100	
$\overline{OE1}$ [8]					
@ 25 °C		-1	--	+50	
T_{MIN} to T_{MAX}		-1	--	+75	
$\overline{OE2}$ [9]					
@ 25 °C		-60	--	1	
T_{MIN} to T_{MA}X		-100	--	1	
Input Capacitance [5]		--	5	--	pF
Clock Timing Duty Cycle [5]		--	50	--	%
Logical "1" Voltage, I_{LOAD} = -1.0 mA	V_{OH}	4.3	--	--	V
Logical "0" Voltage, I_{LOAD} = -2.0 mA	V_{OL}	--	--	0.6	V
Output Capacitance [4,5]	C_O	--	5	--	pF
Data Hold Time [4,5]	t_{HLD}	--	55	--	ns
Data Valid Delay [4,5]	t_{DL}	--	50	--	ns
Data Enable Delay [4,5]	t_{DEN}	--	40	--	ns
Data Trisate Delay [4,5]	t_{DHZ}	--	40	--	ns
Operating Voltage (AV_{DD}, DV_{DD}) [2]	V_{DD}	4	--	6	V
Operating Current (AV_{DD} + DV_{DD}) [2]	I_{DD}				mA
@ 25 °C		--	--	75	
@ T_{MIN} to T_{MAX}		--	--	90	

1. Unless otherwise noted: AV_{DD} = DV_{DD} = 5V, FS = 10 MHz (50% Duty Cycle), $V_{REF(+)}$ = 4.1V, $V_{REF(-)}$ = AGND, T_A = 25 °C.
2. T_{MIN} to T_{MAX} = -55 °C to 125 °C.
3. Values guaranteed for functionality.
4. Guaranteed by design.
5. Typical value at T_A = 25 °C.
6. Switched capcitor analog input required driver with low output resistance.
7. All inputs have diodes to DV_{DD} and DGND. Input $\overline{OE1}$ has internal pull down. Input $\overline{OE2}$ has internal pull up. Input DC currents will not exceed specified limits for any input voltage between DGND and DV_{DD}.
8. Internal resistor to GND biases unconnected input to active low logical level.
9. Internal resistor to DV_{DD} biases unconnected input to active high logical level.

FIGURE 1. TIMING DIAGRAM

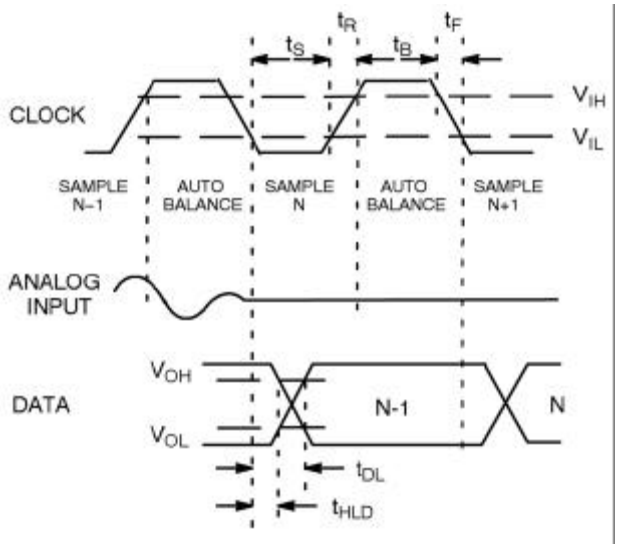


FIGURE 2. OUTPUT ENABLE/DISABLE TIMING DIAGRAM

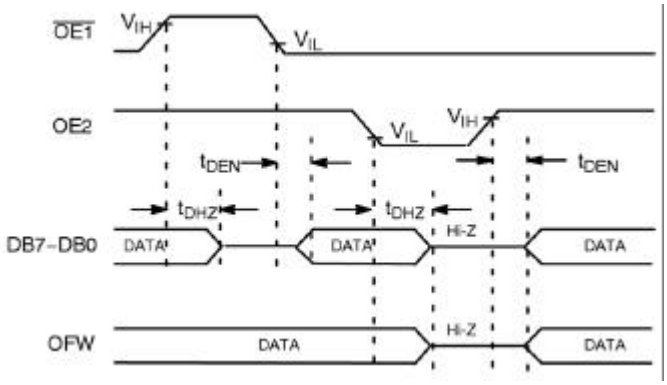


FIGURE 3. DNL MEASUREMENT

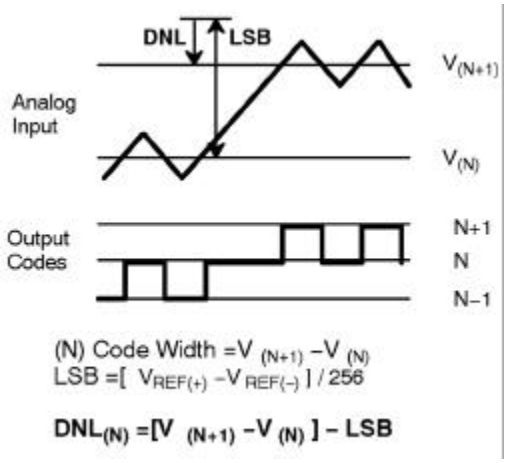


FIGURE 4. INL ERROR CALCULATION

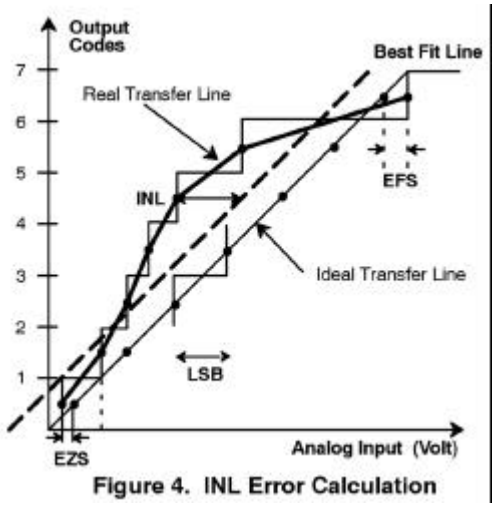


Figure 4. INL Error Calculation

FIGURE 5. FUNCTIONAL EQUIVALENT CIRCUIT AND INTERFACE TIMING

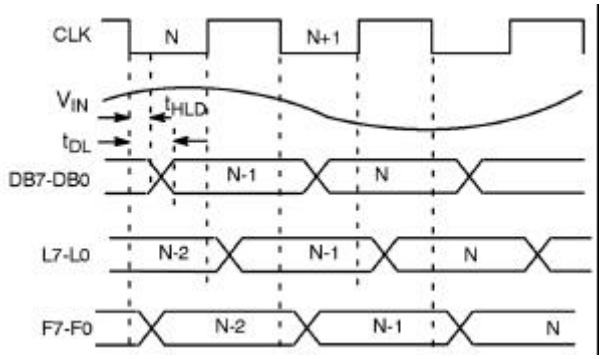
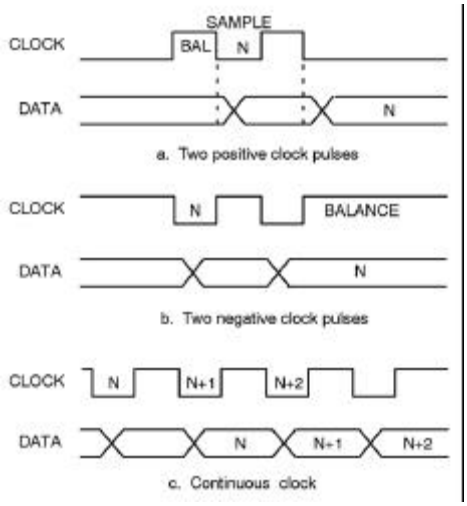
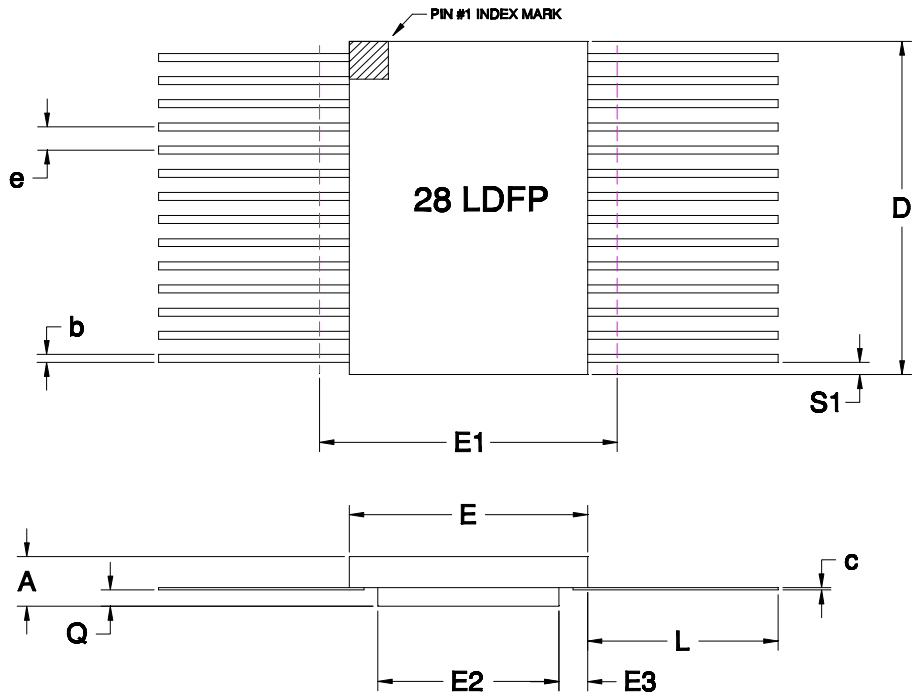


FIGURE 6. RELATIONSHIP OF DATA OF CLOCK





28 PIN FLAT PACKAGE

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.190	0.207	0.224
b	0.015	0.017	0.022
c	0.004	0.005	0.009
D	--	0.720	0.740
E	0.380	0.410	0.420
E1	--	--	0.440
E2	0.180	0.250	--
E3	0.030	0.080	--
e	0.050 BSC		
L	0.390	0.400	0.410
Q	0.062	0.073	0.081
S1	0.000	0.027	--
N	28		

F28-02
Note: All dimensions in inches

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