an Intel company

140 - 155 Mbit/s CMI Interface for E4/STM-1/OC-3 GD16361A/GD16362A*

Preliminary

General Description

The GD16361A and GD16362A is a chip- set intended for use as line interface in SDH STM-1 and PDH E4 systems, where electrical CMI coded interface is needed.

The chip set provides the line interface as described in ITU-T G.703 for system bit rates of 140 and 155 Mbit/s.

The chip set is designed to take care of all line interfaces processing in an SDH STM-1 interface, accommodating both STM-1 electrical and optical as well as PDH-E4 electrical interface.

The Transmitter - GD16361A

The transmit device, GD16361A, generates the CMI coded data signal from NRZ. The CMI code is transmitted via a differential output to the transformer or capacitor coupled line interface.

The data signal is re-timed in a PLL fully implemented on the chip, reducing jitter to a minimum. The integrated VCO is either synchronised directly to the incoming NRZ data stream (CDR mode with 19 MHz reference clock, typ.), or locked to the reference clock input (retiming mode, 70 MHz typ.). A clock output of 140/ 155 MHz allows for various clocking schemes and flexible system solutions.

The Receiver - GD16362A

The receive device, GD16362A, provides an equaliser to reshape the incoming signal, a clock and data recovery circuit that extracts the 311 MHz clock related to the CMI encoding and a decoder that turns CMI into NRZ. The receiver also holds an LOS detector in accordance with ITU-T G.775 The CMI decoder can be switched off when the interface is optical. In this case NRZ is passed through. In case of CMI code violations these are detected and output at CODV.

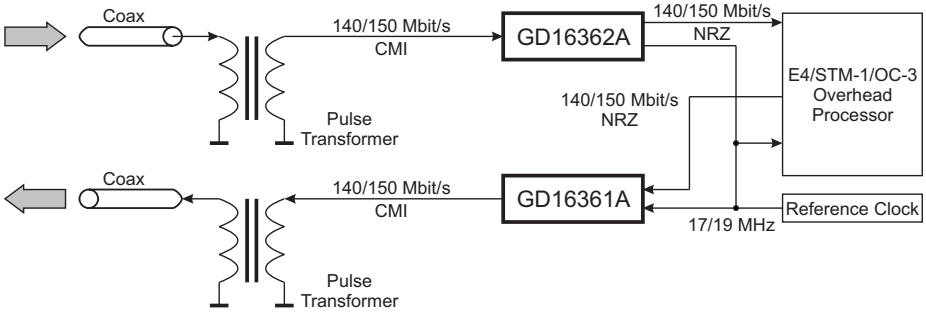


Figure 1. *Electrical Interface*

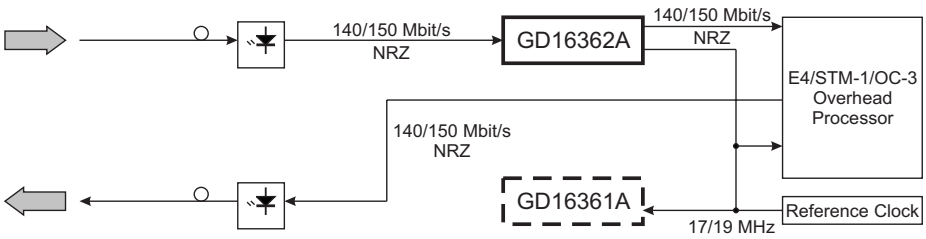


Figure 2. *Optical Interface*

Features

- Meet G.703 for 140 and 155 Mbit/s CMI Interface (return loss, receive sensitivity, and transmitter power).
- Meet G.751, G.823 and G.825 for jitter tolerance and jitter generation
- True LOS detection according to ITU-T G.775.
- On-chip equaliser working for more than 300 m RG-6/U cable (25 dB attenuation).
- CMI disable function for board level reconfiguration to optical interface.
- 3.3 V PECL high speed I/O's.
- CMOS configuration signals.
- Power consumption: 600 mW per device.
- 3.3 V supply voltage (5 V for VCO).
- Designed for low cost and volume production.
- BiCMOS technology.
- 28 pin SSOP package (5 x 10 mm), thermally enhanced.

28-Pin SSOP

Applications

- SDH/PDH Equipment with STM-1/ OC-3 and/or E4 Line interfaces.

: Patent pending

Functional Details

The GD16361A/62A chip set provides all required functions for reception and transmission at 140 Mbit/s (E4) and 155 Mbit/s (STM-1/OC-3) signals.

The GD16361A is the transmitter device (as shown in Figure 5 below) with:
- Clock/Data Recovery/Re-timing
- CMI Encoder
- Cable Driver.

The GD16362A is the receiver device (as shown in Figure 3 below) with:
- Cable Equaliser
- True LOS Detection (G.775)
- Clock/Data Recovery
- CMI Decoder.

The Line Interface

Adaptation to an electrical transmission interface with separation transformers is indicated in the figures. External components and transformers only indicate one way to apply the IC. The transformers could be omitted if direct connection from the IC out of the system is in compliance with the system design policy.

The Internal System Interface

The interface to the system's signal processor is also shown in the figures. All signal and clock paths are differential (balanced) high-speed lines for optimum signal quality, while status outputs and control inputs are single ended CMOS signals.

The Receiver – GD16362A

The incoming signal from the line is received via the balanced SIP/SIN inputs to the cable equaliser. **(SIP/SIN are self-biased ac-coupling is needed)**. This function block has a buffer amplifier in its input from where the signal branches off to the equaliser function and to the *Loss-Of- Signal* (LOS) detector. The LOS detector outputs the LOS output signal (CMOS) to the system processor. If the CMI decoder (see later) is disabled, then the equaliser block is bypassed. Bypassing the equaliser and CMI decoder is intended for use with an optical front end.

The signal continues via a selector to the *Clock and Data Recovery* (CDR) circuit. The CDR integrates:
- a Voltage Controlled Oscillator (VCO)
- a Phase Frequency Comparator (PFC)
- a Bang-Bang Phase Detector

into one integrated function block.

The VCO is a low noise Multi-Vibrator type differential oscillator with a tuning range of more than ±20 % of the nominal operating frequency.

Incoming data is sampled twice in each bit period, once on the transition of the previous bit period and once in the middle of the bit period. When a transition occurs between 2 consecutive bits - the value of the sample in the transition between the bits will show whether the VCO clock leads or lags the data. Hence the *Phase Locked Loop* (PLL) is controlled by the bit transition point, thereby ensuring that data is sampled in the middle of the eye, once the system is in CDR mode.

The external loop filter (R1 and C1) controls the characteristics of the PLL. Component values (please refer to Pin List) are sample values, which should be optimised for the specific application.

The binary output of either the PFC or the Bang-Bang phase detector (depending of the mode of the lock-detection circuit) is fed to a charge pump capable of sinking or sourcing current or tristating. The output of the charge pump (CLOF) is filtered through the external loop filter and controls the internal tuning voltage of the VCO.

The continuous lock-detect monitoring ensures that the VCO frequency never deviates more than ±500 ppm from its reference before the PLL is considered to be 'out of lock'. Hence the acquisition time is short and predictable, and the

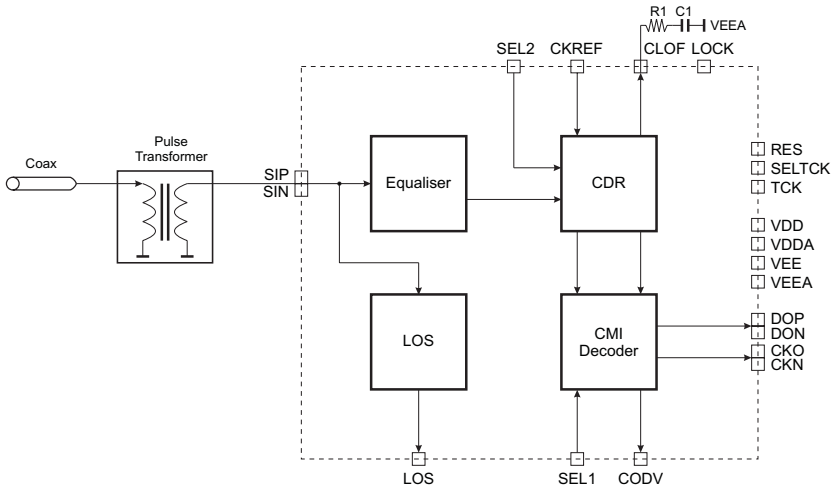


Figure 3. *The Receiver - GD16362A*

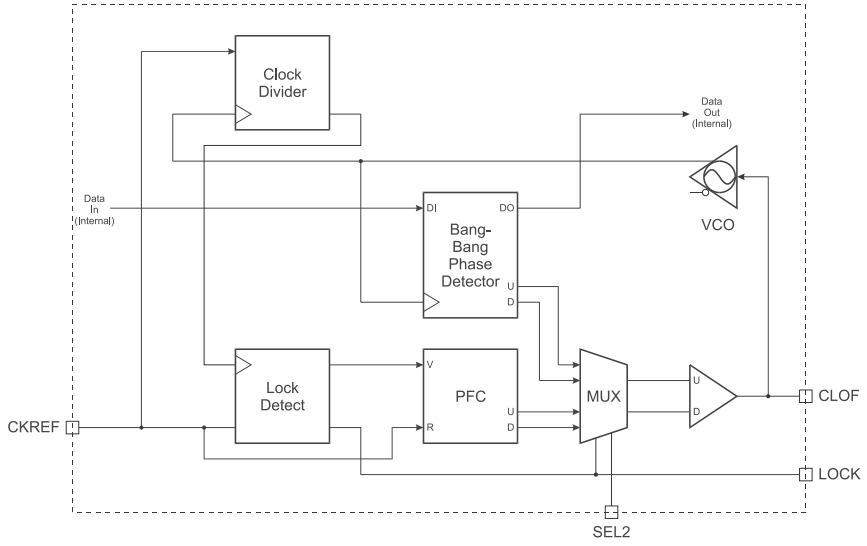


Figure 4. *The Phase Locked Loop Architecture - used in both GD16361A and GD16362A*

output clock (CKO/CKN) is always kept within its operating limits ensuring safe clocking of down stream circuitry. A LOCK output shows the lock state of the PLL.

The SEL2 input determines whether the PLL uses the input data stream as timing reference (if available), or if it is forced to lock onto the reference clock input CKREF.

The final block of the receiver is the CMI decoder which can be operated in decode or bypass mode, controlled by the SEL1 input. The CMI decoder deliveres:

- a differential clock (CKO/CKN)
- a data output (DOP/DON) in phase with the clock
- a signal (CODV) indicating illegal received CMI format.

The CODV signal has a 12.6/14.3 nsec bit period. In NRZ mode the CODV circuit will activate since the signal is not CMI. Please note that the receiving GD16362A will indicate the bit error, but it is able to decode the data correctly despite the enforced bit error. This means that the single introduced error is not transferred to the system ASIC.

The Transmitter – GD16361A

The signal input to the transmit function is the differential terminals (SIP/SIN). Transmit data goes via a selector to the transmit CDR, where the signal is retimed in order to minimise jitter in the system output. The transmit CDR is similar to the receive CDR described above. The LOCK output reflects its lock state, and the SEL2 determines whether the output data is timed by the incoming data stream - monitored by lock detect, or it is locked to the transmit reference clock (CKREF).

The CDR mode (SEL2 low) is intended for processing SONET/SDH signals, while the retiming mode (SEL2 high) is intended for processing PHD signals. The PDH signal is dominated by long CID sequences. Hence retiming og the outgoing data is based on the reference clock (CKREF), which in this mode is around 70 MHz typ.

From the transmit CDR the data signal continues to the CMI encoder. Corresponding to the decoder in the receive path, this function block can also operate in bypass or encode mode, controlled by the SEL1 input.

There is furthermore an input (VIOL) which can be used to force a single ’1’ sign error into the CMI encoded data stream for testing purpose.

The CMI encoder drives 2 separate output circuits, two identical differential open collector outputs (SOP/SON and SPP/SPN) intended for driving the line output, and/or for monitoring, respectively. The output current of both outputs is controlled by the CIP pin.

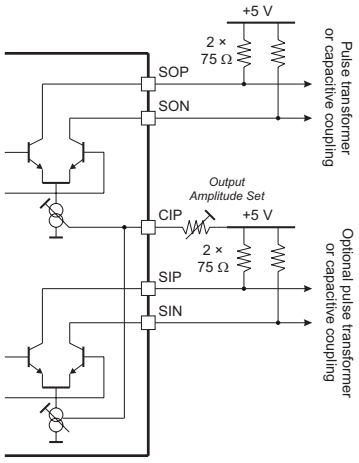


Figure 6. *Structure of the cable driver outputs and amplitude control.*

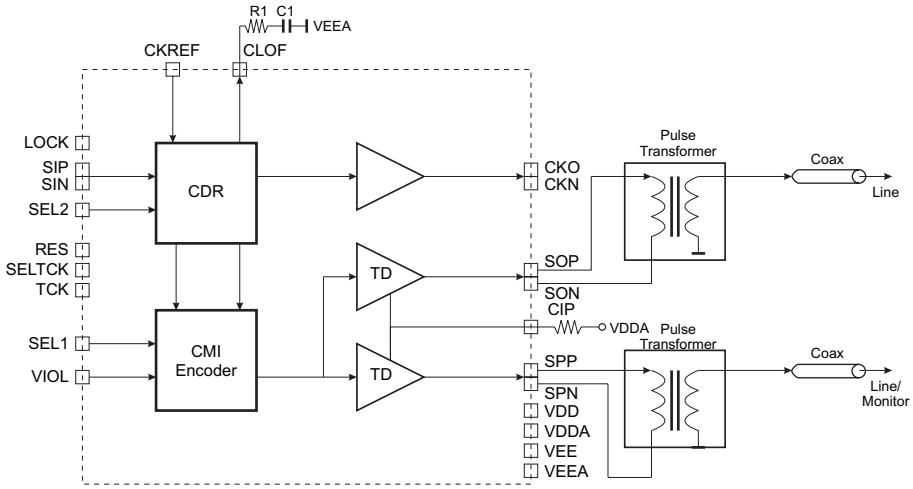


Figure 5. *The Transmitter - GD16361A*

The CIP signal controls the output circuits via a common current mirror. The sum of the output currents is proportional to the current flowing into the CIP terminal. The outputs can be turned off (shut down) by disconnecting the CIP terminal.

Since the CIP terminal is common to the two output circuits, it is recommended to terminate them both, even if only one is used. If one output circuit is left unterminated, the internal operation of the regulation circuit may be affected.

During normal operation, the typical voltage at the CIP terminal is approximately 1 V, and the CIP current is in range 5 - 10 mA.

Practical Considerations

The GD16361A/362A can be used with AC coupling or transformer coupling to the transmission line. If it is preferred to use transformers, any high-speed pulse transformer can in principle be used.

In order to achieve the best possible return loss, care must be taken to design the signal traces as 50 or 75 Ω transmission lines in the PCB, corresponding with the application. Unused cable driver outputs should be terminated in a dummy resistor pair to VDD to optimise working conditions yet minimising power consumption.

If the receiver’s clock output is unused, it should be terminated with dummy resistors to VDD –2 V.

Please Note:
The VCO of the devices are supplied from the VDDA (+5 V). Hence, the PLL performance may be infuenced by noise. The VDDA terminal should therefore be de-coupled well. The 5 V connection to the DC termination of the cable driver(s) should be carefully de-coupled in order to prevent any noise feedback from the cable drivers to the VCO’s.

Thermal Conditions

The integrated heat sink of the GD16361A/362A packages should be connected to a ground plane in the PCB for optimal cooling of the devices. Electrical connection is not required for the operation of the devices, but if present it improves the electrical shielding of the devices against electrical noise etc.

Observations

The figures below show the measured CMI ‘1’s and ‘0’s as observed in the GD90361/362 evaluation board. The oscillograms show unaveraged data, observed on the transmitter’s cable driver output with the transmitter running in CMI mode, differential connection from SOP/SON to pulse transformer.

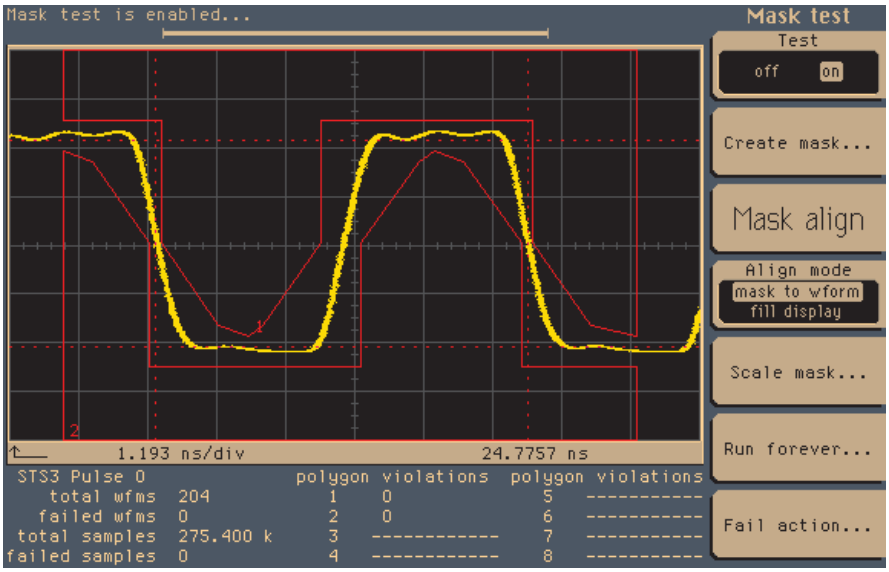


Figure 7. *The GD16361A Transmitter running CMI zeroes.*

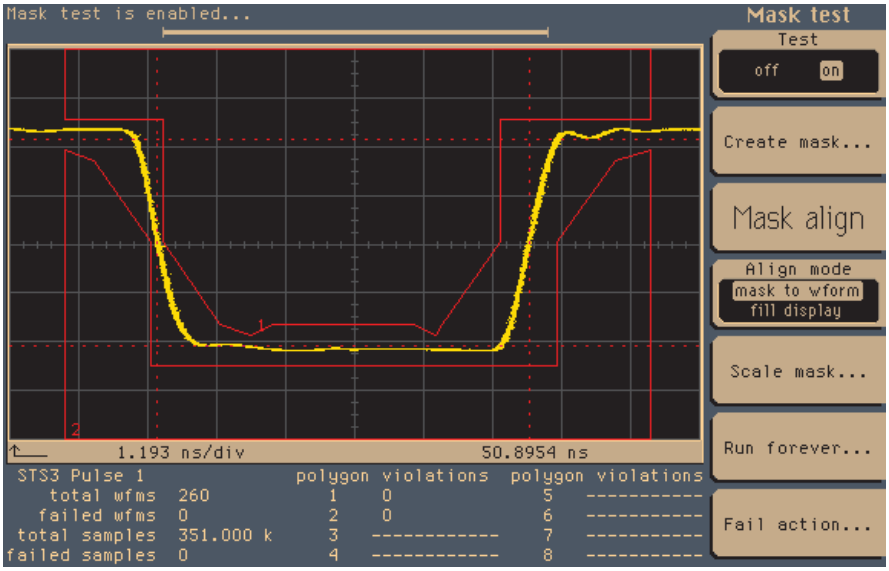


Figure 8. *The GD16361A Transmitter running CMI ones.*

Pin List - GD16361A (Transmitter)

Mnemonic:	Pin No.	Pin Type:	Description:
SIP, SIN	21, 20	PECL IN	Serial differential data input from overhead processor.
SOP, SON	7,8	ANL OUT	Serial differential data output to transformer.
SPP, SPN	10, 11	ANL OUT	Serial differential data output to transformer.
CKO, CKN	4, 5	PECL OUT	Differential 140/155 MHz clock output.
CKREF	1	CMOS IN	19 MHz (STM-1/OC-3) Reference clock input for the CDR. When SEL2 is high the GD16361A output frequency is locked to the CKREF input, and CKREF should be 70 MHz (PDH) or 78 MHz (STM-1) bit-rate/2. When low the CKREF is used for acquisition only - the output frequency is locked to the SIP/SIN.
SEL1	14	CMOS IN	When low, the CMI encoder is enabled. When high, data is passed unchanged (NRZ mode).
SEL2	15	CMOS IN	When high the GD16361A output frequency is locked to the CKREF input. When low the output frequency is locked to the SIP/SIN – CKREF is used for acquisition only.
VIOL	18	CMOS IN	Insert Code Violation. Positively triggered, one violation is inserted (“1" level toggled).
LOCK	16	CMOS OUT	Lock alarm output. When low the divided VCO frequency deviates more than 500 ppm from CKREF. Note 2.
CIP	9	ANL	CML open collector current control input. Connect resistor to positive power supply 5 V. Output current through cable driver propotional to I_{CIP}.
CLOF	24	ANL	Loop filter external capacitance pin. Note 1.
RES	23	ANL	For test purposes only, connect to VEE.
SELTCK	28	ANL	For test purposes only, connect to VDD.
TCK	27	ANL	Test clock input. For test purpose only, connect to VEEA.
VDD	3, 6, 12, 17, 19	PWR	3.3 V power.
VDDA	25	PWR	5 V power for VCO.
VEE	2, 13, 22,	PWR	0 V power.
VEEA	26	PWR	0 V power for VCO.
Heat Sink	Bottom		Connect to VEE (ground plane) for optimal cooling.

Note 1: The loop filter should be optimised to the specific application. A 8 Ω resistor in series with a 10 μF capacitor can be used as sample values.

Note 2: In retiming mode (SEL2=High), the LOCK signal is not applicable as the CDR is inactive.

Package Pinout - GD16361A

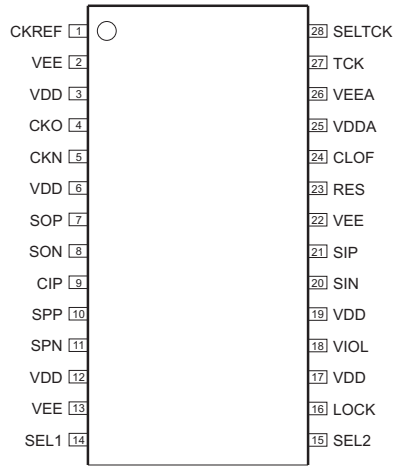


Figure 9. *Package 28 pin, Top View.*

Pin List - GD16362A

Mnemonic:	Pin No.:	Pin Type:	Description:
SIP, SIN	7, 8	ANL IN	Differential serial data input. Internally selfbiased.
DOP, DON	22, 21	PECL OUT	Differential serial data output to overhead processor.
CKO, CKN	25, 24	PECL OUT	Differential 140/155 MHz clock output. Note that the CML data must be present at SIP/SIN in order for CKO/CKN to exist as clock frequency.
CKREF	28	CMOS IN	17/19 MHz Reference clock input for the CDR. When SEL2 is high the GD16362A output frequency is locked to the CKREF input. When low the CKREF is used for acquisition only - the output frequency is locked to the SIP/SIN.
SEL1	14	CMOS IN	When low the CMI decoder is enabled. When high, data is passed unchanged (NRZ mode).
SEL2	15	CMOS IN	When high the GD16362A output frequency is locked to the CKREF input. When low the CKREF is used for acquisition only - the output frequency is locked to the SIP/SIN.
CODV	19	CMOS OUT	Outputs a 12.6/14.3 ns high pulse upon a CMI code error.
LOS	18	CMOS OUT	Asynchronous output. High level indicates loss of signal, i.e. input amplitude has dropped below -18..-35 dB for a 10..255 bit period according to ITU-T G.775 (11/94)
LOCK	20	CMOS OUT	Lock alarm output. When low the divided VCO frequency deviates more than 500 ppm from CKREF.
CLOF	5	ANL	External loop filter. Note 1.
RES	13	ANL	For test purposes only, connect to VEE.
SELTCK	1	ANL	For test purposes only, connect to VDD.
TCK	2	ANL	Test clock input. For test purpose only, connect to VEEA.
VDD	6, 10, 17, 23, 26	PWR	3.3 V power.
VDDA	4	PWR	5 V power for VCO.
VEE	9,11,12, 16,27	PWR	0 V power.
VEEA	3	PWR	0 V power for VCO.
Heat Sink	Bottom		Connect to VEE (ground plane) for optimal cooling.

Note 1: The loop filter should be optimised to the specific application. A 8 Ω resistor in series with a 10 μF capacitor can be used as sample value.

Package Pinout – GD16362A

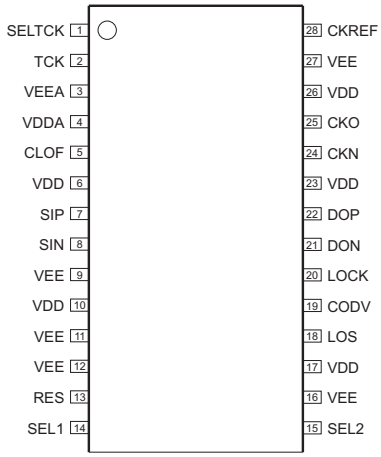


Figure 10. *Package 28 pin SSOP, Top View*

Maximum Ratings

These are the limits beyond which the component may be damaged.
All voltages are referenced to VEE unless otherwise noted.

Symbol:	Characteristic	Conditions	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD}, V_{DDA}	Supply Voltage		0		6	V
V_{O} *max*	Output Voltage	PECL/CMOS	-0.5		V_{DD} + 0.5	V
$I_{O,PECL}$ *max*	Output Current	PECL			40	mA
$I_{O,CMOS}$ *max*	Output Current	CMOS	-10		10	mA
V_{I} *max*	Input Voltage	PECL/CMOS	-0.5		V_{DD} + 0.5	V
I_{I} *max*	Input Current	PECL/CMOS	-1.0		1.0	mA
V_{OI} *ESD*	Static Discharge Voltage	Note 1	500			V
T_{O}	Operating Temperature	Junction	-55		+150	°C
T_{S}	Storage Temperature	Junction	-65		+175	°C

Note 1: Human body model (100 pF, 1500 Ω) MIL 883 std.

DC Characteristics

T_{CASE} = -40 °C to 85 °C.
Thermal Resistance θ_{J-C} = 10 °C/W.
All voltages in table are referred to VEE unless otherwise noted.
Currents are defined positive into the pin.

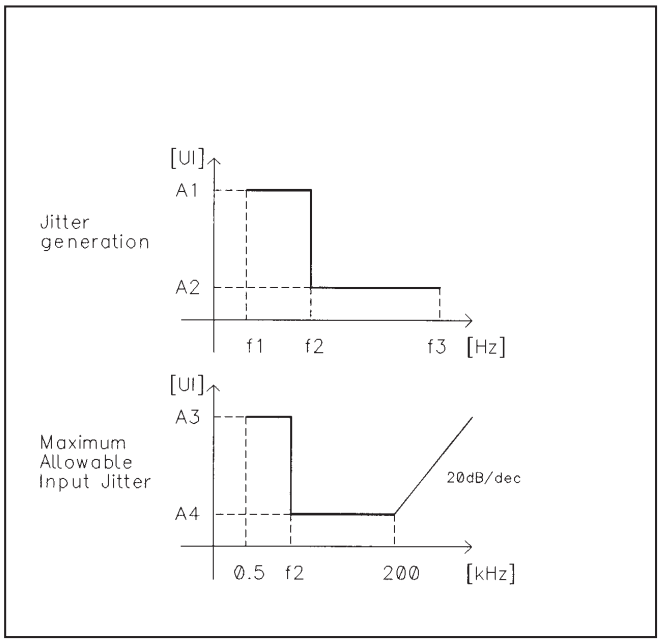
Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
V_{DD}	Supply Voltage		3.15	3.30	3.45	V
V_{DDA}	Supply Voltage, Analog		4.75	5.00	5.25	V
$I_{DD,GD16361A}$	Supply Current, GD16361A	Note 1		130	150	mA
$I_{DDA,GD16361A}$	Supply Current, GD16361A	Note 1		14	18	mA
$I_{DD,GD16362A}$	Supply Current, GD16362A	Note 1		125	150	mA
$I_{DDA,GD16362A}$	Supply Current, GD16362A	Note 1		14	18	mA
$V_{IH,PECL}$	PECL Differential Input HI Voltage	Note 2	V_{DD} -1.75		V_{DD} -0.45	V
$V_{IL,PECL}$	PECL Differential Input LO Voltage	Note 2	V_{DD} -2.00		V_{DD} -0.70	V
$V_{IDIFF,PECL}$	PECL Differential Input Voltage	Note 2	0.250	0.500	1.400	V
$I_{IH,PECL}$	PECL Input HI Current	V_{IH} *PECL, max*			100	µA
$I_{IL,PECL}$	PECL Input LO Current	V_{IL} *PECL, min*	-100			µA
$V_{OH,PECL}$	PECL Output HI Voltage	Note 3	V_{DD} -1.11		V_{DD} -0.67	V
$V_{OL,PECL}$	PECL Output LO Voltage	Note 3	V_{DD} -2.00		V_{DD} -1.50	V
$V_{ODIFF,PECL}$	PECL Output Differential Voltage	Note 3	390		1330	mV
$V_{IH,CMOS}$	CMOS Input HI Voltage		V_{DD} x0.8		V_{DD}	V
$V_{IL,CMOS}$	CMOS Input LO Voltage		0		V_{DD} x0.2	V
I_{IH} *CMOS*	CMOS Input HI Current	V_{IH} *CMOS, max*			100	µA
I_{IL} *CMOS*	CMOS Input LO Current	V_{IL} *CMOS, min*	-100			µA
V_{OH} *CMOS*	CMOS Output HI Voltage	I_{OH}*= 1mA*	V_{DD} - 0.2		V_{DD}	V
V_{OL} *CMOS*	CMOS Output LO Voltage	I_{OL}*= -1mA*	0		0.2	V

Note 1: Supply pin currents. DC currents through external terminations are not included.
Note 2: Although $V_{IDIFF,PECL}$ may vary within $V_{IH,MAX}$ and $V_{IL,MIN}$, it must not exceed $V_{IDIFF,MAX}$.
Note 3: 50 Ω termination to VDD -2.0 V.

AC Characteristics, General

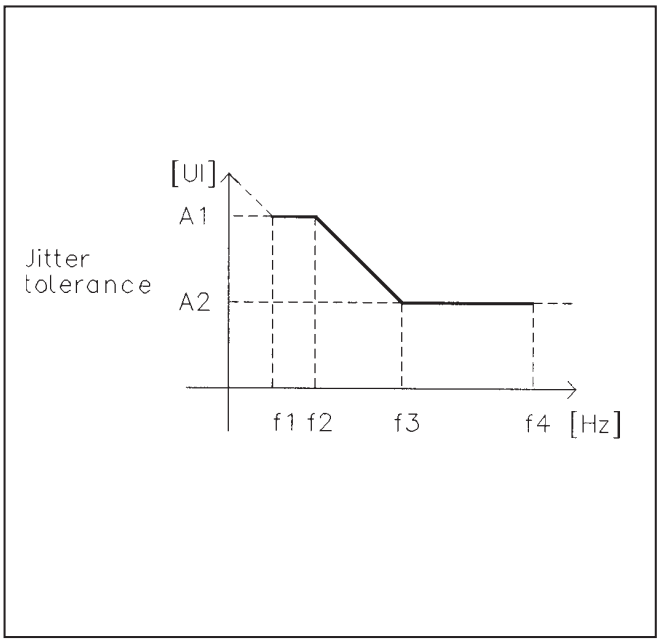
T_{CASE} = -40 °C to 85 °C.

GD16361A



	f1 [Hz]	f2 [Hz]	f3 [Hz]	A1 [UI]	A2 [UI]	A3 [UI]	A4 [UI]
E4	200	10k	3.5M	1.5_{P-P}	0.075_{P-P}	1.45_{P-P}	0.025_{P-P}
STM-1	500	65k	1.3M	1.5_{P-P}	0.15_{P-P}	1.45_{P-P}	0.10_{P-P}
OC-3				0.01_{RMS}	0.01_{RMS}	0.005_{RMS}	0.005_{RMS}

GD16362A



	f1 [Hz]	f2 [Hz]	f3 [Hz]	f4 [Hz]	A1 [UI]	A2 [UI]
E4	200	0.5k	65k	1.3M	1.5	0.075
STM-1-optical	500	6.5k	65k	1.3M	1.5	0.15
STM-1-electrical	500	3.25k	65k	1.3M	1.5	0.075
OC-3	300	6.5k	65k	-	1.5	0.15

Symbol:	**Characteristic:**	**Conditions:**	**MIN.:**	**TYP.:**	**MAX.:**	**UNIT:**
R_{Duty}	Duty cycle, CKREF	Note 1	40/60		60/40	%
F_{VCO}	VCO frequency range		130		160	MHz
t_{Acq-PU}	Acquisition time, GD16361A/362A	Power up to lock			100	µs
$t_{Acq-INT}$	Acquisition time, GD16362A	Input signal valid to lock			10	µs
V_{CID}	Number of consecutive identical digits	Note 2	>120			Units
$t_{R,PECL}$	PECL Rise time	Note 3			800	ps
$t_{F,PECL}$	PECL Fall time	Note 3			800	ps
$t_{R,\ CMOS}$	CMOS Rise time	Note 4			2	ns
$t_{F,CMOS}$	CMOS Fall time	Note 4			2	ns

Note 1: Duty cycle measured at V_{TH} = 1.4 V in CDR-mode. In forward clocking mode a jitter-free CKREF signal is required and duty cycle should be as close as possible to 50/50, especially at GD16361A in re-timing mode (SEL2=High).
Note 2: TBD
Note 3: 20 - 80 %, 50 Ω to VDD -2.0 V.
Note 4: 20 - 80 %, 10 pF and 100 µA load.

AC Characteristics, GD16361A (Transmitter)

Input Timing Relations when SEL2 is High

Improved function of GD16361A compared to GD16361: When SEL2 is High, the GD16361A transmitter works as a retiming device for the NRZ incoming PECL data stream (forward clocking scheme). Data is clocked in in the middle of the half periods of the reference clock signal REFCK. On the basis of REFCK, a 155 MHz signal is generated internally. This signal is used for clocking data into the registers of the GD16361A in the retiming mode. The timing relationship for the retiming mode is shown below:

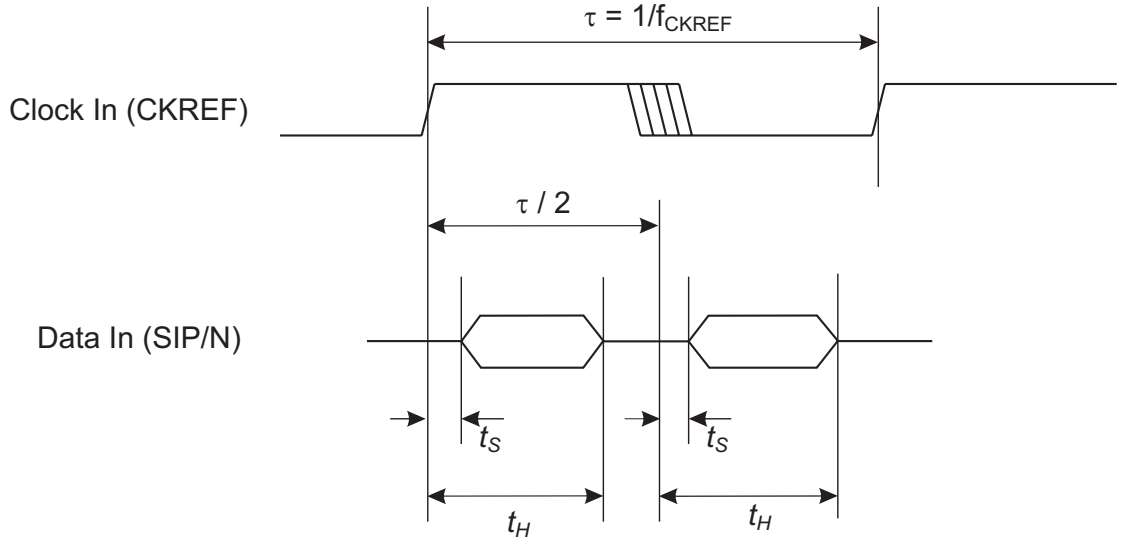


Figure 11. *The timing relationship for the retiming mode.*

Input Timing Relations when SEL2 is Low

When SEL2 is LOW, the device operates as a Clock/Data Recovery block, and automatically locks to the incoming data stream. The REFCK is in this case 1/8 of the line rate, i.e. 17.4 or 19.44 MHz. There is no phase relationship requirement between REFCK and the incoming data.

Output Timing Relations

An output clock signal (CKO/N) from the transmitter is available. The falling (negative) edge of the CKO signal is latching data into the output buffers. The timing between the clock (CKO/N) and the cable driver output data (SOP/N; SPP/N) is shown below:

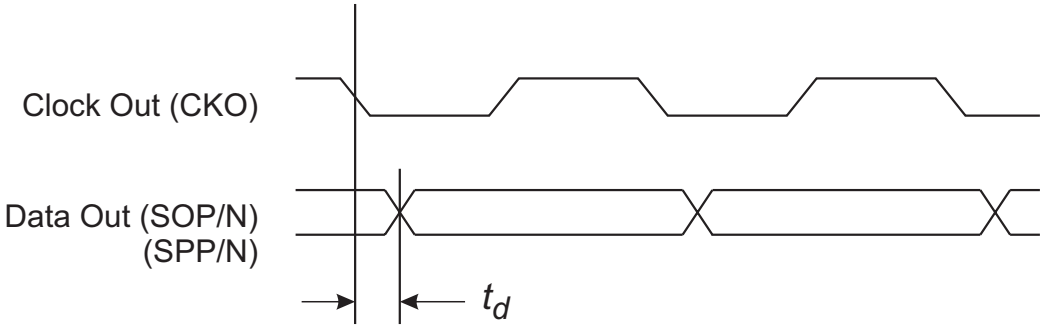


Figure 12. *The timing between the clock out (CKO/N) and output data (SOP/N, SPP/N)*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
$t_{S,\ max}$	Setup time				2400	ps
$t_{H,\ min}$	Hold time		4000			ps
t_d	Delay, clock to data out	Note 1	500	600	1500	ps

Note 1: Output terminated in 75 Ω to VDDA || (100 nF in series with 75 Ω) to ground.

AC Characteristics, GD16362A (Receiver)

Output Timing Relations

The received and decoded PECL output data (DOP/DON), NRZ format, is latched out on the falling edge of the output clock (CKO) as shown below:

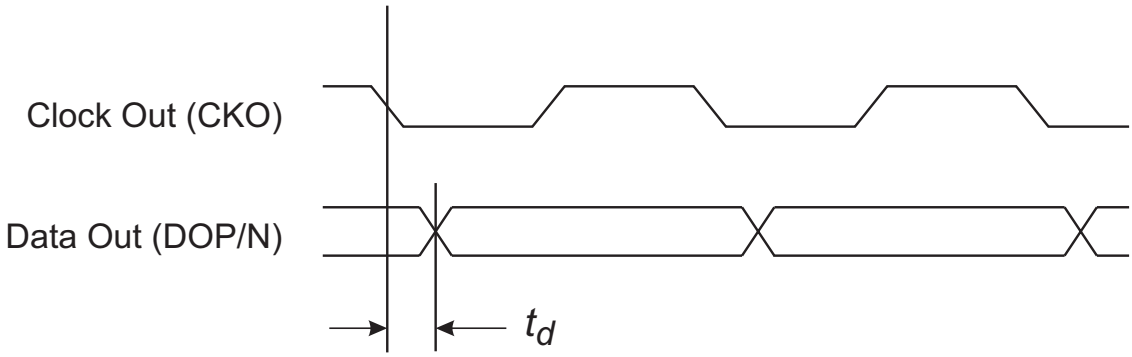
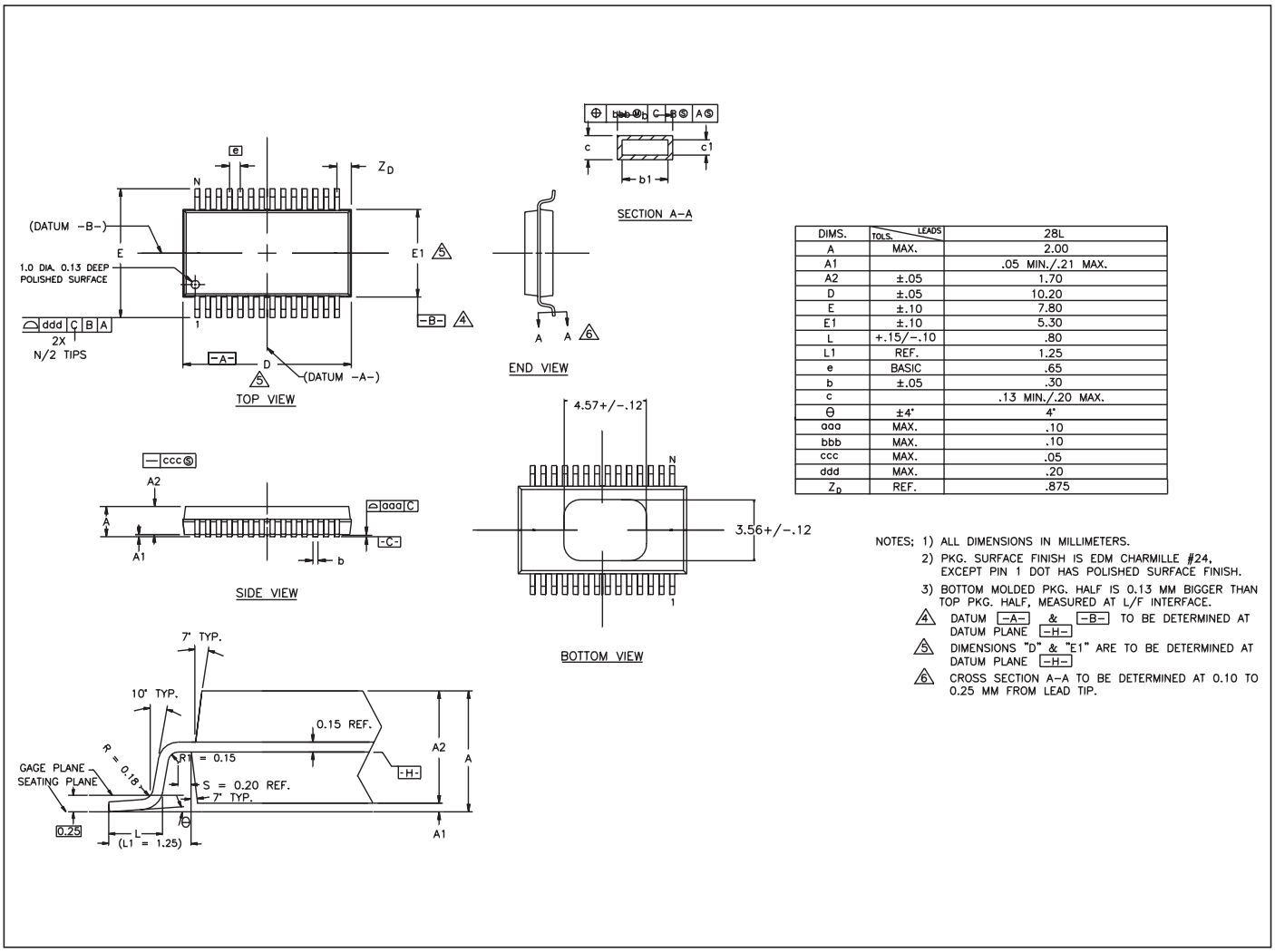


Figure 13. *The timing between the clock out (CKO/N) and output data (DOP/N)*

Symbol:	Characteristic:	Conditions:	MIN.:	TYP.:	MAX.:	UNIT:
t_d	Delay, clock to data out	Note 1	600		1300	ps

Note 1: 20 - 80 %, 50 Ω to VDD -2.0 V.

Package Outline



DIMS.	TOLS. \ LEADS	28L
A	MAX.	2.00
A1		.05 MIN./.21 MAX.
A2	±.05	1.70
D	±.05	10.20
E	±.10	7.80
E1	±.10	5.30
L	+.15/-.10	.80
L1	REF.	1.25
e	BASIC	.65
b	±.05	.30
c		.13 MIN./.20 MAX.
θ	±4°	4°
aaa	MAX.	.10
bbb	MAX.	.10
ccc	MAX.	.05
ddd	MAX.	.20
Z_D	REF.	.875

NOTES:
1) ALL DIMENSIONS IN MILLIMETERS.
2) PKG. SURFACE FINISH IS EDM CHARMILLE #24, EXCEPT PIN 1 DOT HAS POLISHED SURFACE FINISH.
3) BOTTOM MOLDED PKG. HALF IS 0.13 MM BIGGER THAN TOP PKG. HALF, MEASURED AT L/F INTERFACE.
4) DATUM -A- & -B- TO BE DETERMINED AT DATUM PLANE -H-
5) DIMENSIONS "D" & "E1" ARE TO BE DETERMINED AT DATUM PLANE -H-
6) CROSS SECTION A-A TO BE DETERMINED AT 0.10 TO 0.25 MM FROM LEAD TIP.

Figure 14. *Package Outline, 28 pin SSOP (28BA). All dimension are in mm.*

Note: Caution should be taken during design, assembly and processing to prevent deposited board solder from holding the leads up off the board. “A1” dimension is allowed to be zero.

Device Marking

External References

ITU-T G.703 (04/91) : General Aspects of Digital transmission systems, Terminal Equipment.
ITU-T G.751 (11/88) : Digital multiplex equipments operating at the third order bit rate of 34368 kbit/s.
ITU-T G.775 (11/94) : LOS and AIS defect detection criteria.
ITU-T G.823 (3/93) : The control of jitter and wander within digital networks based on the 2048 kbit/s hierarchy.
ITU-T G.825 (9/97) : The control of jitter and wander within digital networks based on SDH.

Ordering Information

To order, please specify as shown below:

Product Name:	Type:	Package Type:	Case Temperature Range:
GD16361A-28BA	**Transmitter**	28 pin SSOP	-40..85°C
GD16362A-28BA	**Receiver**	28 pin SSOP	-40..85°C

GD16361A/GD16362A*, Data Sheet Rev.: 17 - Date: 15 January 2001

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