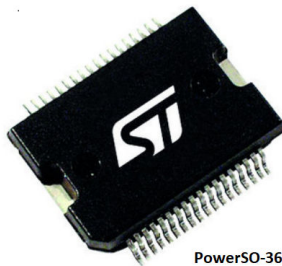


## Octal channel high-side driver



### Features

- $V_{CC}/2$  compatible input
- Junction overtemperature protection
- Case overtemperature protection for thermal independence of the channels
- Current limitation
- Short-circuit load protection
- Undervoltage shutdown
- Protection against loss of ground
- Very low standby current
- Compliance to 61000-4-4 IEC test up to 4 kV

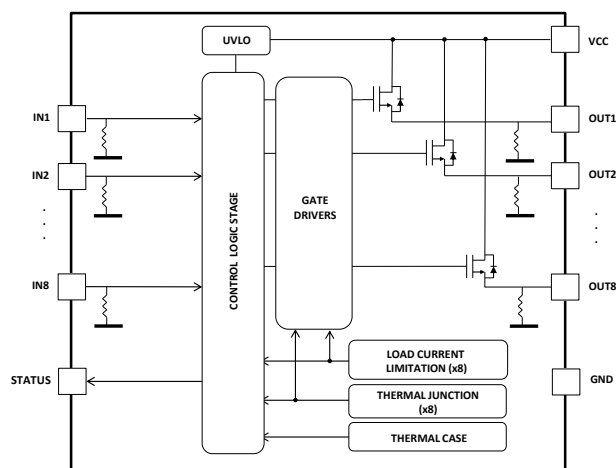
### Description

The VN808-E and VN808-32-E are monolithic devices, realized in STMicroelectronics VIPower M0-3 technology, intended to drive any kind of load with one side connected to ground. Active current limitation combined with thermal shutdown and automatic restart, protect the device against overload. In overload conditions, the channel turns OFF and ON again automatically in order to maintain the junction temperature between  $T_{JSD}$  and  $T_R$ . If this condition causes case temperature reach  $T_{CSD}$ , overloaded channels are turned OFF and restart only when case temperature decreases down to  $T_{CR}$ . Non-overloaded channels continue to operate normally. The device automatically turns OFF in case of ground pin disconnection. This device is especially suitable for industrial applications conform to IEC 61131.

| Product status link                                                                 |                    |           |          |
|-------------------------------------------------------------------------------------|--------------------|-----------|----------|
| VN808-E                                                                             |                    |           |          |
| VN808-32-E                                                                          |                    |           |          |
| Product label                                                                       |                    |           |          |
|  |                    |           |          |
| Type                                                                                | $R_{DS(on)}^{(1)}$ | $I_{OUT}$ | $V_{CC}$ |
| VN808-E                                                                             | 150 mΩ             | 0.7 A     | 45 V     |
| VN808-32-E                                                                          | 150 mΩ             | 1 A       | 45 V     |

1. Per channel

Figure 1. Internal schematic



## 1 Maximum ratings

**Table 1. Absolute maximum ratings**

| Symbol     | Parameter                                                                                                                                             | Max.               | Unit             |
|------------|-------------------------------------------------------------------------------------------------------------------------------------------------------|--------------------|------------------|
| $V_{CC}$   | DC Supply Voltage                                                                                                                                     | 45                 | V                |
| $-I_{GND}$ | DC Ground Reverse Current                                                                                                                             | 250                | mA               |
|            | TRAN ground reverse current (pulse duration < 1 ms)                                                                                                   | 6                  | A                |
| $I_{OUT}$  | DC Output Current                                                                                                                                     | Internally limited | A                |
| $-I_{OUT}$ | Reverse DC Output Current                                                                                                                             | 5 <sup>(1)</sup>   | A                |
| $I_{IN}$   | DC Input Current                                                                                                                                      | ±10                | mA               |
| $V_{IN}$   | Input Voltage Range                                                                                                                                   | -3/+ $V_{CC}$      | V                |
| $V_{ESD}$  | Electrostatic discharge (R = 1.5K $\Omega$ ; C = 100pF)                                                                                               | 2000               | V                |
| $P_{TOT}$  | Power dissipation at $T_c = 25^\circ\text{C}$                                                                                                         | 10                 | W                |
| EAS        | Single pulse Avalanche Energy per channel, all channels driven simultaneously ( $T_{amb} = 125^\circ\text{C}$ , $I_{OUT} = 0.6\text{ A}$ per channel) | 1.15               | J                |
| $T_J$      | Junction Operating Temperature                                                                                                                        | Internally limited | $^\circ\text{C}$ |
| $T_c$      | Case Operating Temperature                                                                                                                            | Internally limited | $^\circ\text{C}$ |
| $T_{STG}$  | Storage Temperature                                                                                                                                   | -40 to 150         | $^\circ\text{C}$ |

1. Limit intended with each couple of  $OUT_x$  ( $x = 1...8$ ) pin shorted on the application board

**Table 2. Thermal data**

| Symbol       | Parameter                                              | Max. Value | Unit               |
|--------------|--------------------------------------------------------|------------|--------------------|
| $R_{th(JC)}$ | Thermal Resistance, Junction-to-case                   | 1.3        | $^\circ\text{C/W}$ |
| $R_{th(JA)}$ | Thermal Resistance, Junction-to-ambient <sup>(1)</sup> | 17         |                    |

1. When mounted on FR4 printed circuit board with 0.5 cm<sup>2</sup> of copper area (at least 35  $\mu\text{m}$  thick) connected to all TAB pins.

## 2 Electrical characteristics

10.5 V < V<sub>CC</sub> < 32 V; - 40 °C < T<sub>J</sub> < 125 °C; unless otherwise specified.

**Table 3. Power Section**

| Symbol                | Parameter                                        | Test Condition                                                                                                                                     | Min. | Typ. | Max.       | Unit     |
|-----------------------|--------------------------------------------------|----------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------------|----------|
| V <sub>CC</sub>       | Operating supply voltage                         |                                                                                                                                                    | 10.5 |      | 45         | V        |
| V <sub>USD</sub>      | V <sub>CC</sub> under-voltage turn-off threshold |                                                                                                                                                    | 7    |      | 10.5       | V        |
| R <sub>ON</sub>       | On-state resistance                              | I <sub>OUT</sub> = 0.5A; T <sub>J</sub> = 25°C<br>I <sub>OUT</sub> = 0.5A; T <sub>J</sub> = 125°C                                                  |      | 150  | 185<br>280 | mΩ<br>mΩ |
| I <sub>S</sub>        | Supply current                                   | OFF-state<br>V <sub>CC</sub> = 24 V; T <sub>CASE</sub> = 25 °C<br>ON-state (all channels ON)<br>V <sub>CC</sub> = 24 V; T <sub>CASE</sub> = 100 °C |      |      | 150<br>12  | μA<br>mA |
| I <sub>LGND</sub>     | Output current at turn-off                       | V <sub>CC</sub> = V <sub>STAT</sub> = V <sub>IN</sub> = V <sub>GND</sub> = 24 V;<br>V <sub>OUT</sub> = 0 V                                         |      |      | 1          | mA       |
| I <sub>L(OFF)</sub>   | OFF-state output current                         | V <sub>IN</sub> = V <sub>OUT</sub> = 0 V                                                                                                           | 0    |      | 5          | μA       |
| V <sub>OUT(OFF)</sub> | OFF-state output voltage                         | V <sub>IN</sub> = 0 V; I <sub>OUT</sub> = 0 A                                                                                                      |      |      | 3          | V        |
| t <sub>d(VCCON)</sub> | Power-on delay time from VCC rising edge         | See Figure 7                                                                                                                                       |      | 1    |            | ms       |

**Table 4. Switching (VCC = 24V)**

| Symbol                                 | Parameter              | Test Condition                                                                                     | Min. | Typ. | Max. | Unit |
|----------------------------------------|------------------------|----------------------------------------------------------------------------------------------------|------|------|------|------|
| t <sub>ON</sub>                        | Turn-ON time           | R <sub>L</sub> = 48 Ω from 80% V <sub>OUT</sub><br>(see Figure 6)                                  |      | 50   | 100  | μs   |
| t <sub>OFF</sub>                       | Turn-OFF time          | R <sub>L</sub> = 48 Ω to 10% V <sub>OUT</sub><br>(see Figure 6)                                    |      | 75   | 150  | μs   |
| dV <sub>OUT</sub> /dt <sub>(ON)</sub>  | Turn-ON voltage slope  | R <sub>L</sub> = 48 Ω from V <sub>OUT</sub> = 2.4 V to V <sub>OUT</sub> = 19.2 V<br>(see Figure 6) |      | 0.7  |      | V/μs |
| dV <sub>OUT</sub> /dt <sub>(OFF)</sub> | Turn-OFF voltage slope | R <sub>L</sub> = 48 Ω from V <sub>OUT</sub> = 21.6 V to V <sub>OUT</sub> = 2.4 V<br>(see Figure 6) |      | 1.5  |      | V/μs |

**Table 5. Input pins**

| Symbol           | Parameter                | Test Condition                            | Min.                  | Typ. | Max.                  | Unit |
|------------------|--------------------------|-------------------------------------------|-----------------------|------|-----------------------|------|
| V <sub>INL</sub> | Input low level          |                                           |                       |      | V <sub>CC</sub> /2 -1 | V    |
| I <sub>INL</sub> | Low level input current  | V <sub>IN</sub> = V <sub>CC</sub> /2 -1 V | 80                    |      | 650                   | μA   |
| V <sub>INH</sub> | Input high level         |                                           | V <sub>CC</sub> /2 +1 |      |                       | V    |
| I <sub>INH</sub> | High level input current | V <sub>IN</sub> = V <sub>CC</sub> /2 +1 V |                       | 150  | 260                   | μA   |

| Symbol         | Parameter                | Test Condition                  | Min. | Typ. | Max. | Unit          |
|----------------|--------------------------|---------------------------------|------|------|------|---------------|
| $V_{IN(HYST)}$ | Input hysteresis voltage |                                 |      | 0.6  |      | V             |
| $I_{INL}$      | Low level input current  | $V_{IN} = V_{CC} = 32\text{ V}$ |      |      | 300  | $\mu\text{A}$ |

**Table 6. Protections**

| Symbol      | Parameter                                       | Test Condition                                       | Min.               | Typ.        | Max.        | Unit               |
|-------------|-------------------------------------------------|------------------------------------------------------|--------------------|-------------|-------------|--------------------|
| $T_{CSD}$   | Case shut-down temperature                      |                                                      | 125                | 130         | 135         | $^{\circ}\text{C}$ |
| $T_{CR}$    | Case reset temperature                          |                                                      | 110                |             |             | $^{\circ}\text{C}$ |
| $T_{CHYST}$ | Case thermal hysteresis                         |                                                      | 7                  | 15          |             | $^{\circ}\text{C}$ |
| $T_{JSD}$   | Junction shutdown temperature                   |                                                      | 150                | 175         | 200         | $^{\circ}\text{C}$ |
| $T_R$       | Junction reset temperature                      |                                                      | 135                |             |             | $^{\circ}\text{C}$ |
| $T_{HYST}$  | Junction thermal hysteresis                     |                                                      | 7                  | 15          |             | $^{\circ}\text{C}$ |
| $I_{PEAK}$  | Maximum DC output current before limitation     | $V_{CC} = 24\text{ V}; R_{LOAD} = 10\text{ m}\Omega$ | 1.1                |             | 2.6         | A                  |
| $I_{LIM}$   | DC short circuit current limitation per channel | $V_{CC} = 24\text{ V}; R_{LOAD} = 10\text{ m}\Omega$ | 0.7 <sup>(1)</sup> |             | 1.7         | A                  |
|             |                                                 |                                                      | 1 <sup>(2)</sup>   |             |             |                    |
| $V_{DEMAG}$ | Turn-OFF output clamp voltage                   | $I_{OUT} = 0.5\text{ A}; L = 6\text{ mH}$            | $V_{CC}-57$        | $V_{CC}-52$ | $V_{CC}-47$ | V                  |

1. VN808-E

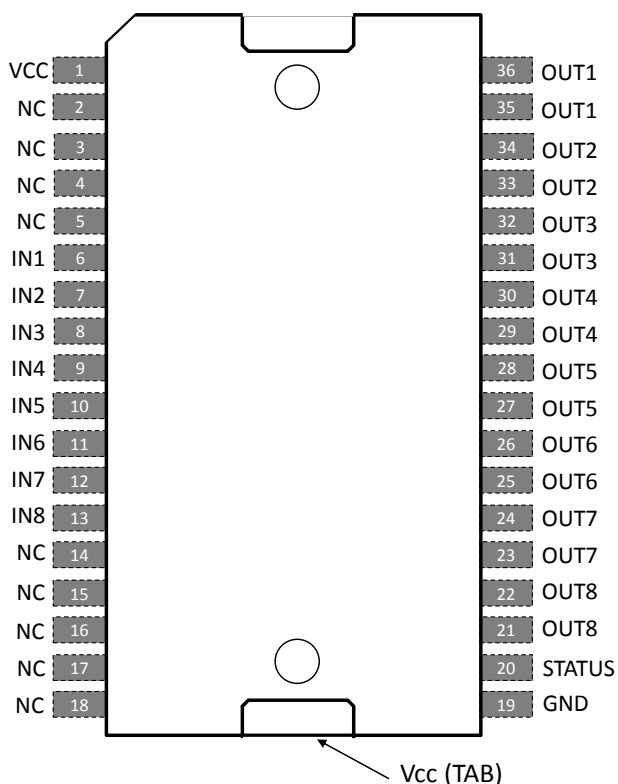
2. VN808-32-E

**Table 7. Status Pin**

| Symbol       | Parameter                     | Test Condition                                                                      | Min. | Typ. | Max. | Unit          |
|--------------|-------------------------------|-------------------------------------------------------------------------------------|------|------|------|---------------|
| $I_{HSTAT}$  | STATUS pin high level current | $V_{CC} = 18\text{ to }32\text{ V}; R_{STAT}=1\text{ k}\Omega$<br>(Fault condition) | 2    | 3    | 4    | mA            |
| $I_{LSTAT}$  | STATUS pin leakage current    | Normal operation; $V_{CC} = 32\text{ V}$                                            |      |      | 0.1  | $\mu\text{A}$ |
| $V_{CLSTAT}$ | STATUS pin clamp voltage      | $I_{STAT} = 1\text{ mA}$                                                            | 6.0  | 6.8  | 8.0  | V             |
|              |                               | $I_{STAT} = -1\text{ mA}$                                                           |      | -0.7 |      |               |

### 3 Pin connections

**Figure 2. Connection diagram (top view)**



**Table 8. Pin functions**

| Pin | Symbol | Description                                                                              |
|-----|--------|------------------------------------------------------------------------------------------|
| 1   | VCC    | Positive power supply voltage                                                            |
| 6   | IN1    | Channel 1 input                                                                          |
| 7   | IN2    | Channel 2 input                                                                          |
| 8   | IN3    | Channel 3 input                                                                          |
| 9   | IN4    | Channel 4 input                                                                          |
| 10  | IN5    | Channel 5 input                                                                          |
| 11  | IN6    | Channel 6 input                                                                          |
| 12  | IN7    | Channel 7 input                                                                          |
| 13  | IN8    | Channel 8 input                                                                          |
| 19  | GND    | Output power ground                                                                      |
| 20  | STATUS | Common open source diagnostic for over-temperature                                       |
| 21  | OUT8   | Channel 8 power stage output;<br>short the pins on the same net of the application board |
| 22  |        |                                                                                          |
| 23  | OUT7   | Channel 7 power stage output;<br>short the pins on the same net of the application board |
| 24  |        |                                                                                          |

| Pin              | Symbol | Description                                                                              |
|------------------|--------|------------------------------------------------------------------------------------------|
| 25               | OUT6   | Channel 6 power stage output;<br>short the pins on the same net of the application board |
| 26               |        |                                                                                          |
| 27               | OUT5   | Channel 5 power stage output;<br>short the pins on the same net of the application board |
| 28               |        |                                                                                          |
| 29               | OUT4   | Channel 4 power stage output;<br>short the pins on the same net of the application board |
| 30               |        |                                                                                          |
| 31               | OUT3   | Channel 3 power stage output;<br>short the pins on the same net of the application board |
| 32               |        |                                                                                          |
| 33               | OUT2   | Channel 2 power stage output;<br>short the pins on the same net of the application board |
| 34               |        |                                                                                          |
| 35               | OUT1   | Channel 1 power stage output;<br>short the pins on the same net of the application board |
| 36               |        |                                                                                          |
| TAB              | VCC    | Exposed tab internally connected to Vcc, positive power supply voltage                   |
| 2 to 5; 14 to 18 | N.C.   | Internally not connected;<br>if necessary, these pins can be routed in the application   |

## 4 Current, voltage conventions and internal diagram

Figure 3. Current and voltage conventions

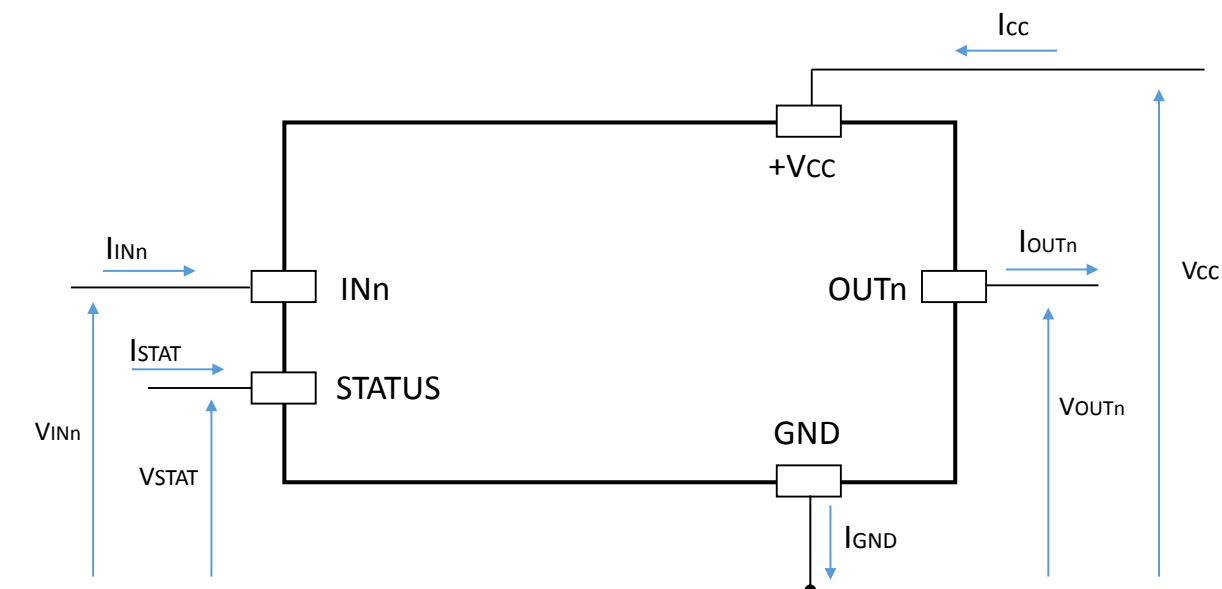
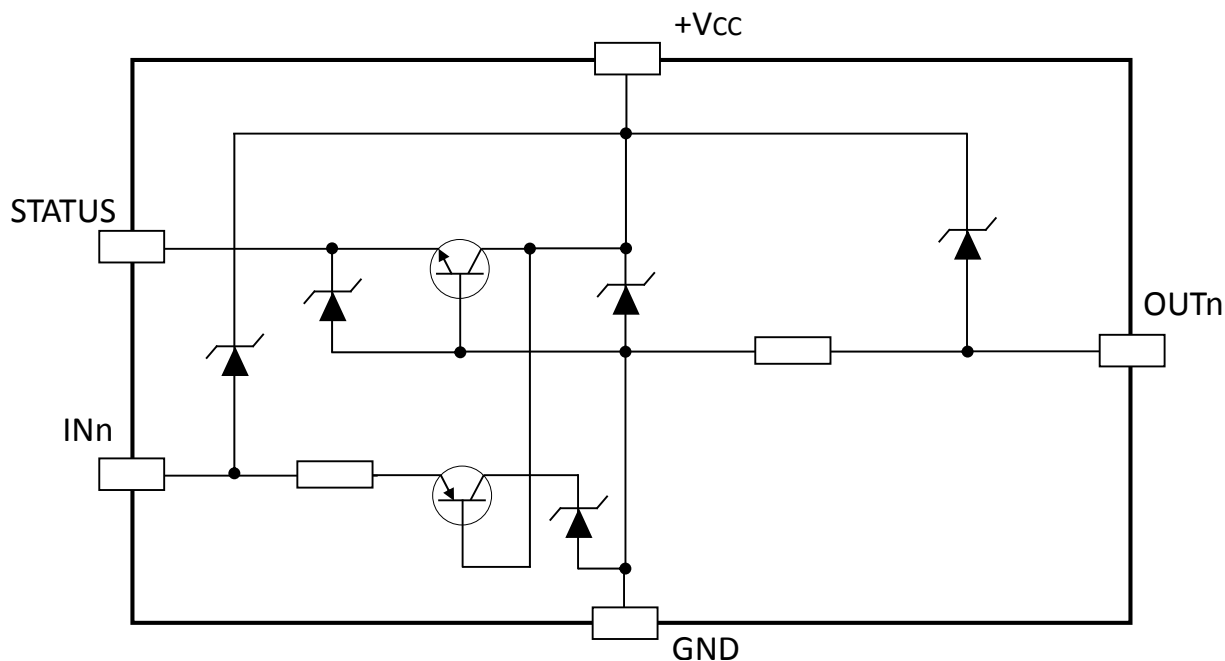
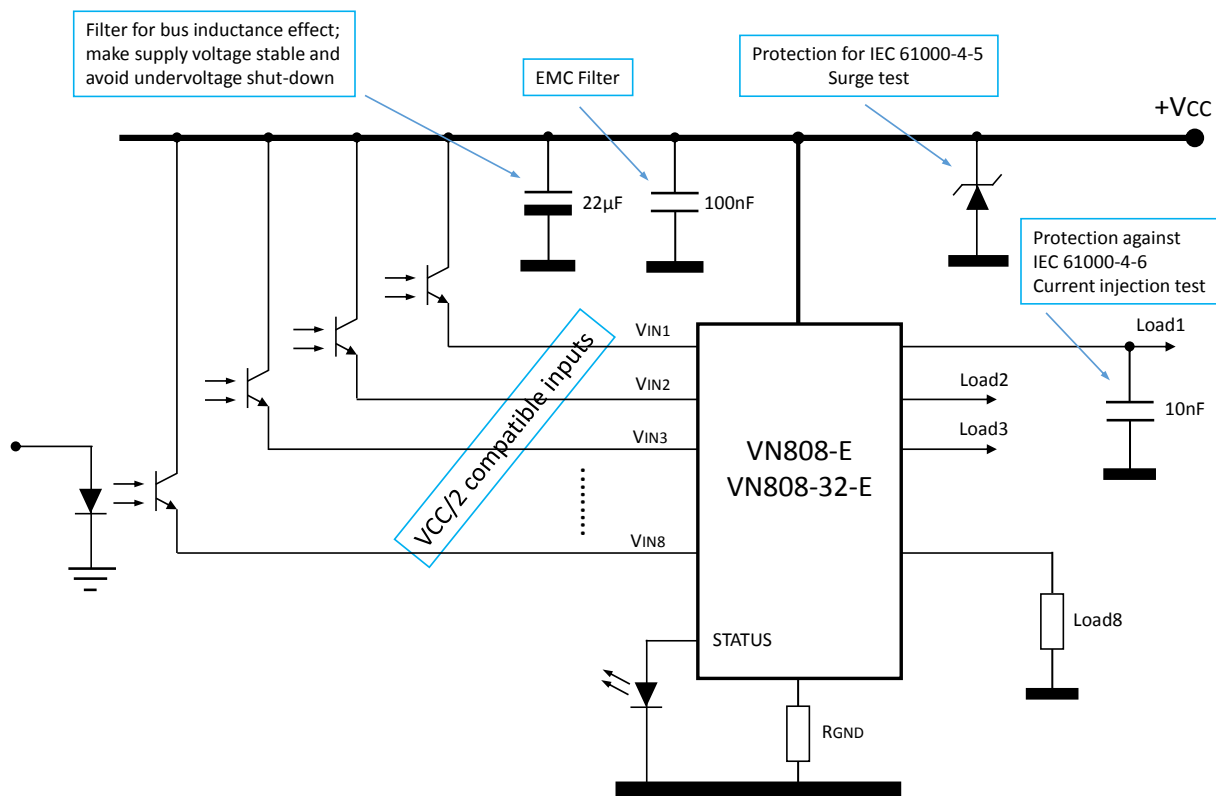


Figure 4. Equivalent internal block diagram (same structure for all channels)



**Figure 5. Application example**



**Table 9. Truth table**

| Conditions                                                                      | INPUTn | OUTPUTn | STATUS |
|---------------------------------------------------------------------------------|--------|---------|--------|
| Normal operation                                                                | L      | L       | L      |
|                                                                                 | H      | H       | L      |
| Current limitation                                                              | L      | L       | L      |
|                                                                                 | H      | X       | L      |
| Over-temperature (see <a href="#">Figure 12</a> and <a href="#">Figure 13</a> ) | L      | L       | L      |
|                                                                                 | H      | L       | H      |
| Undervoltage                                                                    | L      | L       | X      |
|                                                                                 | H      | L       | X      |



## 5 Switching time waveforms

Figure 6. Turn-ON and turn-OFF

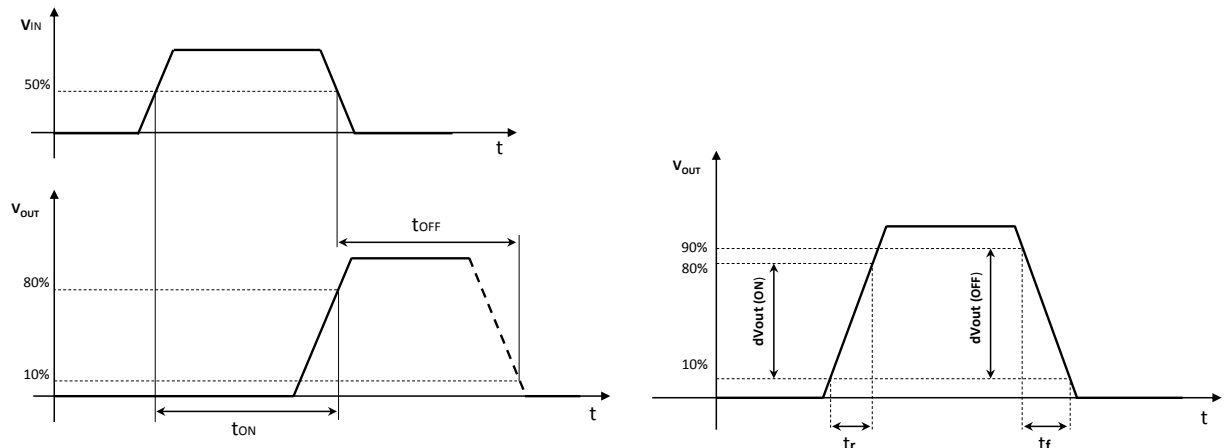
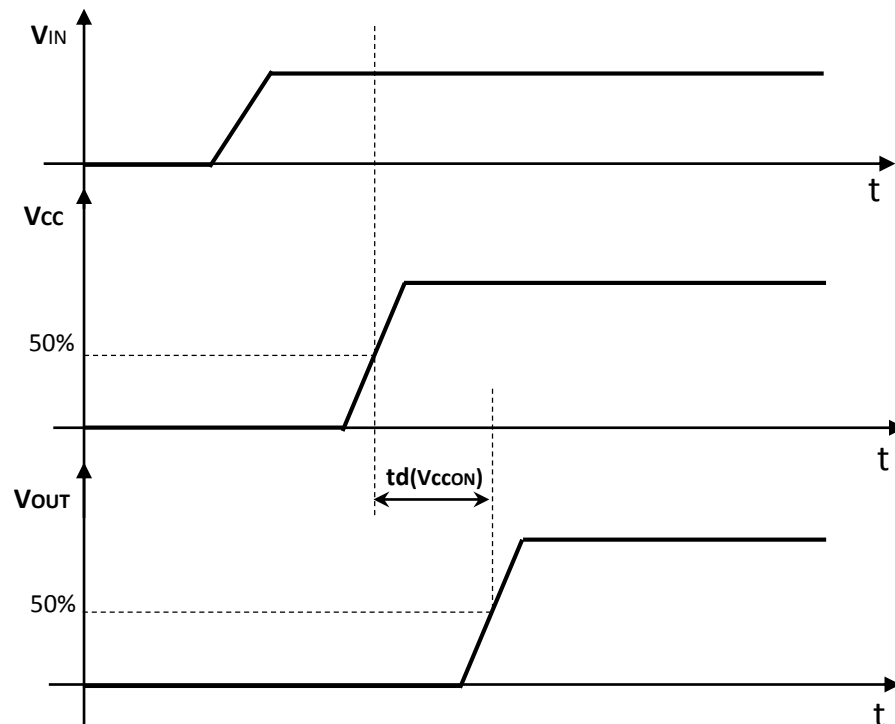


Figure 7.  $V_{CC}$  turn-ON



## 6 Power Section

### 6.1 Current limitation

Current limitation process is activated when the current sense connected on output stage measures a current value higher than a fixed threshold.

When this condition is verified, the gate voltage is modulated to prevent the output current from rising above to the limitation value.

Figure 8. Switching on resistive and on bulb lamp load

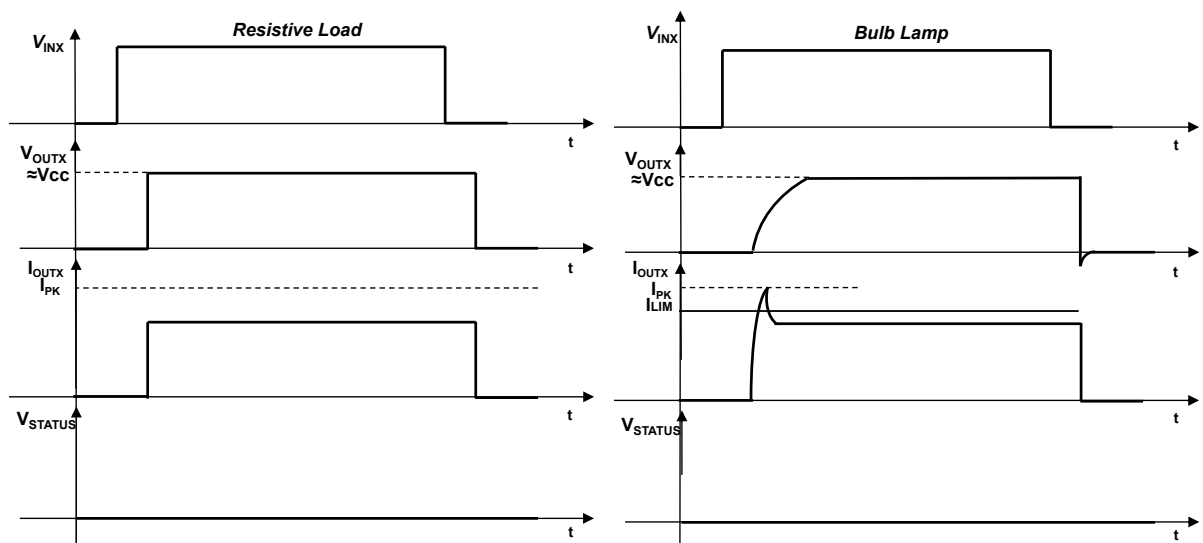
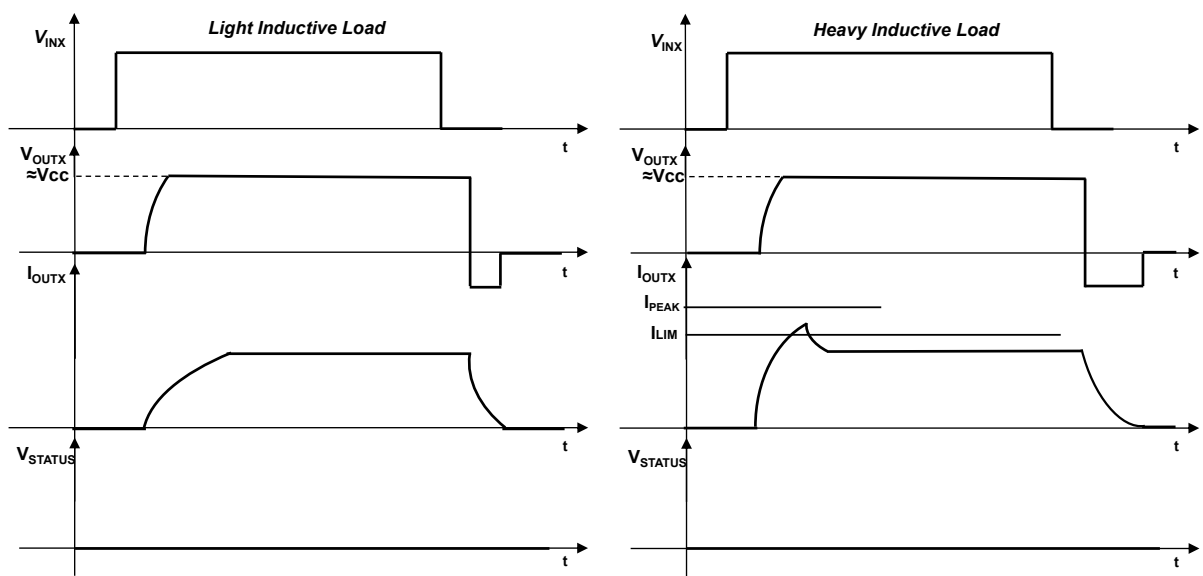
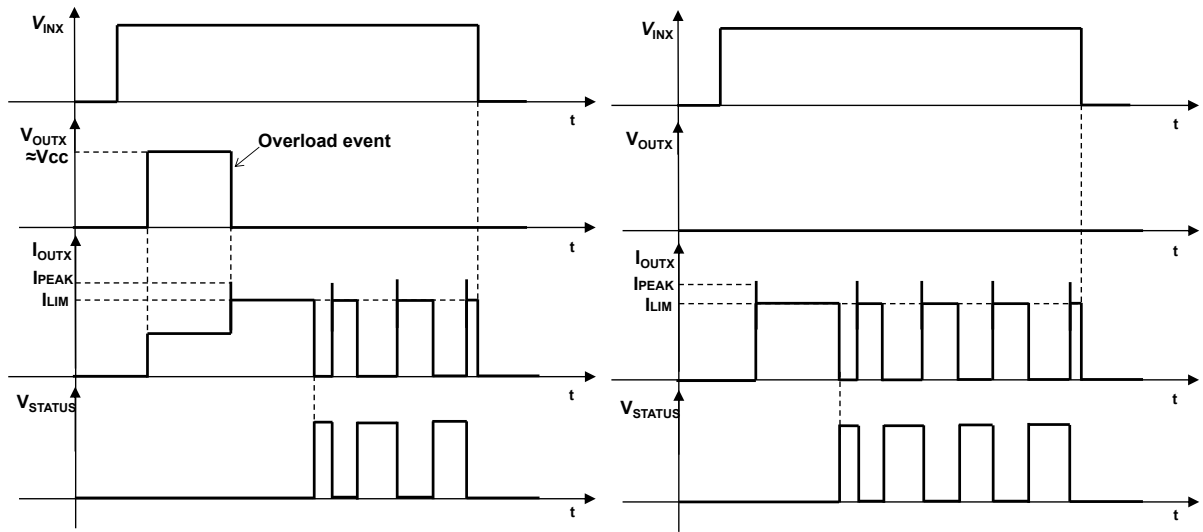


Figure 9. Switching on light and heavy inductive load



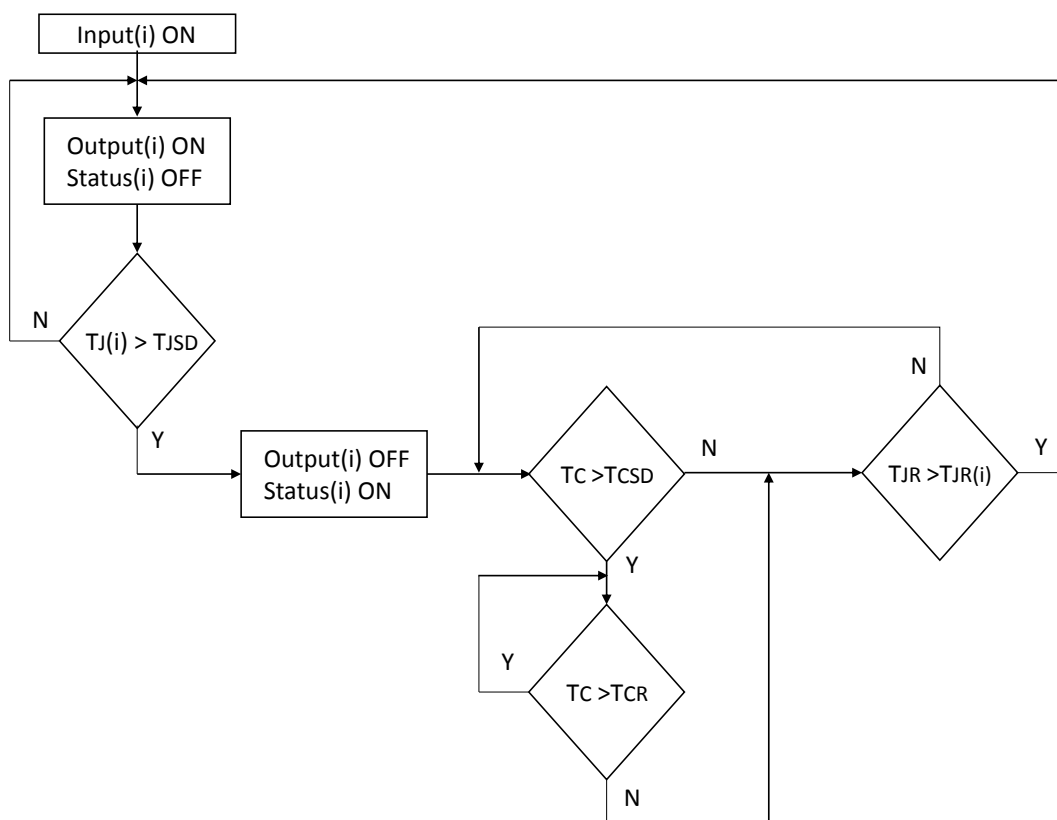
**Figure 10. Short circuit during ON-state and Turn on in short circuit**


## 6.2 Thermal protection

The device is protected against overheating due to overload conditions. During driving period, if the output is overloaded, the device suffers two different thermal stresses, the first one related to the junction, and the second related to the case.

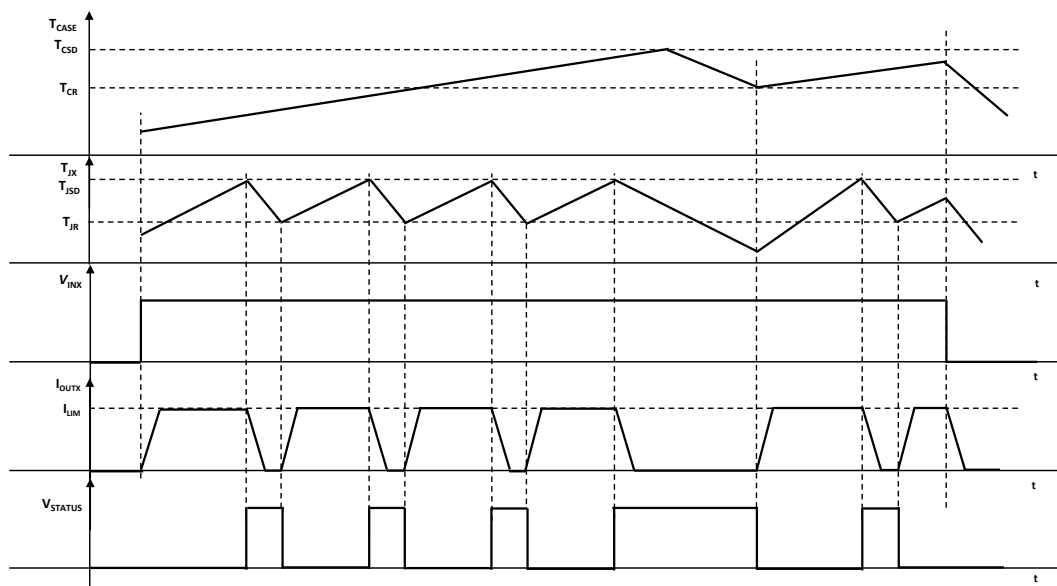
The two faults have different trigger thresholds: the junction protection threshold ( $T_{JSD}$ ) is higher than the case protection one ( $T_{CSD}$ ); generally the first protection that is activated in thermal stress conditions is the junction thermal shut-down. The output is turned-off when the temperature is higher than the related threshold and turned back on when it goes below the reset threshold ( $T_{JR}$ ). This behavior continues until the fault on the output is present.

If the thermal protection is active and the temperature of the package increases over the fixed case protection threshold, the case protection will be activated and the output is switched-off and back on when the junction temperature, of each channel in fault and case temperature, are below the respective reset thresholds.

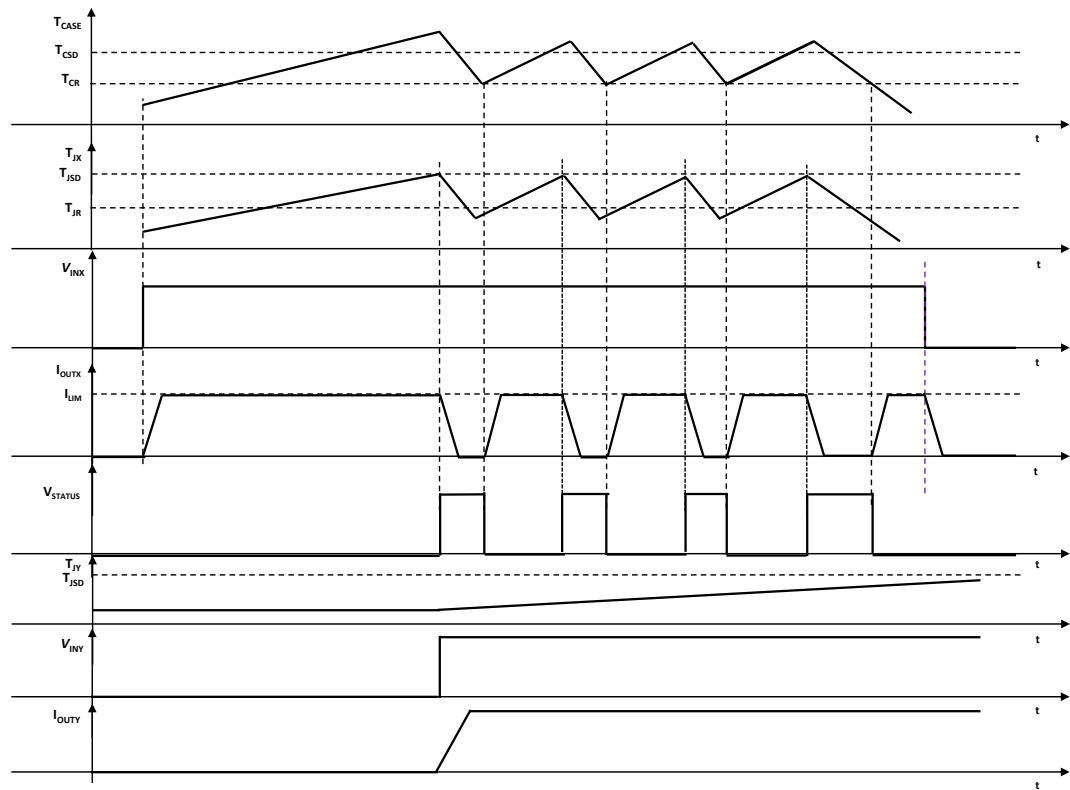
**Figure 11. Thermal protection flowchart**


### 6.3 Status indication

The Status pin is an active high common open source output indicating fault conditions. This pin is activated in case of junction over-temperature ( $T_{JX} > T_{JSD}$ ) of one or more output channels. [Figure 12](#) and [Figure 13](#) show the Status behavior when  $T_{JSD}$  is triggered before  $T_{CSD}$  and when  $T_{CSD}$  is triggered before  $T_{JSD}$  respectively.

**Figure 12. Thermal Protection and STATUS Behavior ( $T_{JSD}$  triggered before  $T_{CSD}$ )**


**Figure 13. Thermal Protection and STATUS Behavior ( $T_{CSD}$  triggered before  $T_{JSD}$ )**



## 7 Reverse polarity protection

Reverse polarity protection can be implemented on board using two different solutions:1.

1. Placing a resistor (R<sub>GND</sub>) between IC GND pin and load GND
2. Placing a diode between IC GND pin and load GND

If option 1 is selected, the minimum resistance value has to be selected according to the following equation:

$$R_{GND} \geq V_{CC}/I_{GND}$$

where I<sub>GND</sub> is the DC reverse ground pin current and can be found in [Section 1 Maximum ratings](#) of this datasheet.

Power dissipated by R<sub>GND</sub> (when V<sub>CC</sub> < 0: during reverse polarity situations) is:

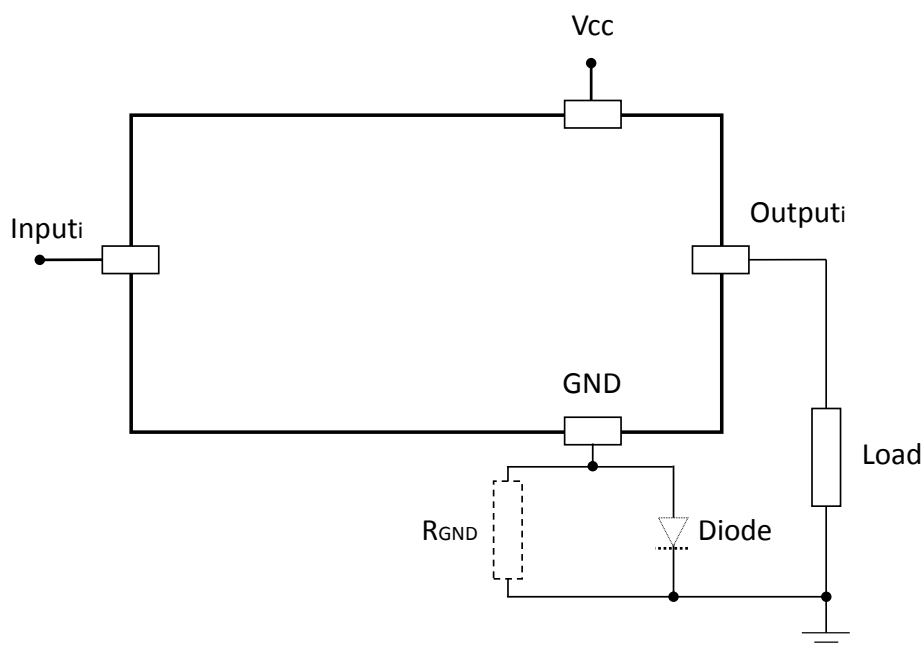
$$P_D = (V_{CC})^2/R_{GND}$$

If option 2 is selected, the diode has to be chosen by taking into account VRRM > |V<sub>cc</sub>| and its power dissipation capability:

$$P_D \geq I_S \cdot V_f$$

**Note:** *In normal operation (no reverse polarity), there is a voltage drop (ΔV) between GND of the device and GND of the system. Using option 1, ΔV = R<sub>GND</sub> \* I<sub>cc</sub>. Using option 2, ΔV = V<sub>F</sub>@(I<sub>F</sub>).*

**Figure 14. V<sub>CC</sub> Reverse Polarity Protection**

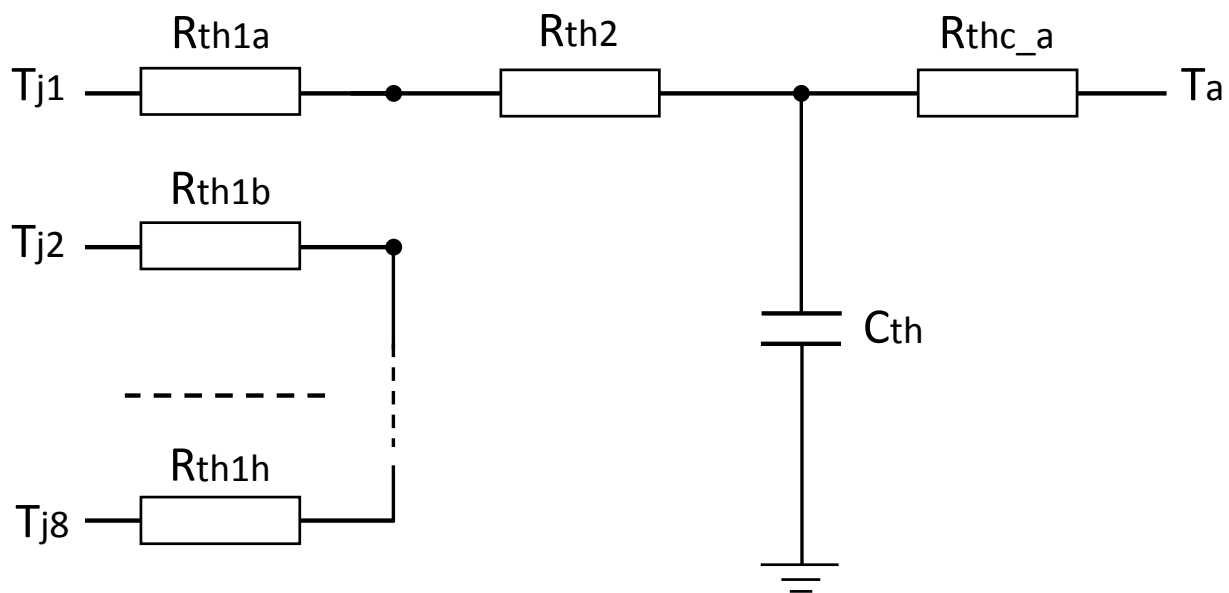


This schematic can be used with any type of load.

## 8 Thermal information

### 8.1 Thermal impedance

Figure 15. Simplified thermal model of the process stage

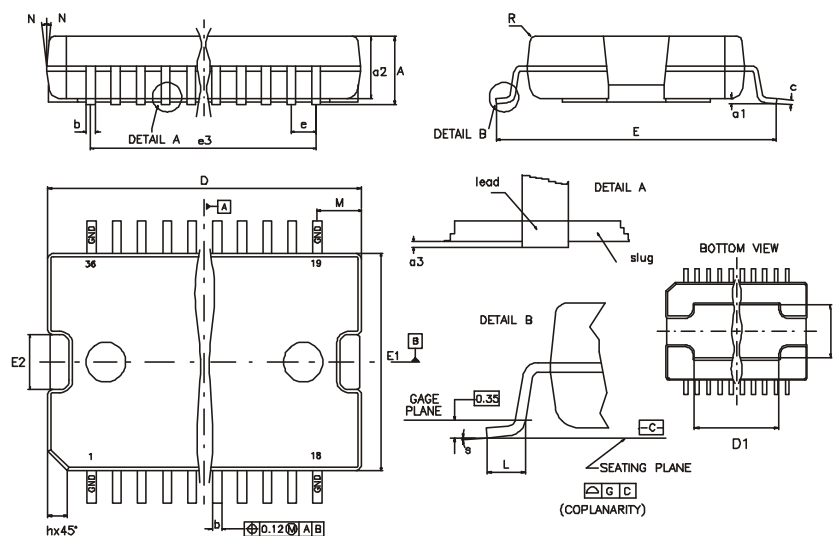


## 9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com)

ECOPACK is an ST trademark.

**Figure 16. PowerSO-36 package outline**



**Table 10. PowerSO-36 mechanical data**

| Dim               | mm    |       |       |
|-------------------|-------|-------|-------|
|                   | Min.  | Typ.  | Max.  |
| A                 |       |       | 3.60  |
| a1                | 0.10  |       | 0.30  |
| a2                |       |       | 3.30  |
| a3                | 0     |       | 0.10  |
| b                 | 0.22  |       | 0.38  |
| c                 | 0.23  |       | 0.32  |
| D <sup>(1)</sup>  | 15.80 |       | 16.00 |
| D1                | 9.40  |       | 9.80  |
| E                 | 13.90 |       | 14.50 |
| E1 <sup>(1)</sup> | 10.90 |       | 11.10 |
| E2                |       |       | 2.90  |
| E3                | 5.80  |       | 6.20  |
| e                 |       | 0.65  |       |
| e3                |       | 11.05 |       |
| G                 | 0     |       | 0.10  |
| H                 | 15.50 |       | 15.90 |
| h                 |       |       | 1.10  |



| Dim | mm   |      |      |
|-----|------|------|------|
|     | Min. | Typ. | Max. |
| L   | 0.80 |      | 1.10 |
| N   |      |      | 10°  |
| S   | 0°   |      | 8°   |

1. D and E1" do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm (0.006"). Critical dimensions are "a3", "E" and "G".

## 9.1 Footprint recommended data

Figure 17. Footprint recommended data

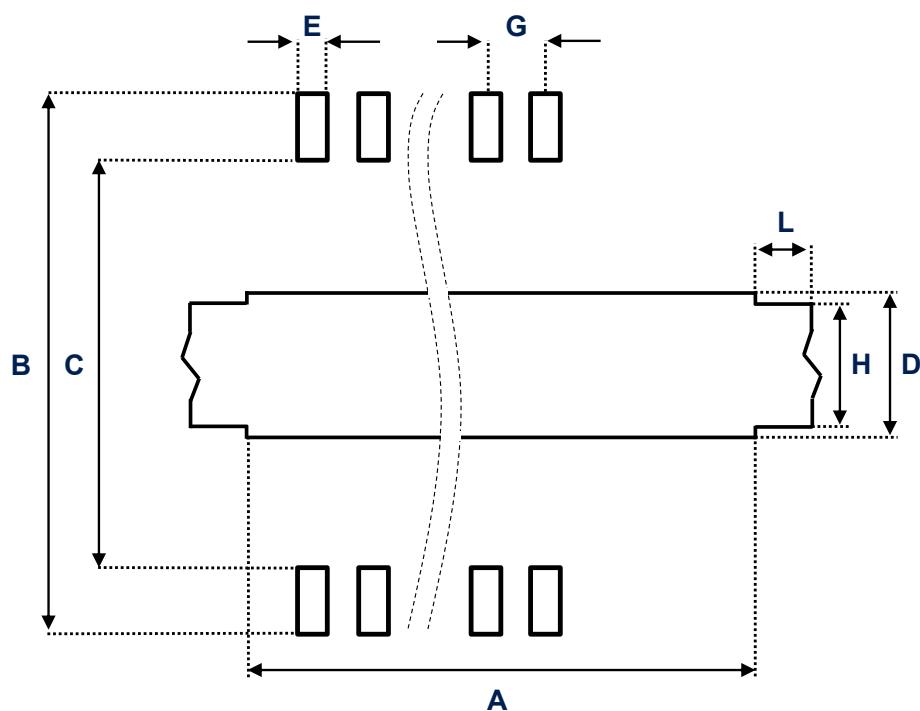


Table 11. Footprint data

| Dim. | mm        |
|------|-----------|
| A    | 9.5       |
| B    | 14.7-15.0 |
| C    | 12.5-12.7 |
| D    | 6.3       |
| E    | 0.42      |
| G    | 0.65      |
| H    | 4.1       |
| L    | 3.2       |

## 9.2 Tube shipment information

Figure 18. Tube shipment information

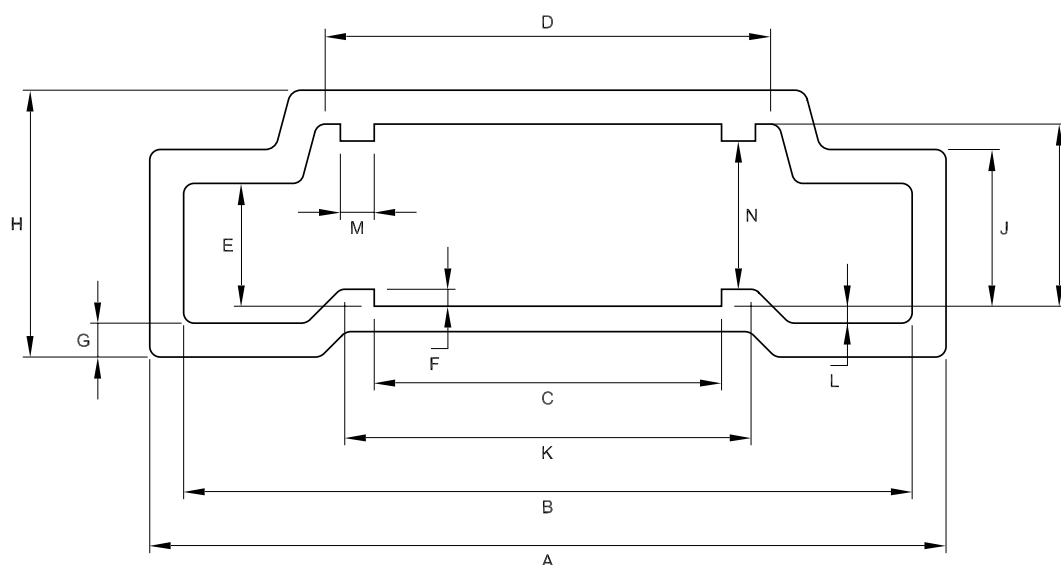


Table 12. Tube mechanical data

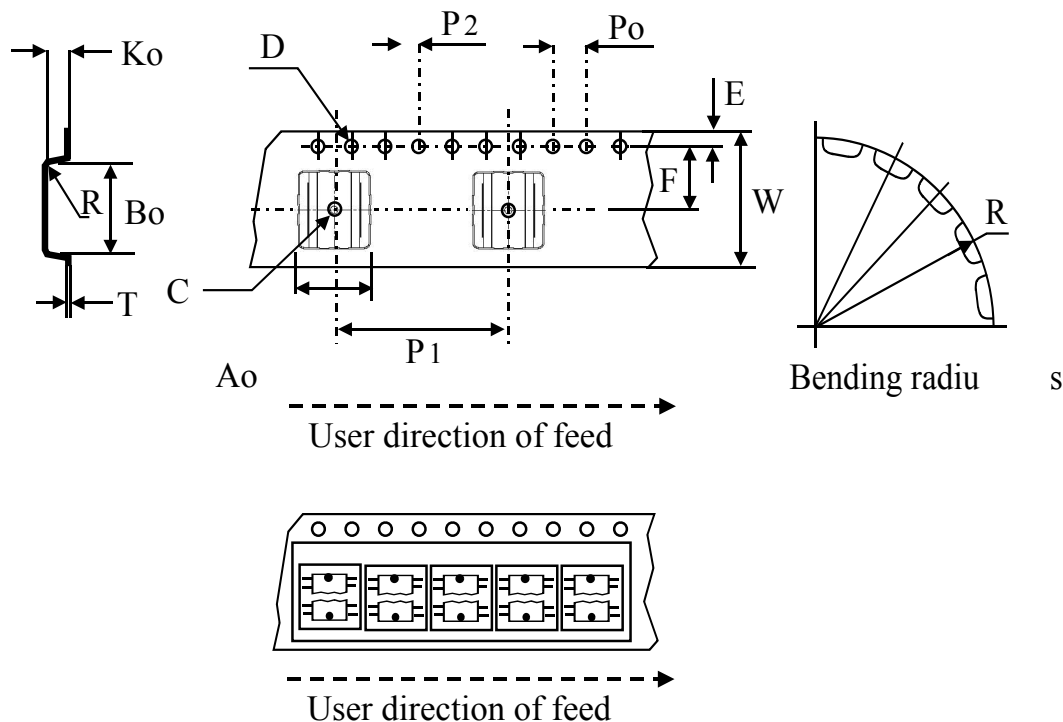
| Dim. | mm              |
|------|-----------------|
| A    | 18.80           |
| B    | 17.2 $\pm$ 0.2  |
| C    | 8.20 $\pm$ 0.2  |
| D    | 10.90 $\pm$ 0.2 |
| E    | 2.90 $\pm$ 0.2  |
| F    | 0.40            |
| G    | 0.80            |
| H    | 6.30            |
| I    | 4.30 $\pm$ 0.2  |
| J    | 3.7 $\pm$ 0.2   |
| K    | 9.4             |
| L    | 0.40            |
| M    | 0.80            |
| N    | 3.50 $\pm$ 0.2  |

Base quantity 310 pcs

Bulk quantity 310 pcs

### 9.3 Tape and reel shipment information

**Figure 19. Tape specifications**



**Table 13. Tape mechanical data**

| Dim.       | mm                    |
|------------|-----------------------|
| D          | 1.50 +0.1/0           |
| E          | 1.75 ±0.1             |
| Po         | 4.00 ±0.1             |
| T max.     | 0.40                  |
| D1 min.    | 1.50                  |
| F          | 11.5 ±0.05            |
| K max.     | 6.50                  |
| P2         | 2.00 ±0.1             |
| R          | 50                    |
| W          | 24.00 ±0.30           |
| P1         | 24.00                 |
| Ao, Bo, Ko | 0.05 min. to 1.0 max. |

Base quantity 600 pcs

Bulk quantity 600 pcs

Figure 20. Reel specifications

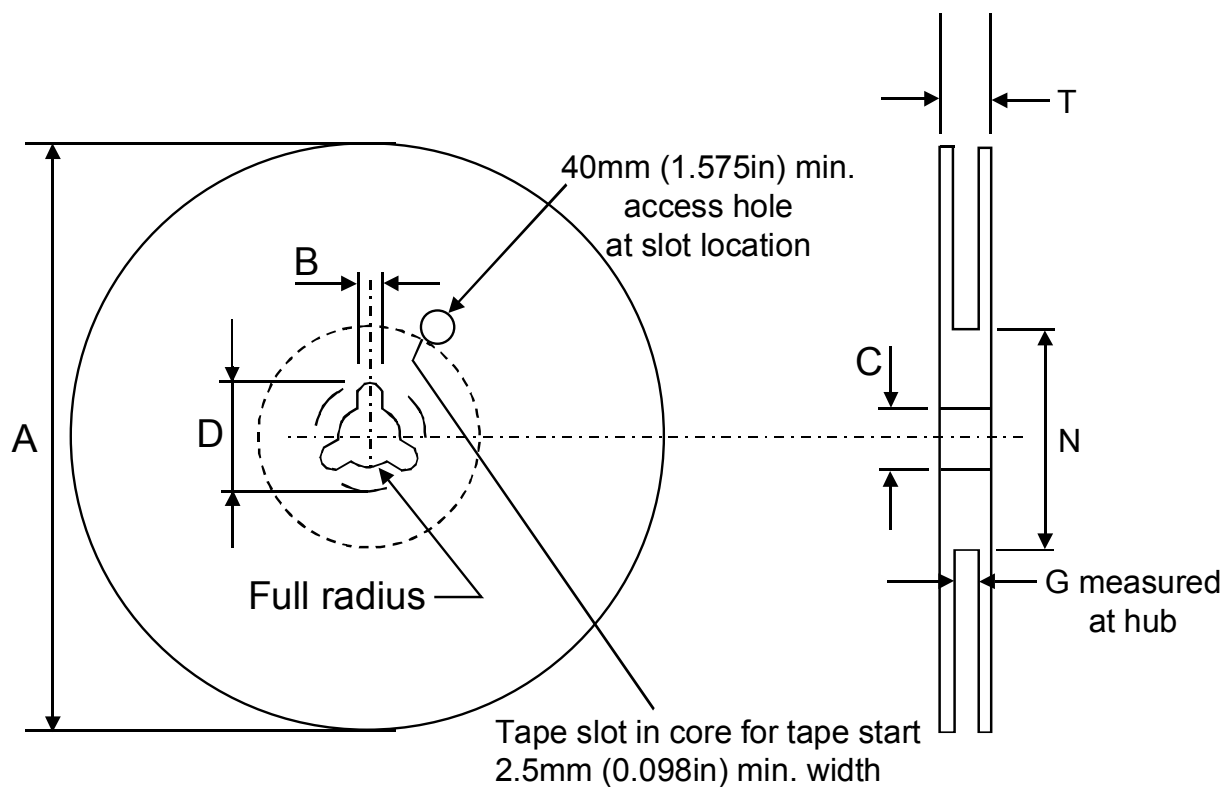


Table 14. Reel mechanical data

| Dim.      | mm         |
|-----------|------------|
| Tape size | 24.0 ±0.30 |
| A max.    | 330.0      |
| B min.    | 1.5        |
| C         | 13.0 ±0.20 |
| D min.    | 20.2       |
| N min.    | 60         |
| G         | 24.4 +2/-0 |
| T max.    | 30.4       |

## 10 Ordering information

Table 15. Ordering information

| Part number  | Package    | Packaging     |
|--------------|------------|---------------|
| VN808-E      | PowerSO-36 | Tube          |
| VN808TR-E    |            | Tape and reel |
| VN808-32-E   |            | Tube          |
| VN808TR-32-E |            | Tape and reel |

## Revision history

**Table 16. Document revision history**

| Date         | Version | Changes                                                                                                                                                                                                                                                                                                  |
|--------------|---------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| 13-Sep-2005  | 1       | Initial release.                                                                                                                                                                                                                                                                                         |
| 1-Mar-2007   | 2       | Document reformatted                                                                                                                                                                                                                                                                                     |
| 12-Mar-2007  | 3       | Typo in Figure 3.                                                                                                                                                                                                                                                                                        |
| 26-Mar-2007  | 4       | Typo note Table 2.                                                                                                                                                                                                                                                                                       |
| 07-Jul-2008  | 5       | Added: Section 6 on page 13                                                                                                                                                                                                                                                                              |
| 04-Aug-2008  | 6       | Added: Figure 12: Footprint recommended data on page 16                                                                                                                                                                                                                                                  |
| 25-Aug-2009  | 7       | Updated Section 6: Reverse polarity protection                                                                                                                                                                                                                                                           |
| 24-Feb-2010  | 8       | Updated Section 7: Package mechanical data                                                                                                                                                                                                                                                               |
| 08-Nov-2012  | 9       | Changed Figure 5.<br>Minor text changes to improve the readability.                                                                                                                                                                                                                                      |
| 19-Nov-2012  | 10      | Added maximum value to $I_{INL}$ parameter in Table 5.                                                                                                                                                                                                                                                   |
| 31-Jul-2013  | 11      | Updated Section 7.1: Footprint recommended data.                                                                                                                                                                                                                                                         |
| 18-Dec-2013  | 12      | Replaced LMAX parameter by EAS parameter in Table 1.<br>Added TJ condition to Table 3.<br>Updated Section 6.                                                                                                                                                                                             |
| 09- Jun-2020 | 13      | Include VN808-32-E ; Updated Table 6, Table 8; Updated notes in Section 7 ;<br>Added Section 6 Power Section, Section 6.1 Current limitation,<br>Section 6.2 Thermal protection, Section 6.2 Thermal protection,<br>Section 8 Thermal information, Section 8.1 Thermal impedance; minor<br>text update . |
| 08-May-2023  | 14      | Changed and merged Figure 8, Figure 9, Figure 10;<br>Changed $-I_{OUT}$ and $P_{TOT}$ values in Table 1;<br>Changed $R_{th(JA)}$ in Table 2;<br>Changed pins description in Table 8.                                                                                                                     |

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