

# LM148, LM248, LM348 QUADRUPLE OPERATIONAL AMPLIFIERS

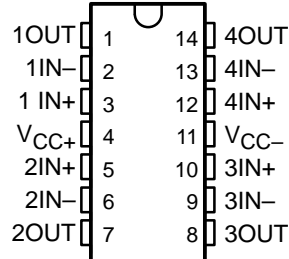
SLOS058C – OCTOBER 1979 – REVISED DECEMBER 2002

- $\mu$ A741 Operating Characteristics
- Low Supply-Current Drain . . . 0.6 mA Typ (per amplifier)
- Low Input Offset Voltage
- Low Input Offset Current
- Class AB Output Stage
- Input/Output Overload Protection
- Designed to Be Interchangeable With Industry Standard LM148, LM248, and LM348

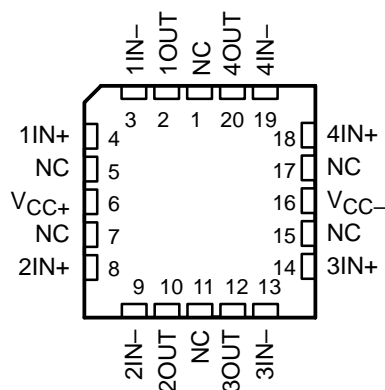
## description/ordering information

The LM148, LM248, and LM348 are quadruple, independent, high-gain, internally compensated operational amplifiers designed to have operating characteristics similar to the  $\mu$ A741. These amplifiers exhibit low supply-current drain and input bias and offset currents that are much less than those of the  $\mu$ A741.

LM148 . . . J PACKAGE  
LM248 . . . D OR N PACKAGE  
LM348 . . . D, N, OR NS PACKAGE  
(TOP VIEW)



LM148 . . . FK PACKAGE  
(TOP VIEW)



NC – No internal connection

## ORDERING INFORMATION

$T_A$	$V_{IOmax}$ AT 25°C	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	6 mV	PDIP (N)	Tube of 25	LM348N	LM348N
		SOIC (D)	Tube of 50	LM348D	LM348
			Reel of 2500	LM348DR	
		SOP (NS)	Reel of 2000	LM348NSR	LM348
–25°C to 85°C	6 mV	PDIP (N)	Tube of 25	LM248N	LM248N
		SOIC (D)	Tube of 50	LM248D	LM248
			Reel of 2500	LM248DR	
–55°C to 125°C	5 mV	CDIP (J)	Tube of 25	LM148J	LM148J
		LCCC (FK)	Tube of 50	LM148FK	LM148FK

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

**TEXAS  
INSTRUMENTS**

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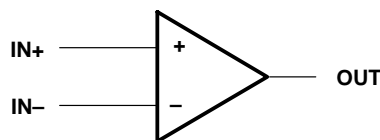
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# LM148, LM248, LM348

## QUADRUPLE OPERATIONAL AMPLIFIERS

SLOS058C – OCTOBER 1979 – REVISED DECEMBER 2002

### symbol (each amplifier)



### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage, $V_{CC+}$ (see Note 1):	LM148	22 V
	LM248, LM348	18 V
Supply voltage, $V_{CC-}$ (see Note 1):	LM148	-22 V
	LM248, LM348	-18 V
Differential input voltage, $V_{ID}$ (see Note 2):	LM148	44 V
	LM248, LM348	36 V
Input voltage, $V_I$ (either input, see Notes 1 and 3):	LM148	-22 V
	LM248, LM348	-18 V
Duration of output short circuit (see Note 4)		Unlimited
Operating virtual junction temperature, $T_J$		150°C
Package thermal impedance, $\theta_{JA}$ (see Notes 5 and 6):	D package	86°C/W
	N package	80°C/W
	NS package	76°C/W
Package thermal impedance, $\theta_{JC}$ (see Notes 7 and 8):	FK package	5.61°C/W
	J package	15.05°C/W
Case temperature for 60 seconds: FK package		260°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds: J package		300°C
Lead temperature 1,6 mm (1/16 inch) from case for 60 seconds: D, N, or NS package		260°C
Storage temperature range, $T_{stg}$		-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES:
1. All voltage values, unless otherwise noted, are with respect to the midpoint between  $V_{CC+}$  and  $V_{CC-}$ .
  2. Differential voltages are at  $IN+$  with respect to  $IN-$ .
  3. The magnitude of the input voltage must never exceed the magnitude of the supply voltage or the value specified in the table, whichever is less.
  4. The output may be shorted to ground or either power supply. Temperature and/or supply voltages must be limited to ensure that the dissipation rating is not exceeded.
  5. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JA}$ , and  $T_A$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_A)/\theta_{JA}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  6. The package thermal impedance is calculated in accordance with JESD 51-7.
  7. Maximum power dissipation is a function of  $T_J(max)$ ,  $\theta_{JC}$ , and  $T_C$ . The maximum allowable power dissipation at any allowable ambient temperature is  $P_D = (T_J(max) - T_C)/\theta_{JC}$ . Operating at the absolute maximum  $T_J$  of 150°C can affect reliability.
  8. The package thermal impedance is calculated in accordance with MIL-STD-883.

### recommended operating conditions

	MIN	MAX	UNIT
Supply voltage, $V_{CC+}$	4	18	V
Supply voltage, $V_{CC-}$	-4	-18	V



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electrical characteristics at specified free-air temperature,  $V_{CC\pm} = \pm 15$  V (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		LM148			LM248			LM348			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>IO</sub>	Input offset voltage	V <sub>O</sub> = 0	25°C	1		5	1		6	1		6	mV
			Full range			6	7.5		7.5				
I <sub>IO</sub>	Input offset current	V <sub>O</sub> = 0	25°C	4		25	4		50	4		50	nA
			Full range			75	125		100				
I <sub>IB</sub>	Input bias current	V <sub>O</sub> = 0	25°C	30		100	30		200	30		200	nA
			Full range			325	500		400				
V <sub>ICR</sub>	Common-mode input voltage range		Full range	±12			±12			±12		V	
V <sub>OM</sub>	Maximum peak output voltage swing	R <sub>L</sub> = 10 kΩ	25°C	±12		±13	±12		±13	±12		±13	V
		R <sub>L</sub> ≥ 10 kΩ	Full range	±12			±12			±12			
		R <sub>L</sub> = 2 kΩ	25°C	±10		±12	±10		±12	±10		±12	
		R <sub>L</sub> ≥ 2 kΩ	Full range	±10			±10			±10			
A <sub>VD</sub>	Large-signal differential voltage amplification	V <sub>O</sub> = ±10 V, R <sub>L</sub> = ≥ 2 kΩ	25°C	50		160	25		160	25		160	V/mV
			Full range	25			15			15			
r <sub>i</sub>	Input resistance‡		25°C	0.8	2.5			0.8	2.5			MΩ	
B <sub>1</sub>	Unity-gain bandwidth	A <sub>VD</sub> = 1	25°C	1			1			1		MHz	
φ <sub>m</sub>	Phase margin	A <sub>VD</sub> = 1	25°C	60°			60°			60°			
CMRR	Common-mode rejection ratio	V <sub>IC</sub> = V <sub>ICRmin</sub> , V <sub>O</sub> = 0	25°C	70		90	70		90	70		90	dB
			Full range	70			70			70			
k <sub>SVR</sub>	Supply-voltage rejection ratio (ΔV <sub>CC±</sub> /ΔV <sub>IO</sub> )	V <sub>CC±</sub> = ±9 V to ±15 V, V <sub>O</sub> = 0	25°C	77		96	77		96	77		96	dB
			Full range	77			77			77			
I <sub>OS</sub>	Short-circuit output current		25°C	±25			±25			±25		mA	
I <sub>CC</sub>	Supply current (four amplifiers)	No load	25°C				2.4		4.5	2.4		4.5	mA
		V <sub>O</sub> = V <sub>OM</sub>		2.4		3.6							
V <sub>O1</sub> /V <sub>O2</sub>	Crosstalk attenuation	f = 1 Hz to 20 kHz	25°C	120			120			120		dB	

† All characteristics are measured under open-loop conditions with zero common-mode input voltage, unless otherwise specified. Full range for  $T_A$  is  $-55^\circ\text{C}$  to  $125^\circ\text{C}$  for LM148,  $-25^\circ\text{C}$  to  $85^\circ\text{C}$  for LM248, and  $0^\circ\text{C}$  to  $70^\circ\text{C}$  for LM348.

‡ This parameter is not production tested.

# LM148, LM248, LM348

## QUADRUPLE OPERATIONAL AMPLIFIERS

SLOS058C – OCTOBER 1979 – REVISED FEBRUARY 2002

operating characteristics,  $V_{CC\pm} = \pm 15\text{ V}$ ,  $T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SR	Slew rate at unity gain	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , See Figure 1		0.5		V/ $\mu\text{s}$

### PARAMETER MEASUREMENT INFORMATION

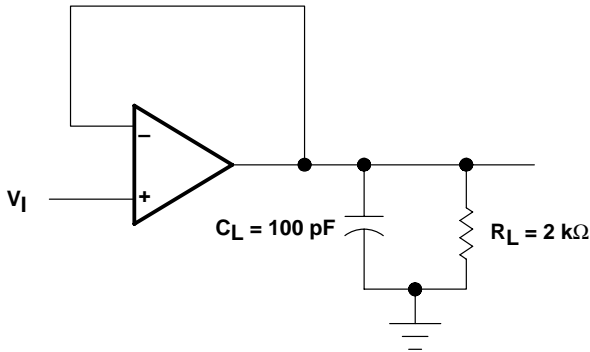


Figure 1. Unity-Gain Amplifier

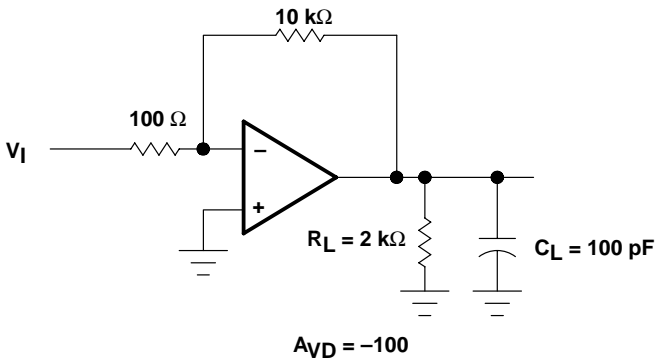


Figure 2. Inverting Amplifier

**PACKAGING INFORMATION**

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/Ball Finish	MSL Peak Temp <sup>(3)</sup>
LM148FKB	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
LM148J	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
LM148JB	ACTIVE	CDIP	J	14	1	TBD	A42 SNPB	N / A for Pkg Type
LM248D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM248DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM248DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM248DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM248N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
LM248NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
LM348D	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM348DE4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM348DG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM348DR	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM348DRE4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM348DRG4	ACTIVE	SOIC	D	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM348N	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
LM348NE4	ACTIVE	PDIP	N	14	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
LM348NSR	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
LM348NSRE4	ACTIVE	SO	NS	14	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

<sup>(1)</sup> The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

<sup>(2)</sup> Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS

compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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J (R-GDIP-T\*\*)

14 LEADS SHOWN

# CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



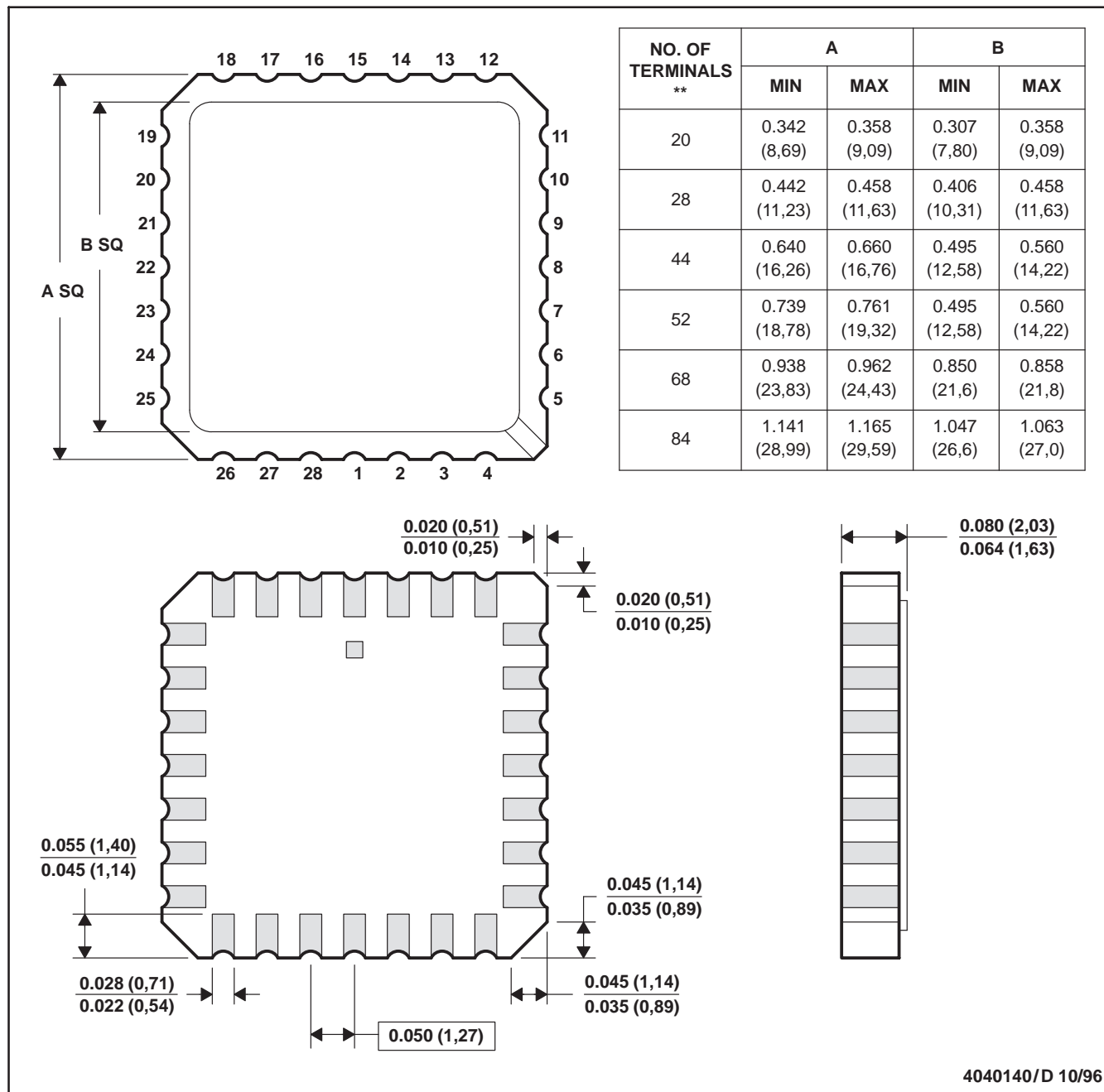
4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package is hermetically sealed with a ceramic lid using glass frit.
  - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
  - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

## FK (S-CQCC-N\*\*)

## LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. This package can be hermetically sealed with a metal lid.
  - D. The terminals are gold plated.
  - E. Falls within JEDEC MS-004



## N (R-PDIP-T\*\*)

16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD

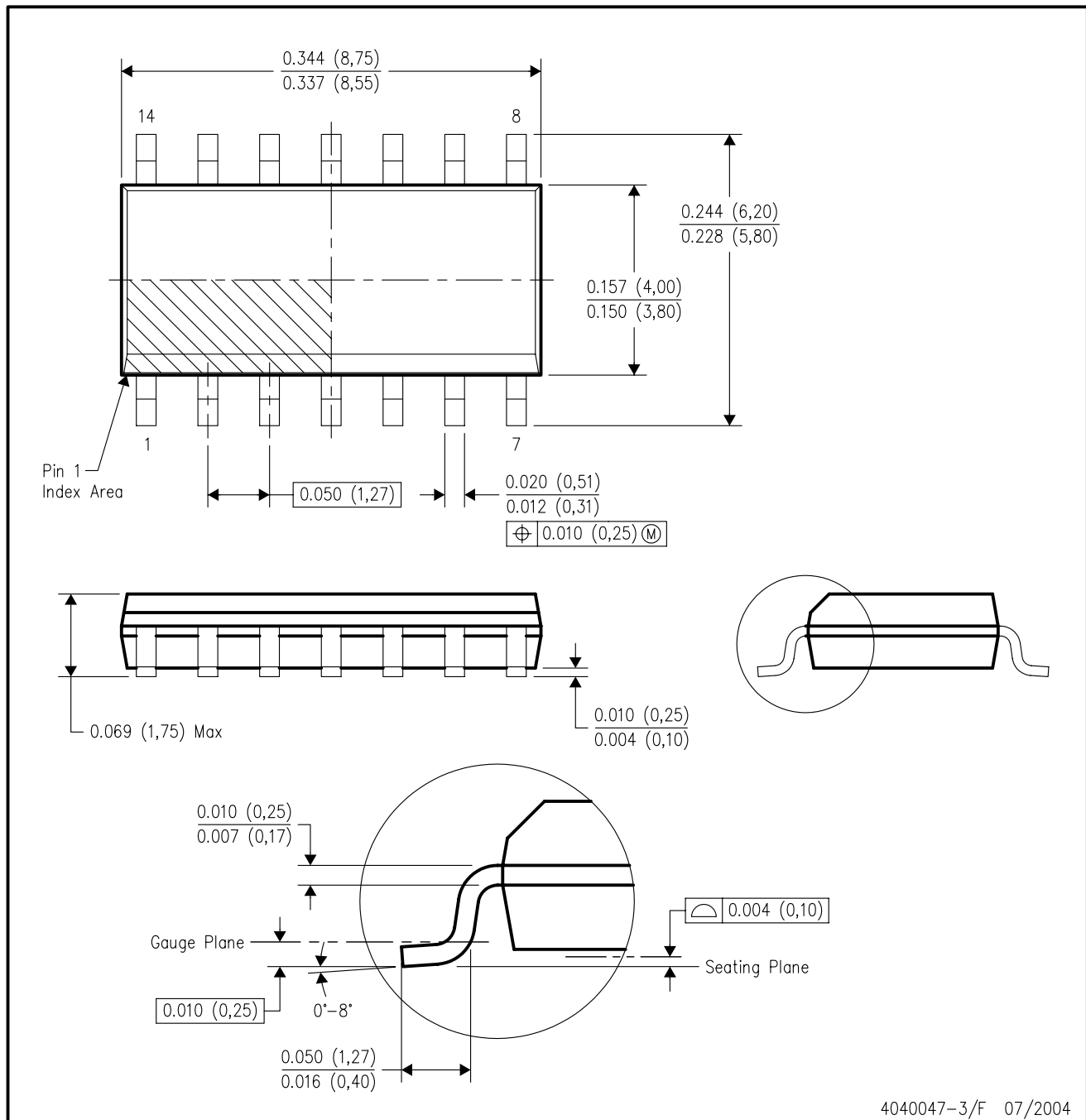


4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

## D (R-PDSO-G14)

## PLASTIC SMALL-OUTLINE PACKAGE



4040047-3/F 07/2004

# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



DIM \ PINS **	14	16	20	24
A MAX	10,50	10,50	12,90	15,30
A MIN	9,90	9,90	12,30	14,70

4040062/C 03/03

- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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