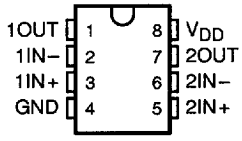
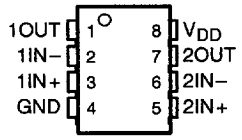
SLCS011 – MAY 1992

- **Wide Range of Supply Voltages 2 V to 8 V**
- **Fully Characterized at 3 V and 5 V**
- **Very-Low Supply-Current Drain 120 μA Typ at 3 V**
- **Output Compatible With TTL, MOS, and CMOS**
- **Fast Response Time . . . 200 ns Typ for TTL-Level Input Step**
- **High Input Impedance . . . 10^{12} Ω Typ**
- **Extremely Low Input Bias Current 5 pA Typ**
- **Common-Mode Input Voltage Range Includes Ground**
- **Built-In ESD Protection**

D OR P PACKAGE
(TOP VIEW)



PW PACKAGE
(TOP VIEW)

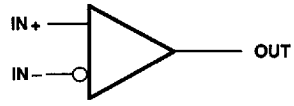


NC – No internal connection

description

The TLV2352 consists of two independent, low-power comparators specifically designed for single power-supply applications and to operate with power-supply rails as low as 2 V. When powered from a 3-V supply, the typical supply current is only 120 μA.

symbol (each comparator)



The TLV2352 is designed using the Texas Instruments LinCMOS™ technology and therefore features an extremely high input impedance (typically greater than 10^{12} Ω), which allows direct interfacing with high-impedance sources. The outputs are N-channel open-drain configurations that require an external pullup resistor to provide a positive output voltage swing, and they can be connected to achieve positive-logic wired-AND relationships. The TLV2352 is fully characterized at 3 V and 5 V for operation from – 40°C to 85°C.

The TLV2352 has internal electrostatic-discharge (ESD)-protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.1. However, care should be exercised in handling this device as exposure to ESD may result in degradation of the device parametric performance.

AVAILABLE OPTIONS

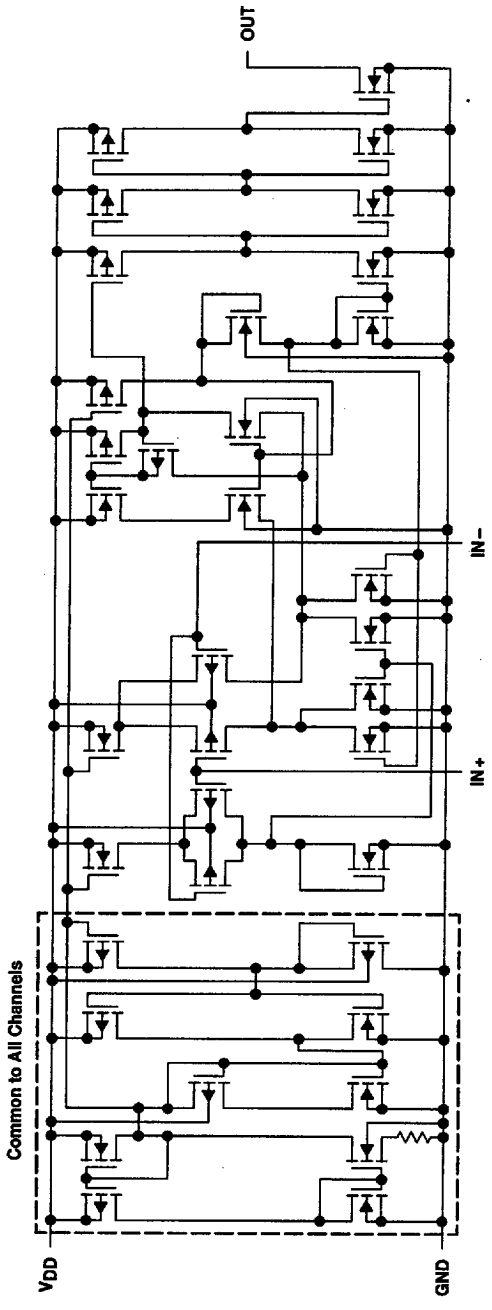
T_A	V_{IO}max at 25°C	PACKAGED DEVICES			CHIP FORM (Y)
		SMALL OUTLINE (D)	PLASTIC DIP (P)	TSSOP (PW)	
–40°C to 85°C	5 mV	TLV2352ID	TLV2352IP	TLV2352IPWLE	TLV2352Y

The D package is available taped and reeled. Add the suffix R to the device type (e.g., TLV2352IDR).
The PW packages are only available left-ended taped and reeled (e.g., TLV2352IPWLE)

These devices have limited built-in protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

LinBiCMOS is a trademark of Texas Instruments Incorporated.

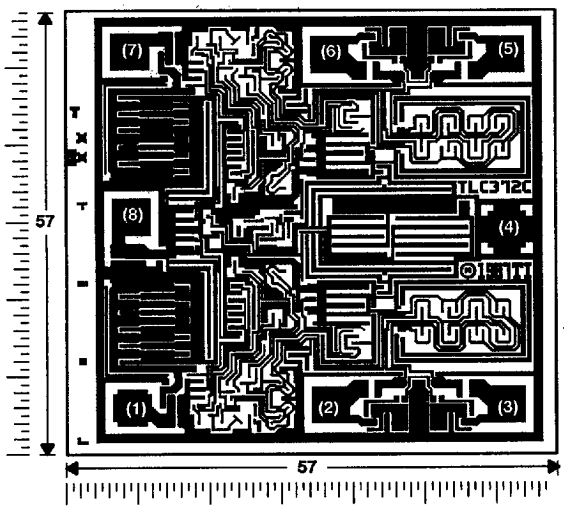
equivalent schematic

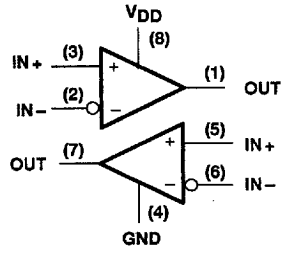


TLV2352Y chip information

These chips, when properly assembled, display characteristics similar to the TLV2352. Thermal compression or ultrasonic bonding may be used on the doped-aluminum bonding pads. Chips may be mounted with conductive epoxy or a gold-silicon preform.

BONDING PAD ASSIGNMENTS





CHIP THICKNESS: 15 TYPICAL

BONDING PADS: 4 × 4 MINIMUM

$T_J$max = 150°C

TOLERANCES ARE ±10%.

ALL DIMENSIONS ARE IN MILS.

PIN (4) INTERNALLY CONNECTED TO BACKSIDE OF CHIP.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{DD} (see Note 1) ..... 8 V
Differential input voltage, V_{ID} (see Note 2) ..... ±8 V
Input voltage range, V_I ..... −0.3 to 8 V
Output voltage, V_O ..... 8 V
Input current, I_I ..... ±5 mA
Output current, I_O ..... 20 mA
Duration of output short-circuit current to GND (see Note 3) ..... unlimited
Continuous total power dissipation ..... See Dissipation Rating Table
Operating free-air temperature range, T_A ..... −40°C to 85°C
Storage temperature range ..... −65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds ..... 260°C

† Stress beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. All voltage values, except differential voltages, are with respect to network ground.
2. Differential voltages are at IN+ with respect to IN−.
3. Short circuits from outputs to V_{DD} can cause excessive heating and eventual device destruction.

DISSIPATION RATING TABLE

PACKAGE	$T_A \le 25°C$ POWER RATING	DERATING FACTOR	$T_A = 85°C$ POWER RATING
D	725 mW	5.8 mW/°C	377 mW
P	1000 mW	8.0 mW/°C	520 mW
PW	525 mW	4.2 mW/°C	273 mW

recommended operating conditions

		MIN	MAX	UNIT
Supply voltage, V_{DD}		2	8	V
Common-mode input voltage, V_{IC}	V_{DD} = 3 V	0	1.75	V
	V_{DD} = 5 V	0	3.75	
Operating free-air temperature, T_A		−40	85	°C

electrical characteristics at specified free-air temperature†

PARAMETER		TEST CONDITIONS	T_A‡	TLV2352I						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min, See Note 4	25°C		1	5		1	5	mV
			Full range			7			7	
I_{IO}	Input offset current		25°C		1			1		pA
			85°C			1			1	nA
I_{IB}	Input bias current		25°C		5			5		pA
			85°C			2			2	nA
V_{ICR}	Common-mode input voltage range		25°C	0 to 2			0 to 4			V
			Full range	0 to 1.75			0 to 3.75			
I_{OH}	High-level output current	V_{ID} = 1 V	25°C		0.1			0.1		nA
			Full range			1			1	µA
V_{OL}	Low-level output voltage	V_{ID} = −1 V, I_{OL} = 2 mA	25°C		115	300		150	400	mV
			Full range			600			700	
I_{OL}	Low-level output current	V_{ID} = −1 V, V_{OL} = 1.5 V	25°C	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V, No load	25°C		120	250		140	300	µA
			Full range			350			400	

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.
‡ Full range is −40°C to 85°C. IMPORTANT: See Parameter Measurement Information.
NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

switching characteristics, V_{DD} = 3 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV2352I			UNIT
			MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, C_L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		640		ns

switching characteristics, V_{DD} = 5 V, T_A = 25°C

PARAMETER	TEST CONDITIONS		TLV2352I			UNIT
			MIN	TYP	MAX	
Response time	R_L = 5.1 kΩ, C_L = 15 pF§, See Note 5	100-mV input step with 5-mV overdrive		650		ns
		TTL-level input step		200		

§ C_L includes probe and jig capacitance.
NOTE 5: The response time specified is the interval between the input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or V_O = 1.4 V with V_{DD} = 5 V.

electrical characteristics at specified free-air temperature, T_A = 25°C†

PARAMETER		TEST CONDITIONS		TLV2352Y						UNIT
				V_{DD} = 3 V			V_{DD} = 5 V			
				MIN	TYP	MAX	MIN	TYP	MAX	
V_{IO}	Input offset voltage	$V_{IC} = V_{ICR}$min,	See Note 4		1	5		1	5	mV
I_{IO}	Input offset current				1			1		pA
I_{IB}	Input bias current				5			5		pA
V_{ICR}	Common-mode input voltage range			0 to 2			0 to 4			V
I_{OH}	High-level output current	V_{ID} = 1 V			0.1			0.1		nA
V_{OL}	Low-level output voltage	V_{ID} = −1 V	I_{OL} = 2 mA		115	300		150	400	mV
I_{OL}	Low-level output current	V_{ID} = −1 V,	V_{OL} = 1.5 V	6	16		6	16		mA
I_{DD}	Supply current	V_{ID} = 1 V	No load		120	250		140	300	µA

† All characteristics are measured with zero common-mode input voltages unless otherwise noted.

NOTE 4: The offset voltage limits given are the maximum values required to drive the output above 4 V with V_{DD} = 5 V, 2 V with V_{DD} = 3 V, or below 400 mV with a 10-kΩ resistor between the output and V_{DD}. They can be verified by applying the limit value to the input and checking for the appropriate output state.

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT VOLTAGE
vs
LOW-LEVEL OUTPUT CURRENT

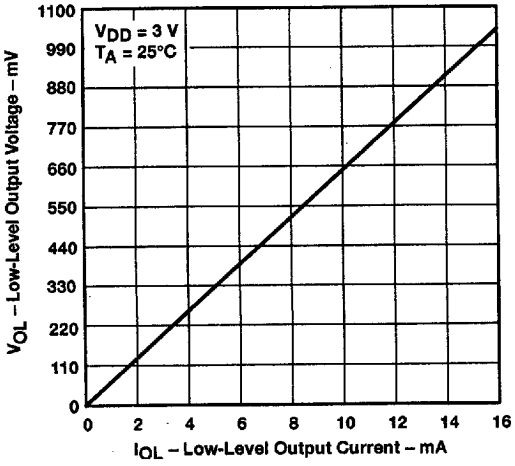


Figure 1

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

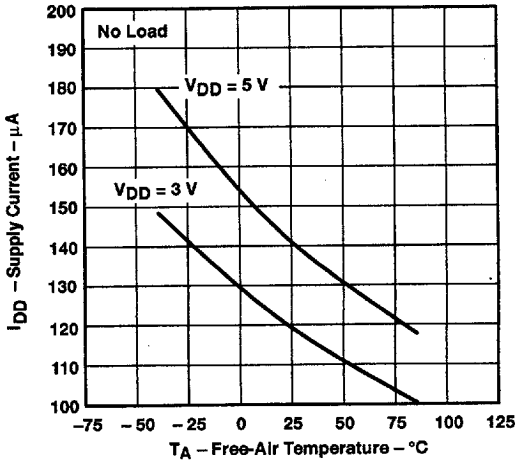


Figure 2

COMMON-MODE INPUT VOLTAGE RANGE
vs
FREE-AIR TEMPERATURE

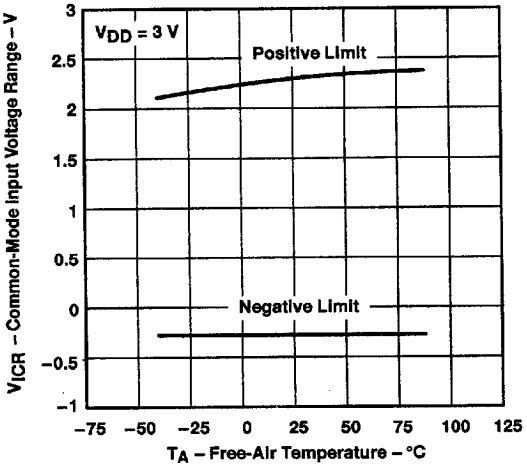


Figure 3

OUTPUT FALL TIME
vs
CAPACITIVE LOAD

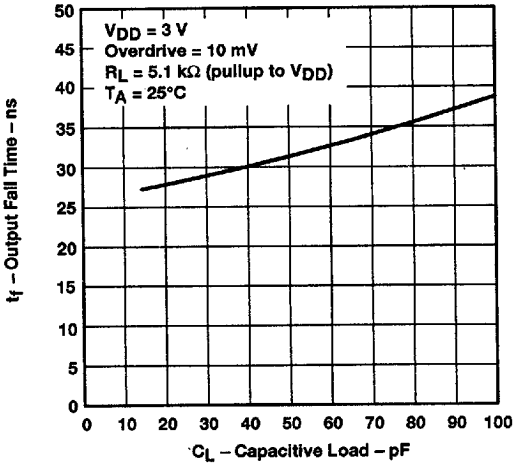


Figure 4

TYPICAL CHARACTERISTICS

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

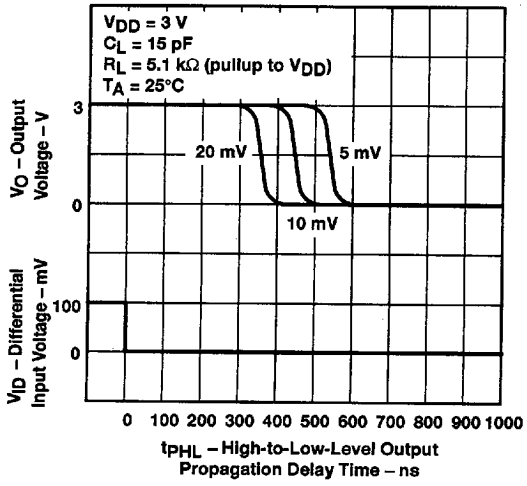


Figure 5

HIGH-TO-LOW-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

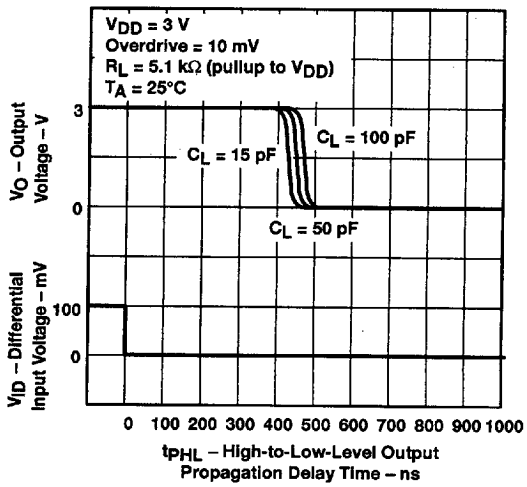


Figure 6

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS OVERDRIVE VOLTAGES

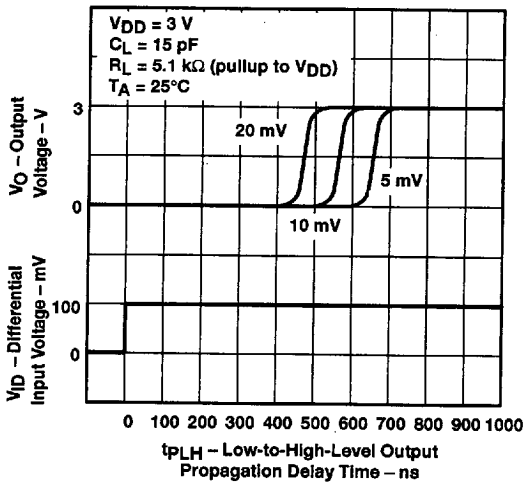


Figure 7

LOW-TO-HIGH-LEVEL OUTPUT
PROPAGATION DELAY
FOR VARIOUS CAPACITIVE LOADS

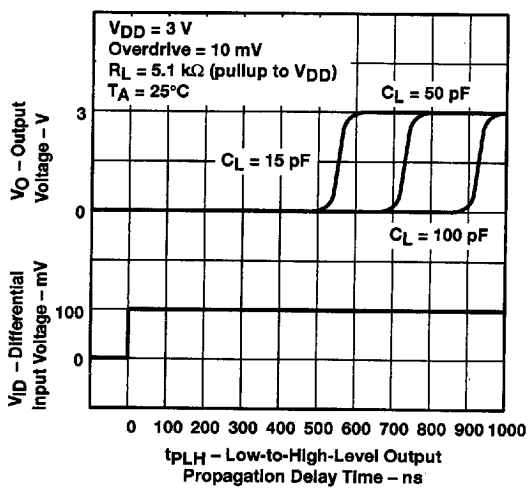


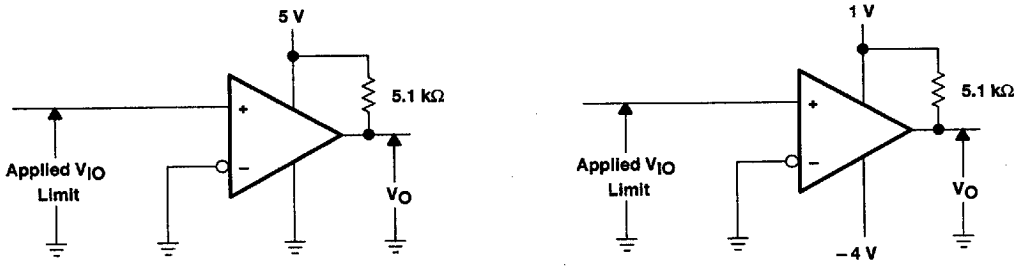
Figure 8

PARAMETER MEASUREMENT INFORMATION

The digital output stage of the TLV2352 can be damaged if it is held in the linear region of the transfer curve. Conventional operational amplifier/comparator testing incorporates the use of a servo loop that is designed to force the device output to a level within this linear region. Since the servo-loop method of testing cannot be used, the following alternatives for measuring parameters such as input offset voltage, common-mode rejection, etc., are offered.

To verify that the input offset voltage falls within the limits specified, the limit value is applied to the input as shown in Figure 9(a). With the noninverting input positive with respect to the inverting input, the output should be high. With the input polarity reversed, the output should be low.

A similar test can be made to verify the input offset voltage at the common-mode extremes. The supply voltages can be slewed as shown in Figure 9(b) for the V_{ICR} test, rather than changing the input voltages to provide greater accuracy.



(a) V_{IO} WITH V_{IC} = 0 (b) V_{IO} WITH V_{IC} = 4 V

Figure 9. Method for Verifying That Input Offset Voltage Is Within Specified Limits

A close approximation of the input offset voltage can be obtained by using a binary search method to vary the differential input voltage while monitoring the output state. When the applied input voltage differential is equal but opposite in polarity to the input offset voltage, the output changes states.

PARAMETER MEASUREMENT INFORMATION

Figure 10 illustrates a practical circuit for direct dc measurement of input offset voltage that does not bias the comparator in the linear region. The circuit consists of a switching-mode servo loop in which U1a generates a triangular waveform of approximately 20-mV amplitude. U1b acts as a buffer with C2 and R4 removing any residual dc offset. The signal is then applied to the inverting input of the comparator under test while the noninverting input is driven by the output of the integrator formed by U1c through the voltage divider formed by R9 and R10. The loop reaches a stable operating point when the output of the comparator under test has a duty cycle of exactly 50%, which can only occur when the incoming triangle wave is sliced symmetrically or when the voltage at the noninverting input exactly equals the input offset voltage.

Voltage dividers R9 and R10 provide a step up of the input offset voltage by a factor of 100 to make measurement easier. The values of R5, R8, R9, and R10 can significantly influence the accuracy of the reading; therefore, it is suggested that their tolerance level be 1% or lower.

Measuring the extremely low values of input current requires isolation from all other sources of leakage current and compensation for the leakage of the test socket and board. With a good picoammeter, the socket and board leakage can be measured with no device in the socket. Subsequently, this open-socket leakage value can be subtracted from the measurement obtained with a device in the socket to obtain the actual input current of the device.

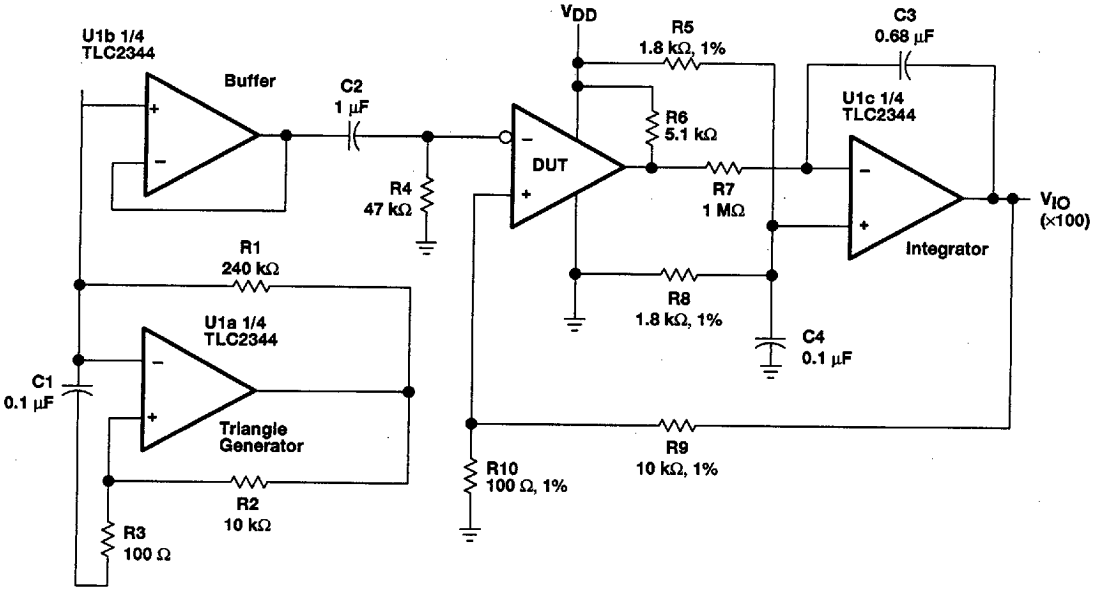
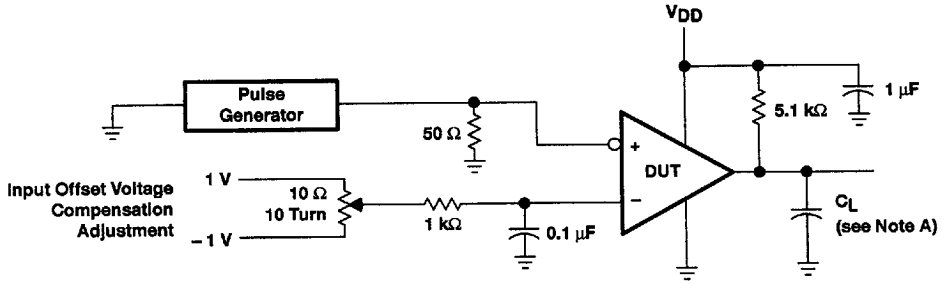


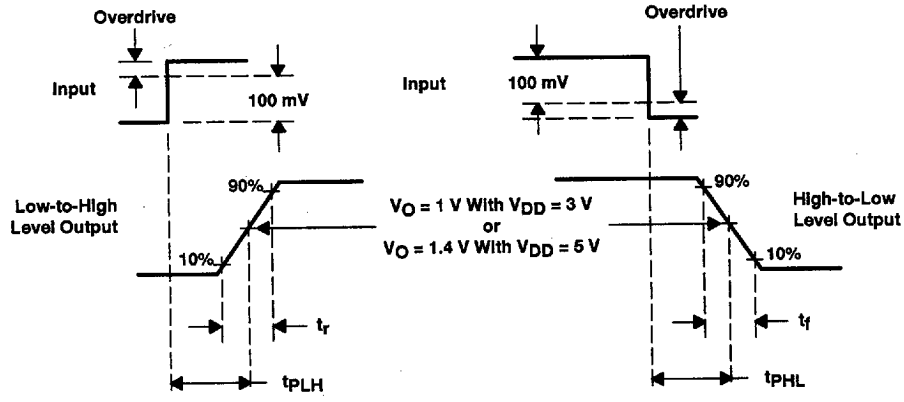
Figure 10. Circuit for Input Offset Voltage Measurement

PARAMETER MEASUREMENT INFORMATION

Propagation delay time is defined as the interval between the application of an input step function and the instant when the output crosses V_O = 1 V with V_{DD} = 3 V or when the output crosses V_O = 1.4 V with V_{DD} = 5 V. Propagation delay time, low-to-high-level output, is measured from the leading edge of the input pulse while propagation delay time, high-to-low-level output, is measured from the trailing edge of the input pulse. Propagation-delay-time measurement at low input signal levels can be greatly affected by the input offset voltage. The offset voltage should be balanced by the adjustment at the inverting input (as shown in Figure 11) so that the circuit is just at the transition point. Then a low signal, for example 105-mV or 5-mV overdrive, causes the output to change states.



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTE A: C_L includes probe and jig capacitance.

Figure 11. Propagation Delay, Rise, and Fall Times Test Circuit and Voltage Waveforms