GENLINX™ GS9004A
Serial Digital Cable Equalizer

DATA SHEET

FEATURES

- **automatic cable equalization**
- **typically greater than 300 m of high quality cable at 270 Mb/s**
- **fully compatible with SMPTE 259M and operational to 400 Mb/s**
- **signal strength indicator**
- **output 'eye' monitor**
- **14 pin SOIC packaging**
- **single +5 or -5 volt power supply operation**

APPLICATIONS

- Front-end cable equalization for digital video systems
- Input equalization for serial digital distribution amplifiers, routers, production switchers and other receiving equipment

ORDERING INFORMATION

Part Number	Package Type	Temperature Range
GS9004ACKB	14 pin SOIC	0 to 70°C
GS9004ACTB	14 pin SOIC Tape	0 to 70°C

DEVICE DESCRIPTION

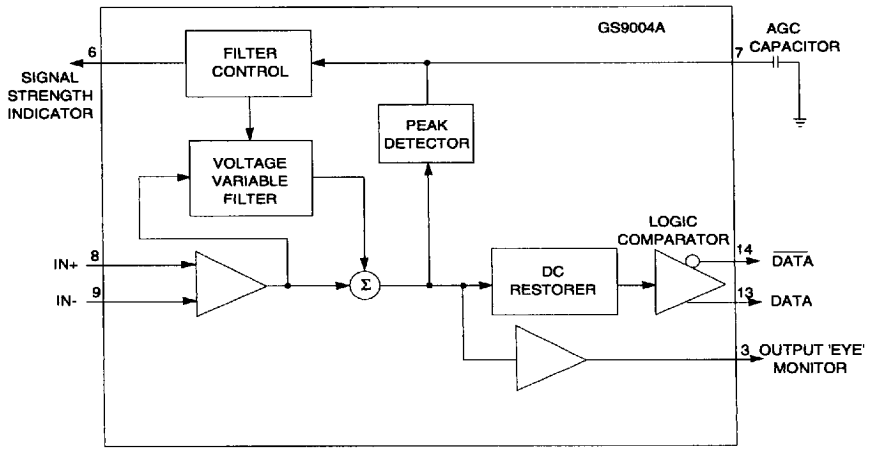
The Gennum GS9004A is a monolithic automatic cable equalizer developed for SMPTE/EBU scrambled NRZI Serial Digital Video signals.

This device features DC restoration to pass the Pathological Test Signals and fully automatic equalization in order to meet the SMPTE 259M Serial Interface Standard. The DATA and $\overline{\text{DATA}}$ outputs typically deliver 800 mV (p-p) equalized signals into 100 Ω loads. These signals can be used to feed cable driver circuits for Serial Distribution Amplifier applications.

This device also incorporates an analog signal strength indicator (SSI) which provides a 0.5 V to 0 V output relative to V_{CC}, indicating the amount of equalization being applied to the signal.

The GS9004A features an OUTPUT 'EYE' MONITOR (OEM), which allows verification of signal integrity after equalization, prior to reslicing.

Operating with a single +5 or -5 volt supply, the GS9004A typically draws 52 mA of current.



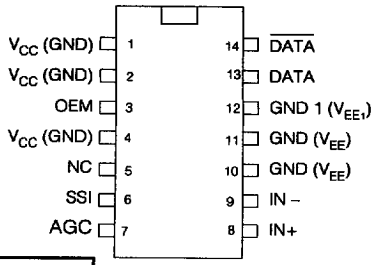
Patents No. 5,420,524, and 5,426,389.

FUNCTIONAL BLOCK DIAGRAM

ABSOLUTE MAXIMUM RATINGS

PARAMETER	VALUE
Supply Voltage (V_S)	5.5 V
Input Voltage Range (any Input)	V_{CC}+0.5 to V_{EE} -0.5 V
DC Input Current (any one input)	10 mA
Power Dissipation	500 mW
Operating Temperature Range	0°C ≤ T_A ≤ 70°C
Storage Temperature Range	-65°C ≤ T_S ≤ 150°C
Lead Temperature (soldering, 10 sec)	260°C

GS9004A PIN CONNECTIONS



PIN DESCRIPTIONS (I = INPUT, O = OUTPUT, S = SUPPLY function)

PIN NO.	SYMBOL	I/O	DESCRIPTION
1	V_{CC} (GND)	S	Most positive supply voltage (ECL outputs)
2	V_{CC}(GND)	S	Most positive supply voltage (DC Restore/Eye Monitor)
3	OEM	O	Output 'Eye' Monitor
4	V_{CC}(GND)	S	Most positive supply voltage (Equalizer)
5	NC		No Connection
6	SSI	O	Signal Strength Indicator
7	AGC	I	AGC capacitor connection
8	IN+	I	Non-inverting signal
9	IN-	I	Inverting signal
10	GND(V_{EE})	S	Most negative supply voltage
11	GND(V_{EE})	S	Most negative supply voltage
12	GND1(V_{EE1})	S	Most negative supply voltage for EYE MONITOR
13	DATA	O	DATA (true)
14	$\overline{DATA}$	O	DATA (inverse)

GS9004A DC ELECTRICAL CHARACTERISTICS

Conditions: V_S = 5 V, T_A = 0° to 70°C, R_L = 100 Ω, to (V_{CC} -2) volts, unless otherwise shown.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Supply Voltage	V_S	Operating Range	4.75	5.0	5.25	V	
Power Consumption	P_D		-	285	360	mW	
		With MONITOR active	-	330	415	mW	
Supply Current	I_S		-	52	72	mA	
		With MONITOR active	-	60	83	mA	
Serial Data Output - High	$V_{OH\ MIN}$	T_A = 25°C	-1.025	-	-0.88	V	with respect to V_{CC}
- Low	$V_{OL\ MAX}$	T_A = 25°C	-1.8	-	-1.6	V	with respect to V_{CC}

GS9004A AC ELECTRICAL CHARACTERISTICS

Conditions: V_S = 5 V, T_A = 0° to 70°C, R_L = 100 Ω, to (V_{CC} -2) volts, unless otherwise shown

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS	NOTES
Output Signal Swing	V_O	T_A = 25°C	700	800	900	mV	
Input Resistance(IN+, IN-)	R_{IN}		3k	5k	-	Ω	see fig. 8
Input Capacitance(IN+, IN-)	C_{IN}	T_A = 25°C	-	1.3	-	pF	see fig. 8
Output 'Eye' Monitor	V_{OEM}	R_L = 50Ω, To V_{CC}	-	40	-	mV p-p	
Signal Strength Output	V_{SS}		4.4	-	5	V	see Fig. 5
GS9004A GAIN	A_V	T_A = 25°C f=135 MHz	30	33	-	dB	see Fig. 4
JITTER 270Mb/s	t_J	T_A = 25°C, 300m of 8281 cable.	-	500	-	ps p-p	Test setup 1 see Fig. 7

GS9004A CABLE EQUALIZER - DETAILED DEVICE DESCRIPTION

The GS9004A Cable Equalizer is a bipolar integrated circuit used to equalize SMPTE 259M signals from a co-axial cable. The device is implemented as a fourteen pin SOIC, powered from a single five volt supply. With an operating frequency up to 400 Mb/s, the equalizer consumes about 285 mW of power.

The Serial Digital signal is connected to the input (pins 8, 9) either differentially or single ended with the unused input being decoupled. The equalized signal is generated by passing the cable signal through a voltage variable filter having a characteristic which closely matches the inverse cable loss characteristic. Additionally, the variation of the filter characteristic with control voltage is designed to imitate the variation of the inverse cable loss characteristic as the cable length is varied.

The amplitude of the equalized signal is monitored by a peak detector circuit which produces an output current with a polarity corresponding to the difference between the desired peak signal level and the actual peak signal level.

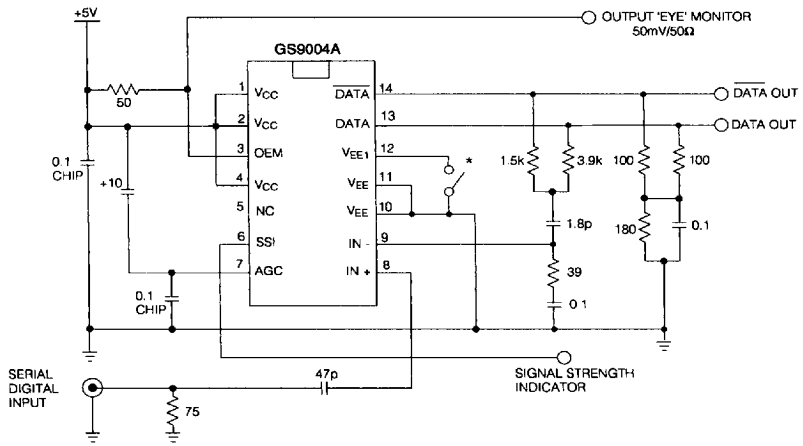
This output is integrated by an external AGC filter capacitor (AGC CAP pin 7), providing a steady control voltage for the voltage variable filter.

A separate signal strength indicator output, (SSI pin 6), proportional to the amount of AGC, is also provided. As the filter characteristic is varied automatically by the application of negative feedback, the amplitude of the equalized signal is kept at a constant level which is representative of the original amplitude at the transmitter.

The equalized signal is then DC restored, effectively restoring the logic threshold of the equalized signal to its correct level irrespective of shifts due to AC coupling.

As the final stage of signal conditioning, a comparator converts the analog output of the DC restorer to a regenerated digital output signal having pseudo-ECL voltage levels. These outputs, DATA and $\overline{\text{DATA}}$, are available from pins 13 and 14 respectively.

An OUTPUT 'EYE' MONITOR (pin 3) allows verification of signal integrity after equalization, prior to reslicing.



Note: All resistors in ohms, all capacitors in microfarads unless otherwise stated.
* Pin 12 is connected to V_{EE} (GND) when the MONITOR function is desired.

Patents Pending

Fig. 1 Test Circuit

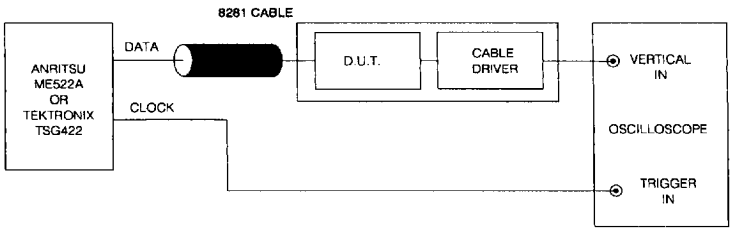


Fig. 2 Test Set-up 1

TYPICAL PERFORMANCE CURVES (unless otherwise shown V_S = 5V, T_A = 25°C)

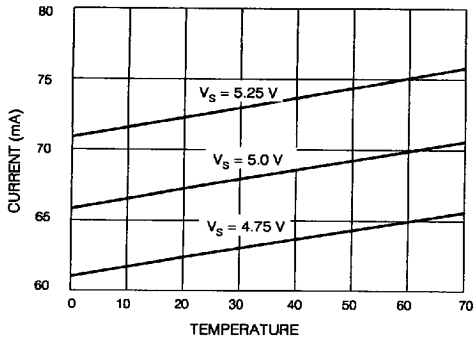


Fig. 3 Supply Current

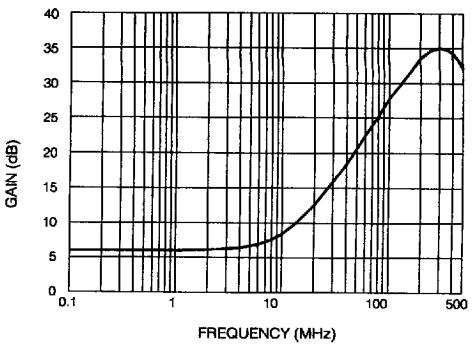


Fig. 4 Equalizer Gain

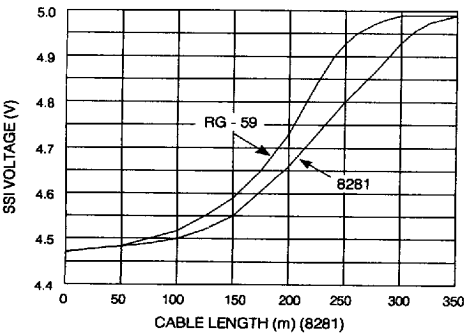


Fig. 5 Signal Strength Output

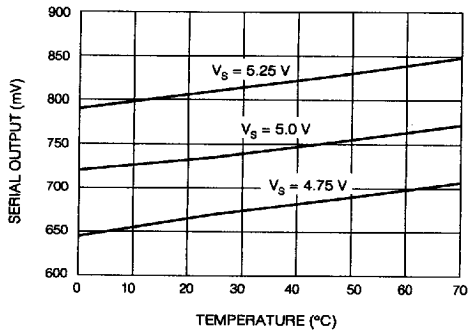


Fig. 6 Data and $\overline{\text{Data}}$ Output

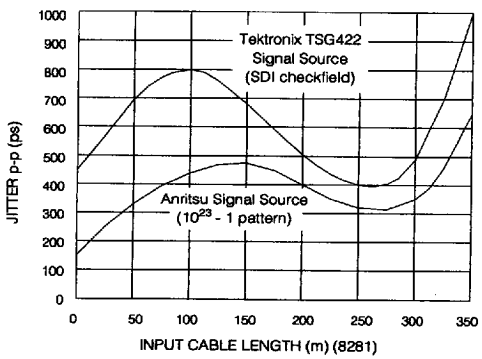
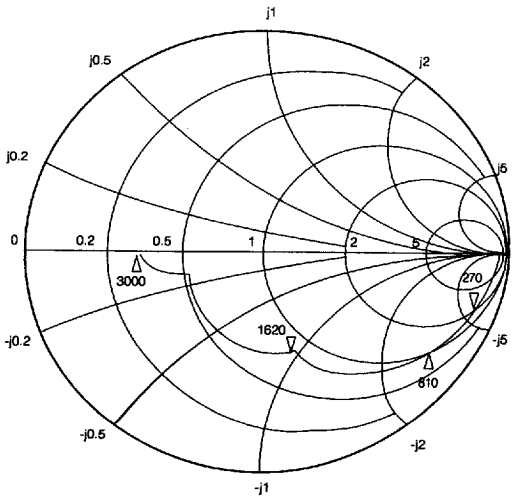


Fig. 7 Output Jitter vs Input Cable Length at 270 Mb/s



Δ Frequencies in MHz, impedances normalized to 50 Ω.

Fig. 8 Equalizer Input Impedance

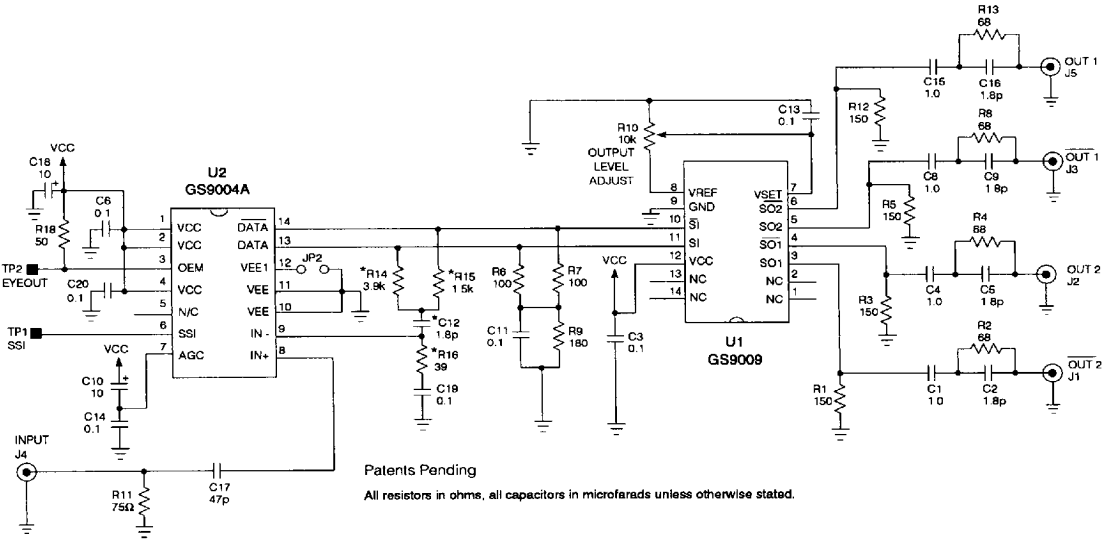


Fig. 9 Typical Application Circuit

In the above circuit JP2 enables the "EYE' monitor. Components R14, R15, R16 and C12 are used to reduce long cable length jitter. This is accomplished by feeding back a controlled portion of the true and inverse output signals to the inverting input. In this manner the effects of bond wire and packaging parasitics (which increase the jitter under low signal to noise ratio conditions) are significantly reduced. The circuit is independent of PCB layout or loading conditions.

In multi-input applications these components may increase cross-talk between channels. Figure 9 shows the circuit of a non-reclocking distribution amplifier using the GS9004A equalizer and GS9009 cable driver.

Complete circuit descriptions and PCB details are available in Application Note 520 - 84 entitled "Serial Digital Non - Reclocking Distribution Amplifier using the GS9004 and GS9009".

The Application Note and Evaluation Board is available from Gennum.

REVISION NOTES

Tape ordering information added.

CAUTION
ELECTROSTATIC
SENSITIVE DEVICES
DO NOT OPEN PACKAGES OR HANDLE
EXCEPT AT A STATIC-FREE WORKSTATION