FAIRCHILD

SEMICONDUCTOR®

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74VHCT14A
Hex Schmitt Inverter

Features

- High speed: t_{PD} = 5.0ns (Typ.) at T_A = 25°C
- High noise immunity: V_{IH} = 2.0V, V_{IL} = 0.8V
- Power down protection is provided on all inputs and outputs
- Low noise: V_{OLP} = 1.0V (Max.)
- Low power dissipation: I_{CC} = 2µA (Max.) @ T_A = 25°C
- Pin and function compatible with 74HCT14

General Description

The VHCT14A is an advanced high speed CMOS Hex Schmitt Inverter fabricated with silicon gate CMOS technology. The VHCT14A contains six independent inverters which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with V_{CC} = 0V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to inter-face 3V to 5V systems and two supply systems such as battery backup.

Ordering Information

Order Number	Package Number	Package Description
74VHCT14AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHCT14ASJ	M14D	14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT14AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering number.

All packages are lead free per JEDEC: J-STD-020B standard.

Connection Diagram

Pin			Pin	
A_0	1		14	V_{CC}
$\overline{O}_0$	2		13	A_3
A_1	3		12	$\overline{O}_3$
$\overline{O}_1$	4		11	A_4
A_2	5		10	$\overline{O}_4$
$\overline{O}_2$	6		9	A_5
GND	7		8	$\overline{O}_5$
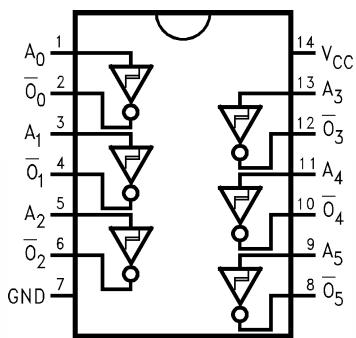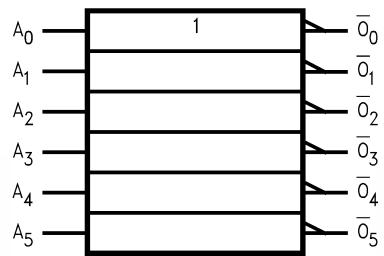
Pin Description

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Logic Symbol

Truth Table

A	$\overline{O}$
L	H
H	L

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	–0.5V to +7.0V
V_{IN}	DC Input Voltage	–0.5V to +7.0V
V_{OUT}	DC Output Voltage Note 1 Note 2	 –0.5V to V_{CC} + 0.5V –0.5V to 7.0V
I_{IK}	Input Diode Current	–20mA
I_{OK}	Output Diode Current[3]	±20mA
I_{OUT}	DC Output Current	±25mA
I_{CC}	DC V_{CC}/GND Current	±50mA
T_{STG}	Storage Temperature	–65°C to +150°C
T_L	Lead Temperature (Soldering, 10 seconds)	260°C

Recommended Operating Conditions[4]

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	4.5V to +5.5V
V_{IN}	Input Voltage	0V to +5.5V
V_{OUT}	Output Voltage Note 1 Note 2	 0V to V_{CC} 0V to +5.5V
T_{OPR}	Operating Temperature	–40°C to +85°C

Notes:

1. HIGH or LOW state. I_{OUT} absolute maximum rating must be observed.

2. V_{CC} = 0V.

3. V_{OUT} < GND, V_{OUT} > V_{CC} (Outputs Active).

4. Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	V$_{CC}$ (V)	Conditions		T$_A$ = 25°C			T$_A$ = −40°C to +85°C		Units
					Min.	Typ.	Max.	Min.	Max.	
V$_P$	Positive Threshold Voltage	4.5					1.9		1.9	V
		5.5					2.1		2.1	
V$_N$	Negative Threshold Voltage	4.5			0.5			0.5		V
		5.5			0.6			0.6		
V$_H$	Hysteresis Voltage	4.5			0.4		1.4	0.4	1.4	V
		5.5			0.4		1.5	0.4	1.5	
V$_{OH}$	HIGH Level Output Voltage	4.5	V$_{IN}$ = V$_{IL}$	I$_{OH}$ = −50µA	4.40	4.50		4.40		V
				I$_{OH}$ = −8mA	3.94			3.80		
V$_{OL}$	LOW Level Output Voltage	4.5	V$_{IN}$ = V$_{IH}$	I$_{OL}$ = 50µA		0.0	0.1		0.1	V
				I$_{OL}$ = 8mA			0.36		0.44	
I$_{IN}$	Input Leakage Current	0 – 5.5	V$_{IN}$ = 5.5V or GND				±0.1		±1.0	µA
I$_{CC}$	Quiescent Supply Current	5.5	V$_{IN}$ = V$_{CC}$ or GND				2.0		20.0	µA
I$_{CCT}$	Maximum I$_{CC}$ / Input	5.5	V$_{IN}$ = 3.4V, Other Inputs = V$_{CC}$ or GND				1.35		1.50	mA
I$_{OFF}$	Output Leakage Current (Power Down State)	0.0	V$_{OUT}$ = 5.5V				0.5		5.0	µA

Noise Characteristics

Symbol	Parameter	V$_{CC}$ (V)	Conditions	T$_A$ = 25°C		Units
				Typ.	Limits	
V$_{OLP}$[5]	Quiet Output Maximum Dynamic V$_{OL}$	5.0	C$_L$ = 50pF	0.8	1.0	V
V$_{OLV}$[5]	Quiet Output Minimum Dynamic V$_{OL}$	5.0	C$_L$ = 50pF	−0.8	1.0	V
V$_{IHD}$[5]	Minimum HIGH Level Dynamic Input Voltage	5.0	C$_L$ = 50pF		2.0	V
V$_{ILD}$[5]	Maximum LOW Level Dynamic Input Voltage	5.0	C$_L$ = 50pF		0.8	V

Note:

5. Parameter guaranteed by design.

AC Electrical Characteristics

Symbol	Parameter	V$_{CC}$ (V)	Conditions	T$_A$ = 25°C			T$_A$ = −40°C to +85°C		Units
				Min.	Typ.	Max.	Min.	Max.	
t$_{PHL}$, t$_{PLH}$	Propagation Delay	5.0 ± 0.5	C$_L$ = 15pF		5.0	7.6	1.0	9.0	ns
			C$_L$ = 50pF		6.5	9.6	1.0	11.0	
C$_{IN}$	Input Capacitance		V$_{CC}$ = OPEN		2	10		10	pF
C$_{PD}$	Power Dissipation Capacitance		[6]		11				pF

Note:

6. C$_{PD}$ is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:

$$I_{CC} \text{ (Opr.)} = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC} / 6 \text{ (per gate)}$$

Physical Dimensions

8.75
8.50

A

7.62

14   8

B

6.00

4.00
3.80

PIN ONE
INDICATOR

1   7

1.27

0.51
0.35

(0.33)

⊕ | 0.25 Ⓜ | C | B | A

0.65

5.60

1.70   1.27

LAND PATTERN RECOMMENDATION

1.75 MAX
1.50
1.25

0.25
0.10   C

△ | 0.10 | C

SEE DETAIL A

0.25
0.19
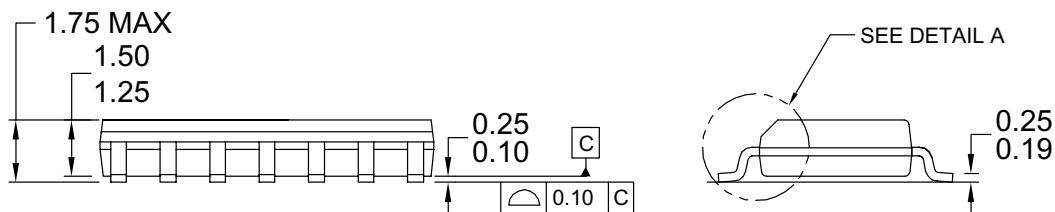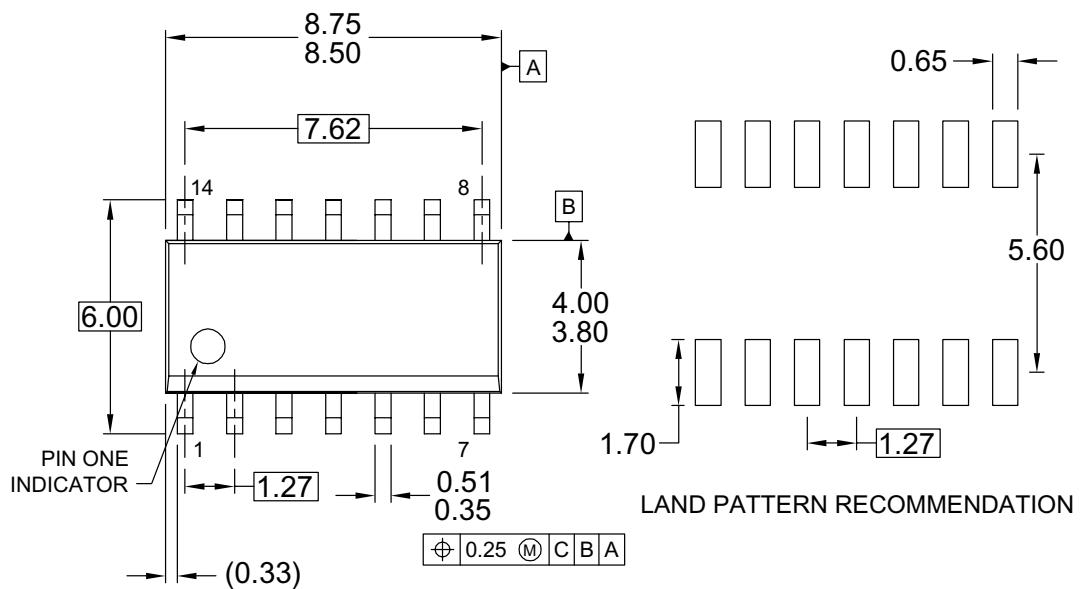
NOTES: UNLESS OTHERWISE SPECIFIED
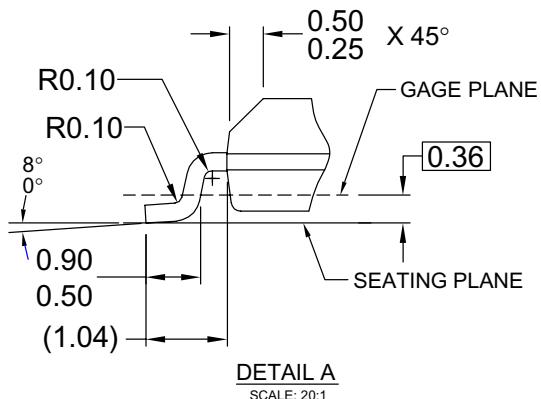
A) THIS PACKAGE CONFORMS TO JEDEC
   MS-012, VARIATION AB, ISSUE C,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD
   FLASH OR BURRS.
D) LANDPATTERN STANDARD:
   SOIC127P600X145-14M
E) DRAWING CONFORMS TO ASME Y14.5M-1994
F) DRAWING FILE NAME: M14AREV13

0.50
0.25   X 45°

R0.10

R0.10

GAGE PLANE

8°
0°

0.36

0.90

SEATING PLANE

0.50

(1.04)

DETAIL A
SCALE: 20:1

Figure 1. 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow

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Physical Dimensions (Continued)

10.2±0.1

−A−

1.1 TYP

14   8

7.8

5.3±0.1

−B−

3.9

PIN #1 IDENT.

1   7

0.2 C B A

ALL LEAD TIPS

LAND PATTERN RECOMMENDATION

14   13   9   8

5.01 TYP

9.27 TYP

(2.13 TYP)

1   2   6   7

1.27 TYP   0.6 TYP

ALL LEAD TIPS

0.1 C

2.1 MAX.

1.8±0.1

−C−

0.15±0.05

1.27 TYP   0.35−0.51

0.12(M) C A
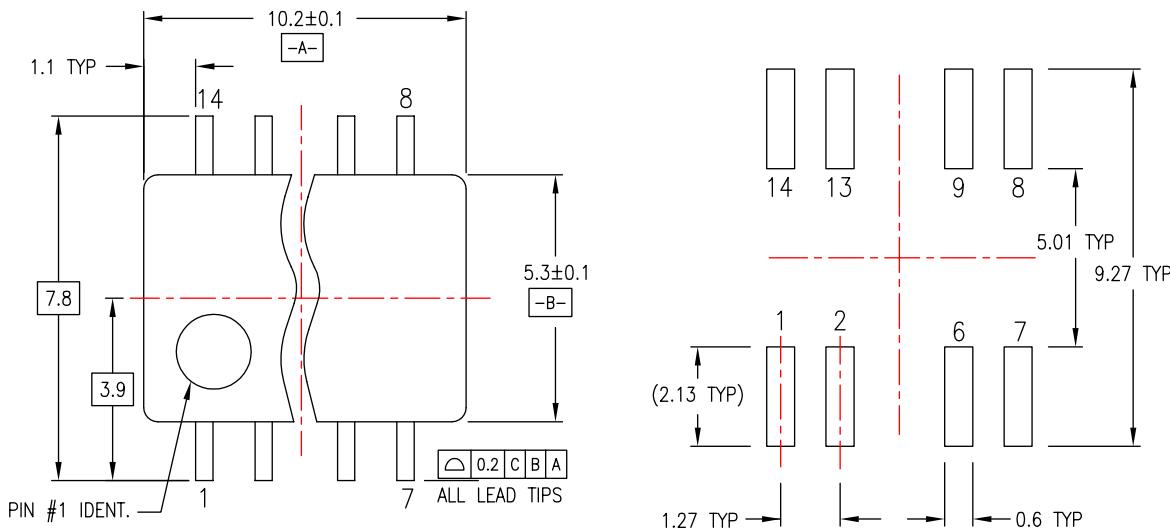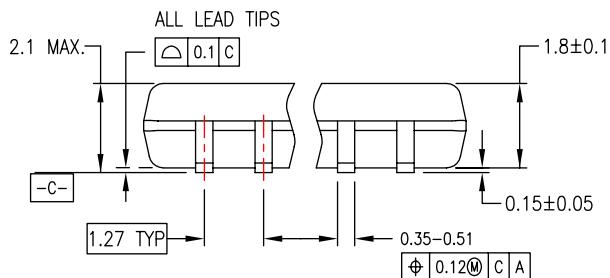
DIMENSIONS ARE IN MILLIMETERS

NOTES:
A. CONFORMS TO EIAJ EDR−7320 REGISTRATION,
    ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
    FLASH, AND TIE BAR EXTRUSIONS.

M14DREVC

SEE DETAIL A

0.15−0.25

7° TYP

GAGE PLANE

0°−8° TYP

0.25

0.60±0.15

1.25

SEATING PLANE
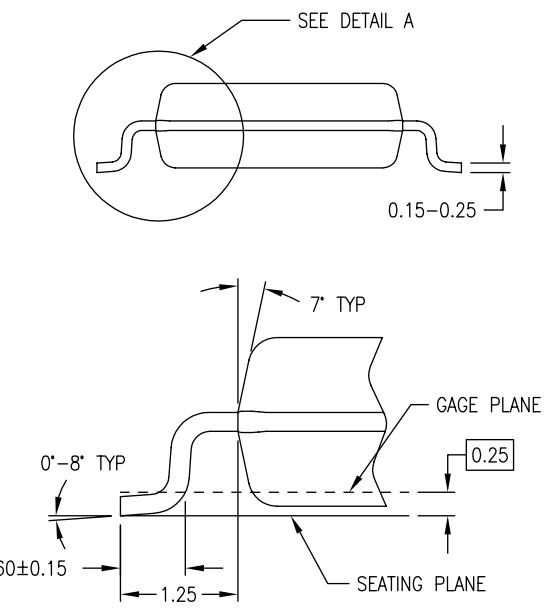
DETAIL A

Figure 2. 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide

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Physical Dimensions (Continued)

5.0±0.1
-A-

0.43 TYP

14   8

6.4

4.4±0.1
-B-

3.2

1

7

□ 0.2 C B A
ALL LEAD TIPS

PIN #1 IDENT.

0.65

1.65

0.45

6.10

LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
□ 0.1 C

1.2 MAX

0.90 +0.15 -0.10

-C-

0.10±0.05

0.65

0.19 - 0.30

⊕ 0.13 Ⓜ A BⓈ CⓈ

SEE DETAIL A

0.09-0.20

12.00° TOP & BOTTOM

R0.09 min

GAGE PLANE

0.25

0°-8°

0.6±0.1

SEATING PLANE

R0.09min

1.00

DETAIL A

NOTES:

A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6
B. DIMENSIONS ARE IN MILLIMETERS
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
D. DIMENSIONING AND TOLERANCES PER ANSI Y14.5M, 1982
E. LANDPATTERN STANDARD: SOP65P640X110-14M
F. DRAWING FILE NAME: MTC14REV6
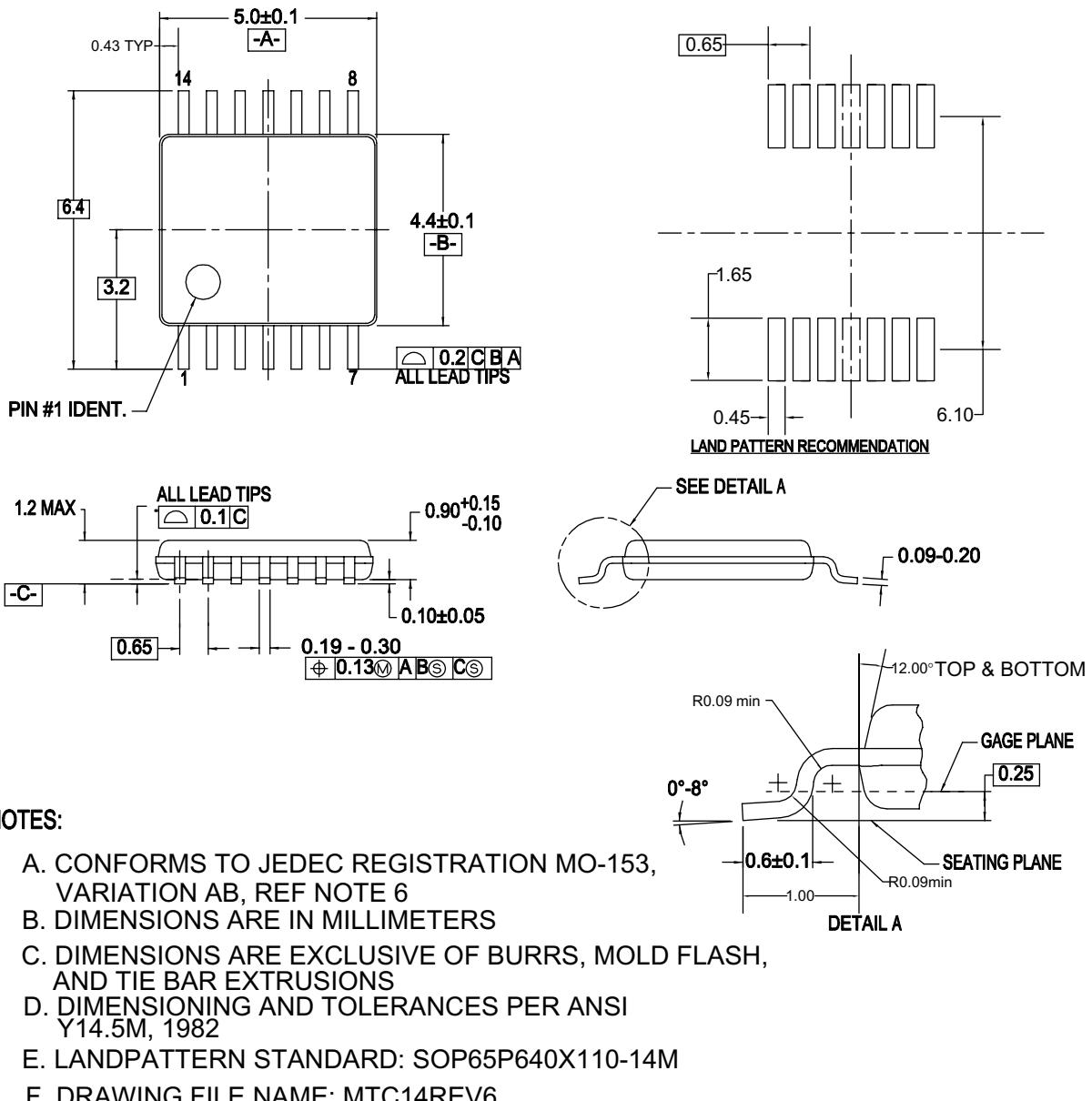
Figure 3. 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

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