HM-6514/883

March 1997

1024 x 4 CMOS RAM

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **Low Power Standby. . . . . 125μW Max**
- **Low Power Operation . . . . . .35mW/MHz Max**
- **Data Retention . . . . . at 2.0V Min**
- **TTL Compatible Input/Output**
- **Common Data Input/Output**
- **Three-State Output**
- **Standard JEDEC Pinout**
- **Fast Access Time . . . . . 120/200ns Max**
- **18 Pin Package for High Density**
- **Gated Inputs - No Pull Up or Pull Down Resistors Required**
- **On-Chip Address Register**

Description

The HM-6514/883 is a 1024 x 4 static CMOS RAM fabricated using self-aligned silicon gate technology. The device utilizes synchronous circuitry to achieve high performance and low power operation.

On chip latches are provided for addresses allowing efficient interfacing with microprocessor systems. The data output can be forced to a high impedance state for use in expanded memory arrays.

Gated inputs allow lower operating current and also eliminates the need for pull up or pull down resistors. The HM-6514/883 is fully static RAM and may be maintained in any state for an indefinite period of time.

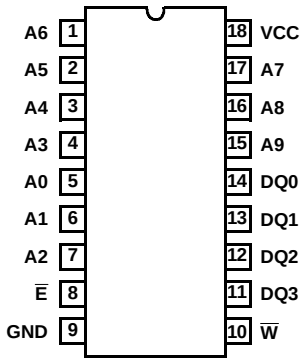
Data retention supply voltage and supply current are guaranteed over temperature.

Ordering Information

120ns	200ns	300ns	TEMPERATURE RANGE	PACKAGE	PKG. NO.
HM1-6514S/883	HM1-6514B/883	HM1-6514/883	-55^{O}C to 125^{O}C	CERDIP	F18.3

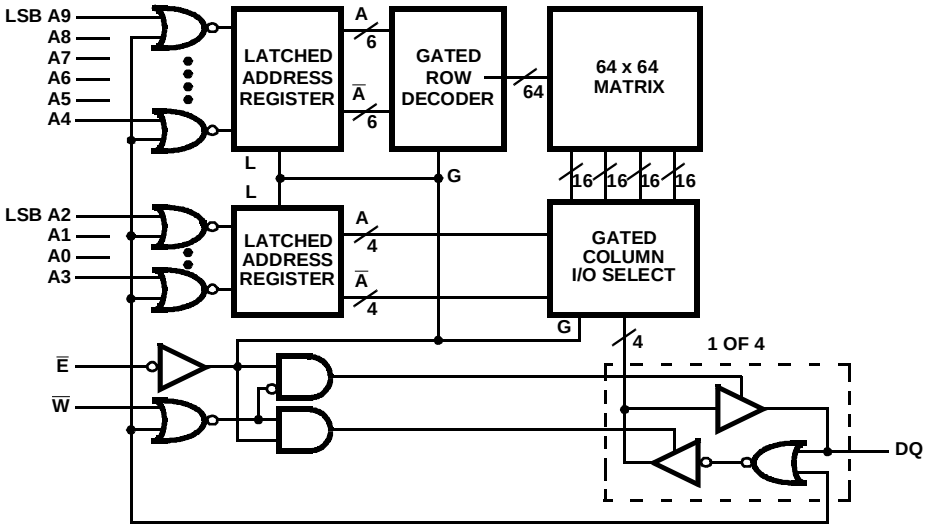
Pinout

HM-6514/883
(CERDIP)
TOP VIEW



PIN	DESCRIPTION
A	Address Input
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
D	Data Input
Q	Data Output

Functional Diagram



Absolute Maximum Ratings

Supply Voltage . . . . . +7.0V
Input, Output or I/O Voltage . . . . . GND -0.3V to VCC +0.3V
ESD Classification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
CERDIP Package	$75^oC/W$	$15^oC/W$

Maximum Storage Temperature Range . . . . . -65^oC to $+150^oC$
Maximum Junction Temperature. . . . . $+175^oC$
Maximum Lead Temperature (Soldering 10s). . . . . $+300^oC$

Die Characteristics

Gate Count . . . . . 6910 Gates

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

Operating Voltage Range . . . . . +4.5V to +5.5V
Operating Temperature Range. . . . . -55^oC to $+125^oC$
Input Low Voltage. . . . . 0V to +0.8V
Input High Voltage. . . . . VCC -2.0V to VCC
Input Rise and Fall Time . . . . . 40ns Max

TABLE 1. HM-6514/883 DC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTE 1) CONDITIONS	GROUP A SUBGROUPS	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNITS
Output Low Voltage	VOL	VCC = 4.5V IOL = 3.2mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	0.4	V
Output High Voltage	VOH	VCC = 4.5V IOH = -1.0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	2.4	-	V
Input Leakage Current	II	VCC = 5.5V, VI = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	+1.0	µA
Input/Output Leakage Current	IIOZ	VCC = 5.5 V, VIO = GND or VCC	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-1.0	+1.0	µA
Data Retention Supply Current	ICCDR	VCC = 2.0V, $\overline{E}$ = VCC -0.3V, IO = 0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	25	µA
Operating Supply Current	ICCOP	VCC = 5.5V, (Note 2) $\overline{E}$ = 1MHz	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	7	mA
Standby Supply Current	ICCSB	VCC = 5.5V, $\overline{E}$ = VCC-0.3V, IO = 0mA	1, 2, 3	$-55^oC \le T_A \le +125^oC$	-	50	µA

NOTES:

1. All voltages referenced to device GND.
2. Typical derating 1.5mA/MHz increase in ICCOP.

TABLE 2. HM-6514/883 AC ELECTRICAL PERFORMANCE SPECIFICATIONS

Device Guaranteed and 100% Tested

PARAMETER	SYMBOL	(NOTES 1, 2) CONDITIONS	GROUP A SUB-GROUPS	TEMPERATURE	LIMITS						UNITS
					HM-6514S/883		HM-6514B/883		HM-6514/883		
					MIN	MAX	MIN	MAX	MIN	MAX	
Chip Enable Access Time	(1) TELQV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	200	-	300	ns
Address Access Time	(2) TAVQV	VCC = 4.5 and 5.5V, Note 3	9, 10, 11	$-55^oC \le T_A \le +125^oC$	-	120	-	220	-	320	ns
Chip Enable Pulse Negative Width	(5) TELEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Chip Enable Pulse Positive Width	(6) TEHEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	90	-	120	-	ns
Address Setup Time	(7) TAVEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	20	-	20	-	ns
Address Hold Time	(8) TELAX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	40	-	50	-	50	-	ns
Write Enable Pulse Width	(9) TWLWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Write Enable Pulse Setup Time	(10) TWLEH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Write Enable Pulse Hold Time	(11) TELWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	120	-	200	-	300	-	ns
Data Setup Time	(12) TDVWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	50	-	120	-	200	-	ns
Data Hold Time	(13) TWHDX	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Write Data Delay Time	(14) TWLDV	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	70	-	80	-	100	-	ns
Early Output High-Z Time	(15) TWLEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Late Output High-Z Time	(16) TEHWH	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	0	-	0	-	0	-	ns
Read or Write Cycle Time	(17) TELEL	VCC = 4.5 and 5.5V	9, 10, 11	$-55^oC \le T_A \le +125^oC$	170	-	290	-	420	-	ns

NOTES:

1. All voltages referenced to device GND.
2. Input pulse levels: 0.8V to VCC-2.0V; Input rise and fall times: 5ns (max); Input and output timing reference level: 1.5V; Output load: 1 TTL gate equivalent, CL = 50pF (min) - for CL greater than 50pF, access time is derated by 0.15ns per pF.
3. TAVQV = TELQV + TAVEL.

TABLE 3. HM-6514/883 ELECTRICAL PERFORMANCE SPECIFICATIONS

PARAMETER	SYMBOL	CONDITIONS	NOTE	TEMPERATURE	HM-6514/883 LIMITS MIN	HM-6514/883 LIMITS MAX	UNITS
Input Capacitance	CI	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	8	pF
Input/Output Capacitance	CIO	VCC = Open, f = 1MHz, All Measurements Referenced to Device Ground	1	$T_A = +25^oC$	-	10	pF
Chip Enable Output Disable Time	TELQX	VCC = 4.5 and 5.5V	1	$-55^oC \le T_A \le +125^oC$	5	-	
Chip Enable Output Disable Time	TEHQZ	VCC = 4.5 and 5.5V HM-6514S/883	1	$-55^oC \le T_A \le +125^oC$	-	50	ns
		VCC = 4.5 and 5.5V HM-6514B/883	1	$-55^oC \le T_A \le +125^oC$	-	80	ns
		VCC = 4.5 and 5.5V HM-6514/883	1	$-55^oC \le T_A \le +125^oC$	-	100	ns
High Level Output Voltage	VOH2	VCC = 4.5V, IO = -100µA	1	$-55^oC \le T_A \le +125^oC$	VCC -0.4	-	V

NOTES:

1. The parameters listed in Table 3 are controlled via design, or process parameters are characterized upon initial design and after major process and/or design changes.

TABLE 4. APPLICABLE SUBGROUPS

CONFORMANCE GROUPS	METHOD	SUBGROUPS
Initial Test	100%/5004	-
Interim Test	100%/5004	1, 7, 9
PDA	100%/5004	1
Final Test	100%/5004	2, 3, 8A, 8B, 10, 11
Group A	Samples/5005	1, 2, 3, 7, 8A, 8B, 9, 10, 11
Groups C & D	Samples/5005	1, 7, 9

Timing Waveforms

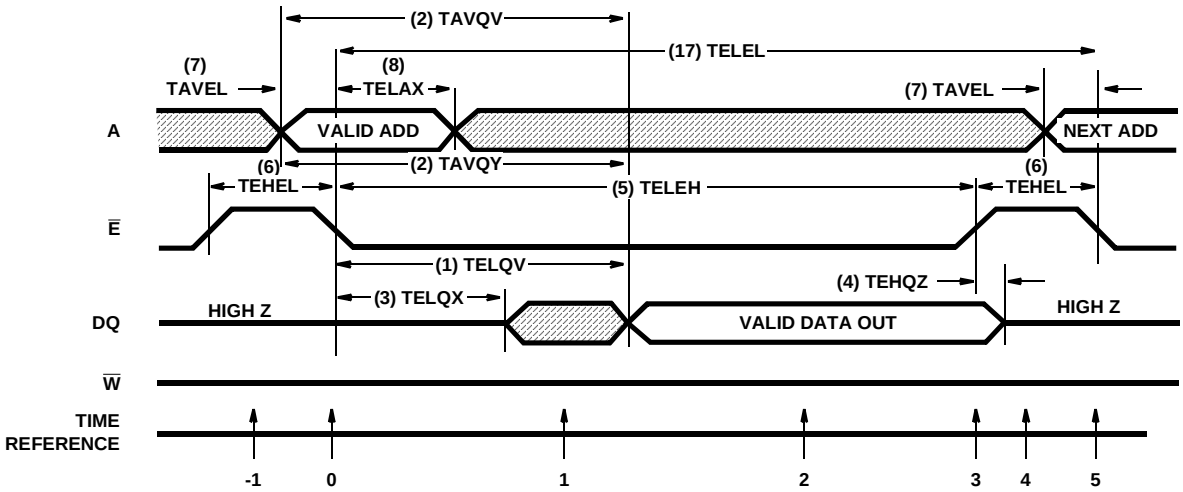


FIGURE 1. READ CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			DATA I/O DQ	FUNCTION
	$\overline{E}$	$\overline{W}$	A		
-1	H	X	X	Z	Memory Disabled
0	↘	H	V	Z	Cycle Begins, Addresses are Latched
1	L	H	X	X	Output Enabled
2	L	H	X	V	Output Valid
3	↗	H	X	V	Read Accomplished
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↘	H	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The address information is latched in the on-chip registers on the falling edge of $\overline{E}$ (T = 0). Minimum address set up and hold time requirements must be met. After the required hold time, the addresses may change state without affecting device operation. During time (T = 1) the output becomes enabled but data is not valid until during time (T = 2). $\overline{W}$ must remain high throughout the read cycle. After the output data has been read, $\overline{E}$ may return high (T = 3). This will disable the output buffer and all inputs, and ready the RAM for the next memory cycle (T = 4).

Timing Waveforms (Continued)

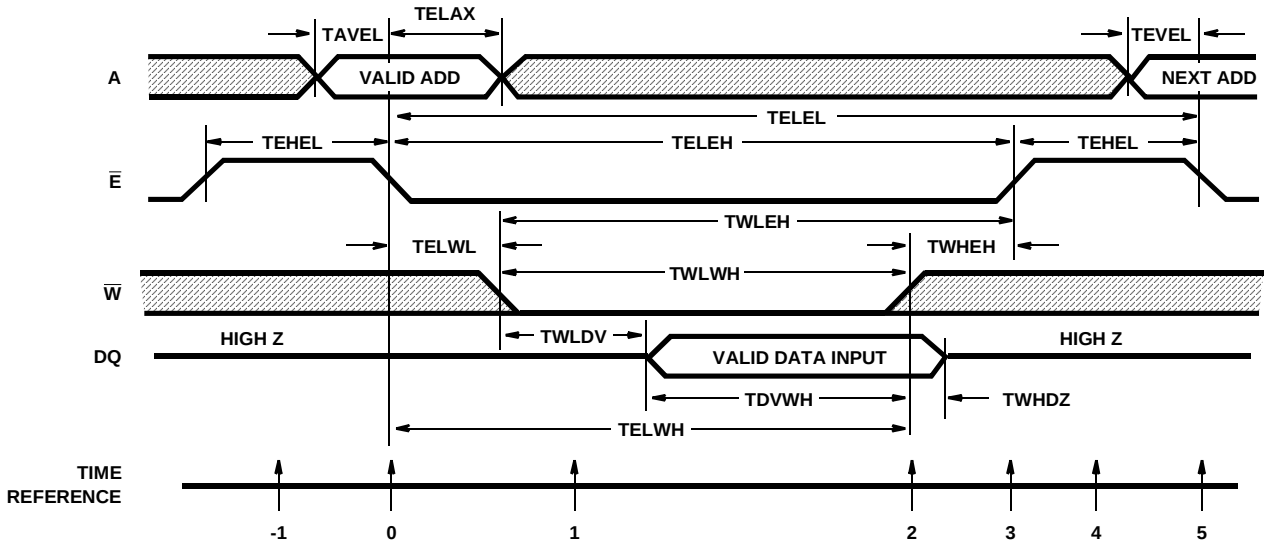


FIGURE 2. WRITE CYCLE

TRUTH TABLE

TIME REFERENCE	INPUTS			DQ	FUNCTION
	$\overline{E}$	$\overline{W}$	A		
-1	H	X	X	Z	Memory Disabled
0	↓	X	V	Z	Cycle Begins, Addresses are Latched
1	L	L	X	Z	Write Period Begins
2	L	↑	X	V	Data In is Written
3	↑	H	X	Z	Write Completed
4	H	X	X	Z	Prepare for Next Cycle (Same as -1)
5	↓	X	V	Z	Cycle Ends, Next Cycle Begins (Same as 0)

The write cycle is initiated by the falling edge of $\overline{E}$ (T = 0), which latches the address information in the on-chip registers. There are two basic types of write cycles, which differ in the control of the common data-in/data-out bus.

Case 1: $\overline{E}$ falls before $\overline{W}$ falls

The output buffers may become enabled (reading) if $\overline{E}$ falls before $\overline{W}$ falls. $\overline{W}$ is used to disable (three-state) the outputs so input data can be applied. TWLDV must be met to allow the $\overline{W}$ signal time to disable the outputs before applying input data. Also, at the end of the cycle the outputs may become active if $\overline{W}$ rises before $\overline{E}$. The RAM outputs and all inputs will three-state after $\overline{E}$ rises (TEHQZ). In this type of write cycle TWLEL and TEHWH may be ignored.

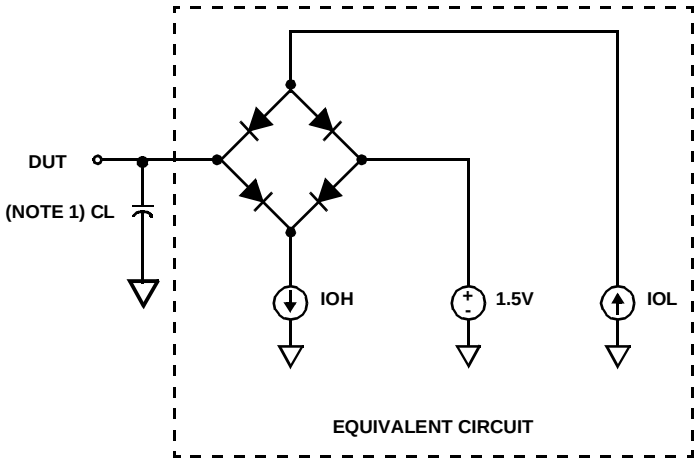
Case 2: $\overline{E}$ falls equal to or after $\overline{W}$ falls, and $\overline{E}$ rises before or equal to $\overline{W}$ rising

This $\overline{E}$ and $\overline{W}$ control timing will guarantee that the data outputs will stay disabled throughout the cycle, thus simplifying the data input timing. TWLEL and TEHWH must be met, but TWLDV becomes meaningless and can be ignored. In this cycle TDVWH and TWHDX become TDVEH and TEHDX. In other words, reference data setup and hold times to the $\overline{E}$ rising edge.

	IF	OBSERVE	IGNORE
Case 1	$\overline{E}$ falls before $\overline{W}$	TWLDV	TWLEL
Case 2	$\overline{E}$ falls after $\overline{W}$ and $\overline{E}$ rises before $\overline{W}$	TWLEL TEHWH	TWLDV TWHDX

If a series of consecutive write cycles are to be performed, $\overline{W}$ may be held low until all desired locations have been written (an extension of Case 2).

Test Load Circuit

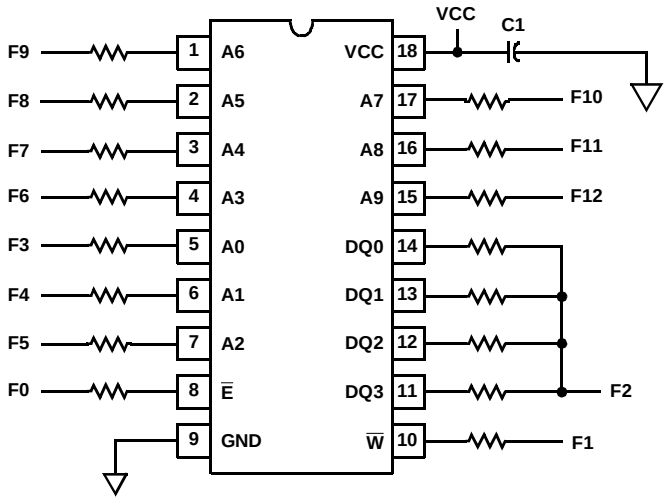


NOTE:

1. Test head capacitance.

Burn-In Circuit

HM6514/883 CERDIP



NOTES:

All resistors 47kΩ ±5%.

F0 = 100kHz ±10%.

F1 = F0 ÷ 2, F2 = F1 ÷ 2, F3 = F2 ÷ 2 . . . F12 = F11 ÷ 2.

VCC = 5.5V ±0.5V.

VIH = 4.5V ±10%.

VIL = -0.2V to +0.4V.

C1 = 0.01µF Min.

Die Characteristics

DIE DIMENSIONS:
136 x 167 x 19 ±1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ±2kÅ

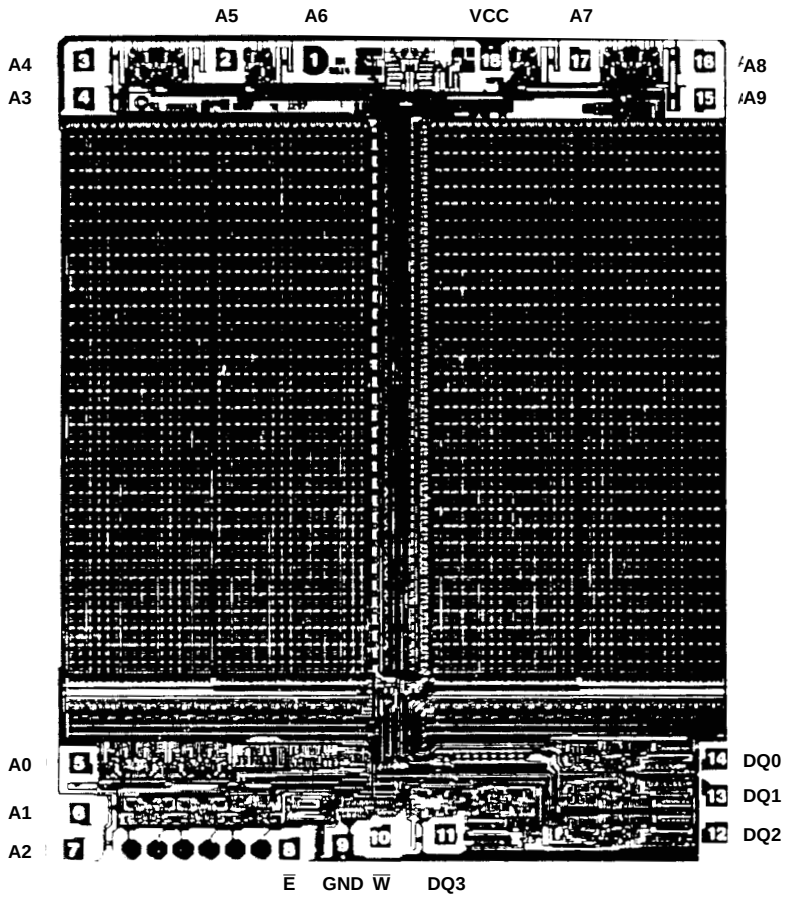
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

WORST CASE CURRENT DENSITY:
1.79×10^5 A/cm^2

LEAD TEMPERATURE (10s soldering):
300^{o}C

Metallization Mask Layout

HM-6514/883



NOTE:

1. Pin numbers correspond to DIP Package only.