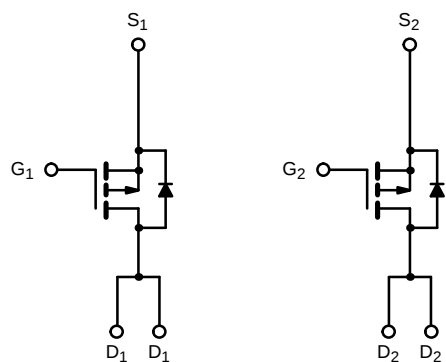
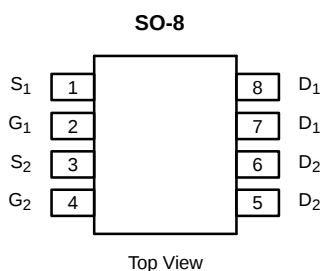




Dual P-Channel 20-V (D-S) MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-20	0.25 @ $V_{GS} = -10$ V	± 2.3
	0.40 @ $V_{GS} = -4.5$ V	± 1.5



P-Channel MOSFET

P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)				
Parameter		Symbol	Limit	Unit
Drain-Source Voltage		V _{DS}	−20	V
Gate-Source Voltage		V _{GS}	± 20	
Continuous Drain Current (T _J = 150°C) ^a	T _A = 25°C	I _D	± 2.3	A
	T _A = 70°C		± 1.8	
Pulsed Drain Current		I _{DM}	± 10	
Continuous Source Current (Diode Conduction) ^a		I _S	−1.7	
Maximum Power Dissipation ^a	T _A = 25°C	P _D	2.0	W
	T _A = 70°C		1.3	
Operating Junction and Storage Temperature Range		T _J , T _{stg}	−55 to 150	°C

THERMAL RESISTANCE RATINGS			
Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	62.5	$^\circ\text{C/W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

For SPICE model information via the Worldwide Web: <http://www.vishay.com/www/product/spice.htm>

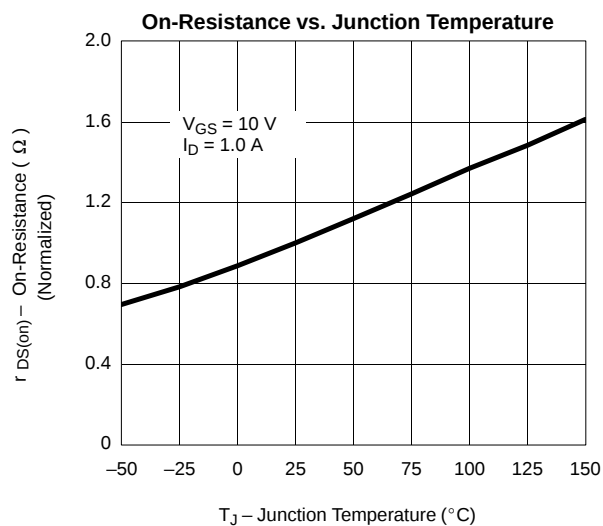
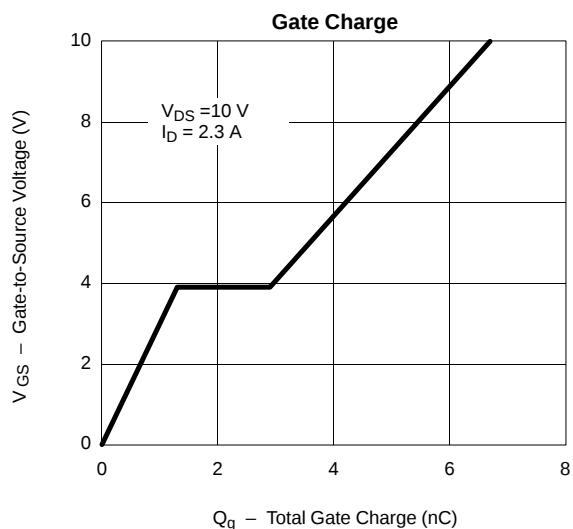
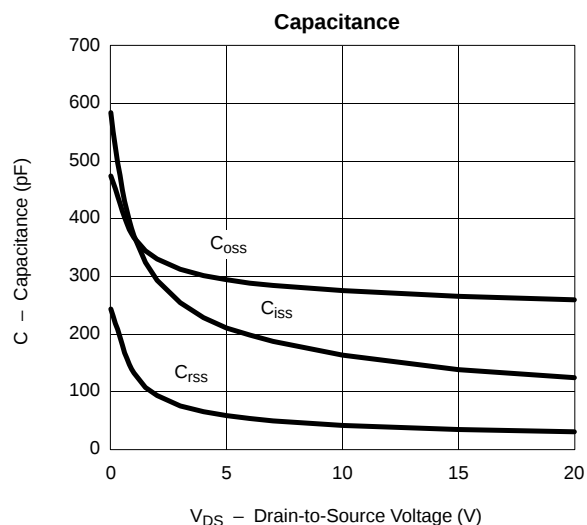
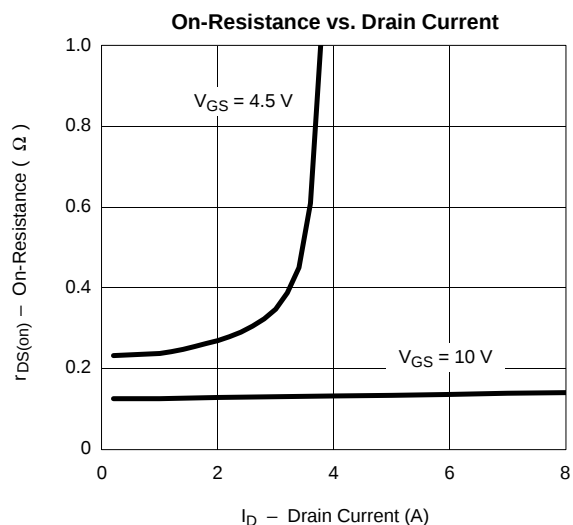
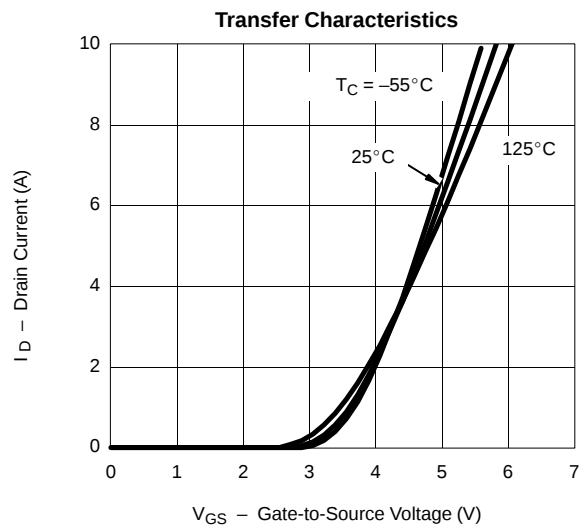
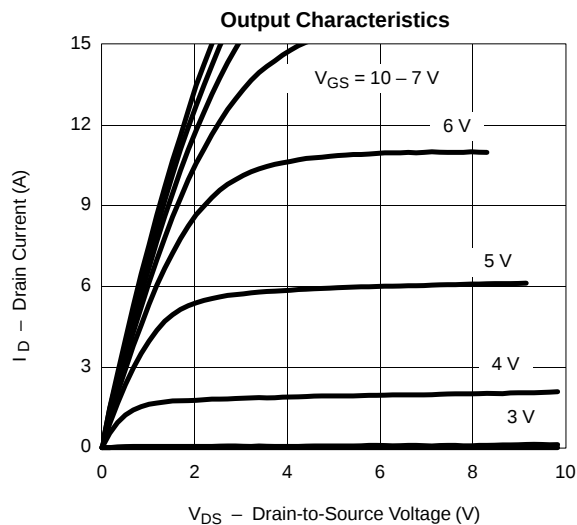
SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED)						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = -250 μA	-1.0			V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = -16 V, V _{GS} = 0 V			-2	μA
		V _{DS} = -16 V, V _{GS} = 0 V, T _J = 55°C			-25	
On-State Drain Current ^b	I _{D(on)}	V _{DS} ≤ -5 V, V _{GS} = -10 V	-10			A
		V _{DS} ≤ -5 V, V _{GS} = -4.5 V	-1.5			
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = -10 V, I _D = 1 A		0.12	0.25	Ω
		V _{GS} = -4.5 V, I _D = 0.5 A		0.22	0.40	
Forward Transconductance ^b	g _{fs}	V _{DS} = -15 V, I _D = -2.3 A		2.5		S
Diode Forward Voltage ^b	V _{SD}	I _S = -1.7 A, V _{GS} = 0 V		-0.8	-1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = -10 V, V _{GS} = -10 V, I _D = -2.3 A		6.7	25	nC
Gate-Source Charge	Q _{gs}			1.3		
Gate-Drain Charge	Q _{gd}			1.6		
Turn-On Delay Time	t _{d(on)}	V _{DD} = -10 V, R _L = 10 Ω I _D ≅ -1 A, V _{GEN} = -10 V, R _G = 6 Ω		10	40	ns
Rise Time	t _r			12	40	
Turn-Off Delay Time	t _{d(off)}			20	90	
Fall Time	t _f			10	50	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs		70	100	

Notes

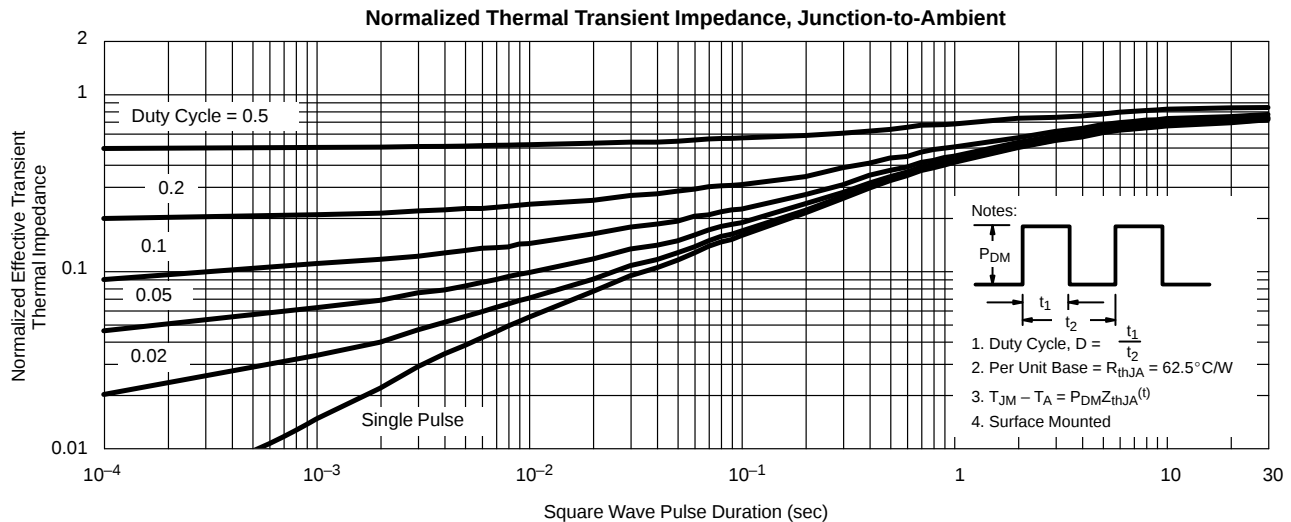
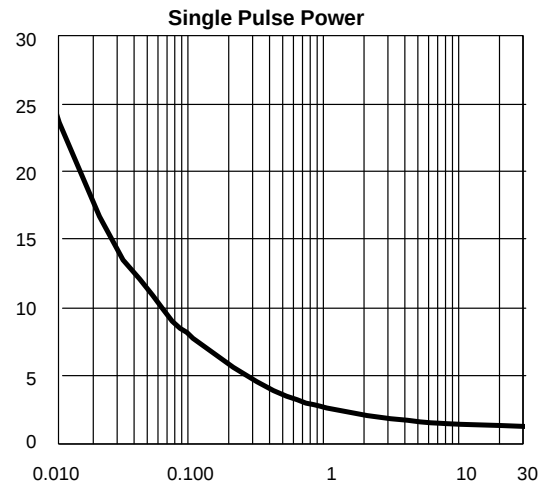
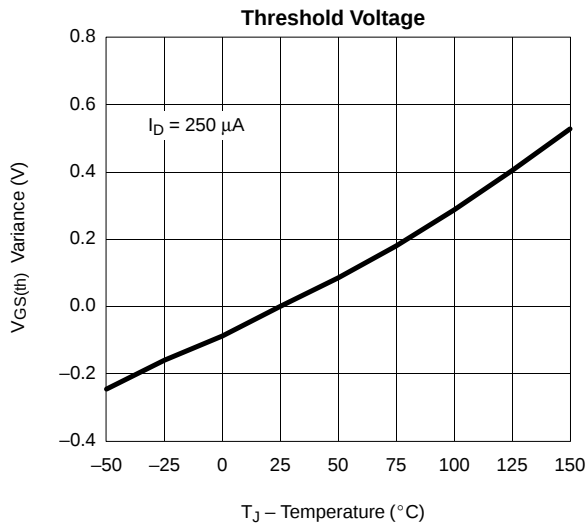
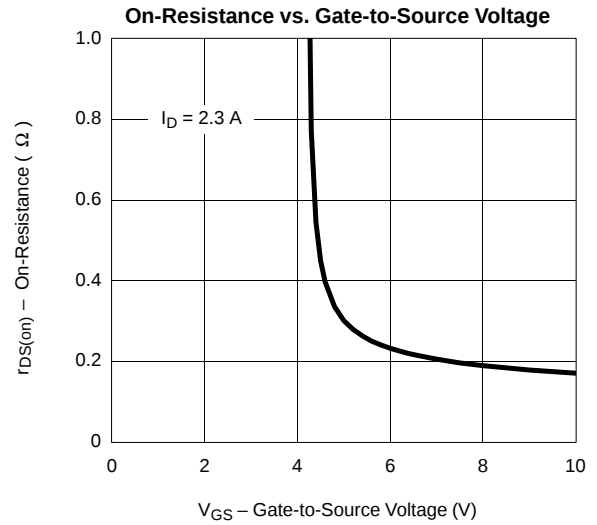
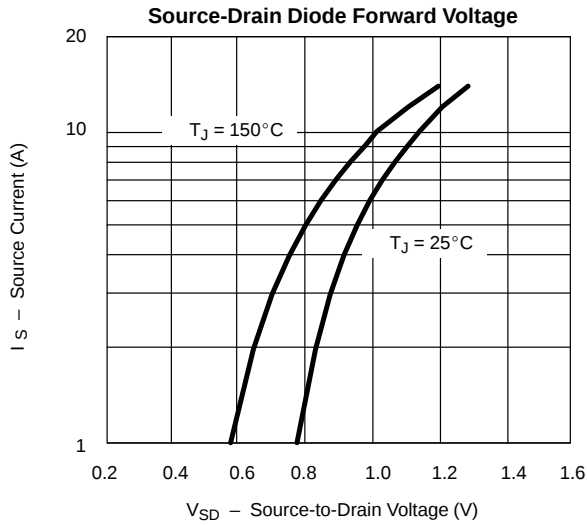
- a. Guaranteed by design, not subject to production testing.
b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)



TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)





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