Low Distortion, Dual High Speed Rail-to-Rail Input/Output Amplifier

Preliminary Technical Data — AD8028

FEATURES

High Speed
- 190 MHz, –3 dB bandwidth (G = +1)
- 100 V/µs slew rate

Low distortion
- 120 dBc @ 1 MHz SFDR
- 80 dBc @ 5 MHz SFDR
- Selectable input crossover threshold

Low noise
- 4.3 nV/√Hz
- 1.6 pA/√Hz

Low offset voltage: 900 µV max

Low power
- 6 mA/amplifier supply current
- Power-down disable feature

No phase reversal

Wide supply range: 2.7 V to 12 V

Small packaging: SOIC-8, µSOIC-10

APPLICATIONS

Filters

ADC drivers

Level shifting

Buffering

Professional video

Low voltage instrumentation

GENERAL DESCRIPTION

The AD8028 is a high speed amplifier with rail-to-rail input and output that operates on low supply voltages and is optimized for high performance and wide dynamic signal range. The AD8028 has low noise (4.3 nV/√Hz, 1.6 pA/√Hz) and low distortion. In applications that use a fraction of or the entire input dynamic range and require low distortion, the AD8028 is an ideal choice.

Many rail-to-rail input amplifiers have an input stage that switches from one differential pair to another as the input signal crosses a threshold voltage, which causes distortion. The AD8028 has a unique feature that allows the user to select the input crossover threshold voltage through the SELECT pin. This feature controls the voltage at which the complementary transistor input pairs switch. The AD8028 also has intrinsically low crossover distortion.

CONNECTION DIAGRAMS

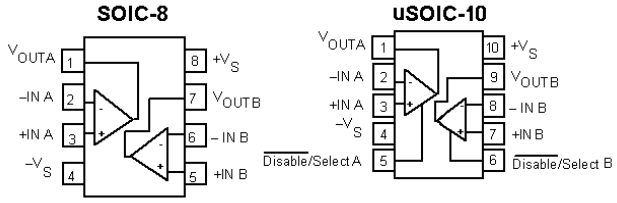

Figure 1. Connection Diagrams (Top View)

With its wide supply voltage range (2.7 V to 12 V) and wide bandwidth (190 MHz), the AD8028 amplifier is designed to work in a variety of applications where speed and performance are needed on low supply voltages. The high performance of the AD8028 is achieved with a quiescent current of only 8.5 mA/amplifier maximum. The AD8028 has a shut down mode that is controlled via the SELECT pin.

The AD8028 is available in SOIC-8 and µSOIC-10 packages. They are rated to work over the industrial temperature range of –40°C to +125°C.

The single version of the AD8028 the **AD8027 is released**.

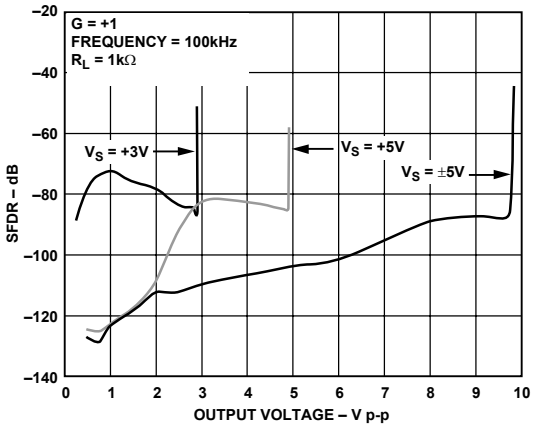

Figure 2. SFDR vs. Output Amplitude

REV.PrA

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 **www.analog.com**
Fax: 781.326.8703

TABLE OF CONTENTS

REVISION HISTORY

Revision 0: Initial Version

AD8028—SPECIFICATIONS

Table 1. V_S = ±5 V (@ T_A = 25°C, R_L = 1 kΩ to midsupply, G = +1, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O= 0.2 V p-p	138	190		MHz
	G = +1, V_O = 2 V p-p	20	32		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		16		MHz
Slew Rate	G = +1, V_O = 2 V Step / G = –1, V_O = 2 V Step		90/100		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		35		ns
NOISE/DISTORTION PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	f_C = 1 MHz, V_O = 2 V p-p, R_F= 24.9 Ω		120		dBc
	f_C = 5 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		80		dBc
Input Voltage Noise	f = 100 kHz		4.3		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.10		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.20		Degree
Crosstalk, Output to Output	G = 1, RL=100, Vout = 2Vpp, Vs = ±5V @1MHz		-93		dB
DC PERFORMANCE					
Input Offset Voltage	SELECT = Tri-State or Open, PNP Active		200	800	µV
	SELECT = High NPN Active		240	900	µV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.50		µV/°C
Input Bias Current[1]	V_{CM} = 0 V, NPN Active		3.80	5.50	µA
	T_{MIN} to T_{MAX}		4		µA
Input Bias Current[1]	V_{CM} = 0 V, PNP Active		–7.8	–10.5	µA
	T_{MIN} to T_{MAX}		–8		µA
Input Offset Current			±0.1	±0.9	µA
Open-Loop Gain	V_O = ±2.5 V		108		dB
INPUT CHARACTERISTICS					
Input Impedance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			–5.2 to +5.2		V
Common-Mode Rejection Ratio	V_{CM} = ±2.5 V	90	105		dB
SELECT PIN					
Crossover Low—Selection Input Voltage	Tri-State < ±20 µA		–3.3 to +5		V
Crossover High—Selection Input Voltage			–3.9 to –3.3		V
Disable Input Voltage			–5 to –3.9		V
Disable Switching Speed	50% of Input to <10% of Final V_O		980		ns
Enable Switching Speed			45		ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_I = +6 V to –6 V, G = –1		40/45		ns
Output Voltage Swing		$-V_S$ + 0.10		$+V_S$ – 0.10	V
Short Circuit Output	Sinking and Sourcing		120		mA
Off Isolation	V_{IN} = 0.2 V p-p, f = 1 MHz, SELECT = LOW		–49		dB
Capacitive Load Drive	30% Overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			6.5	8.5	mA
Quiescent Current (Disabled)	SELECT = Low		370	500	µA
Power Supply Rejection Ratio	V_S ± 1 V	90	107		dB

[1] No sign or a plus indicates current into pin, minus indicates current out of pin.

AD8028—SPECIFICATIONS

Table 2. V_S = +5 V (@ T_A = 25°C, R_L = 1 kΩ to midsupply, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
−3 dB Bandwidth	G = +1, V_O = 0.2 V p-p	131	185		MHz
	G = +1, V_O = 2 V p-p	18	28		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		12		MHz
Slew Rate	G = +1, V_O = 2 V Step/ G = −1, V_O = 2 V Step		85/100		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		40		ns
NOISE/DISTORTION PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	f_C = 1 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		90		dBc
	f_C = 5 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		64		dBc
Input Voltage Noise	f = 100 kHz		4.3		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.10		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.20		Degree
Crosstalk, Output to Output	G = 1, RL=100, Vout = 2Vpp, Vs = ±5V @1MHz		-92		dB
DC PERFORMANCE					
Input Offset Voltage	SELECT = Tri-State or Open, PNP Active		200	800	µV
	SELECT = High NPN Active		240	900	µV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.5		µV/°C
Input Bias Current[1]	V_{CM} = 2.5 V, NPN Active		3.7	5.5	µA
	T_{MIN} to T_{MAX}		4		µA
Input Bias Current[1]	V_{CM} = 2.5 V, PNP Active		−7.8	−10.5	µA
	T_{MIN} to T_{MAX}		−7.9		µA
Input Offset Current			±0.1	±0.9	µA
Open-Loop Gain	V_O = 1 V to 4 V		105		dB
INPUT CHARACTERISTICS					
Input Impedance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range			−0.2 to +5.2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 2.5 V	90	105		dB
SELECT PIN					
Crossover Low—Selection Input Voltage	Tri-State < ±20 µA		1.7 to 5		V
Crossover High—Selection Input Voltage			1.1 to 1.7		V
Disable Input Voltage			0 to 1.1		V
DISABLE Switching Speed	50% of Input to <10% of Final V_O		1100		ns
Enable Switching Speed			50		ns
OUTPUT CHARACTERISTICS					
Overdrive Recovery Time (Rising/Falling Edge)	V_I = −1 V to +6 V, G = −1		50/50		ns
Output Voltage Swing	R_L = 1 kΩ	$-V_S$ + 0.08		$+V_S$ − 0.08	V
Off Isolation	V_{IN} = 0.2 V p-p, f =1 MHz, SELECT = LOW		−49		dB
Short Circuit Current	Sinking and Sourcing		105		mA
Capacitive Load Drive	30% Overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			6	8.5	mA
Quiescent Current (Disabled)	SELECT = Low		320		µA
Power Supply Rejection Ratio	V_S ± 1 V	90	107		dB

[1] No sign or a plus indicates current into pin, minus indicates current out of pin.

AD8028—SPECIFICATIONS

Table 3. V_S = +3 V (@ T_A = 25°C, R_L = 1 kΩ to midsupply, unless otherwise noted.)

Parameter	Conditions	Min	Typ	Max	Unit
DYNAMIC PERFORMANCE					
–3 dB Bandwidth	G = +1, V_O = 0.2 V p-p	125	180		MHz
	G = +1, V_O = 2 V p-p	19	29		MHz
Bandwidth for 0.1 dB Flatness	G = +2, V_O = 0.2 V p-p		10		MHz
Slew Rate	G = +1, V_O = 2 V Step / G = –1, V_O = 2 V Step		73/100		V/µs
Settling Time to 0.1%	G = +2, V_O = 2 V Step		48		ns
NOISE/DISTORTION PERFORMANCE					
Spurious Free Dynamic Range (SFDR)	f_C = 1 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		85		dBc
	f_C = 5 MHz, V_O = 2 V p-p, R_F = 24.9 Ω		64		dBc
Input Voltage Noise	f = 100 kHz		4.3		nV/√Hz
Input Current Noise	f = 100 kHz		1.6		pA/√Hz
Differential Gain Error	NTSC, G = +2, R_L = 150 Ω		0.15		%
Differential Phase Error	NTSC, G = +2, R_L = 150 Ω		0.20		Degree
Crosstalk, Output to Output	G = 1, RL=100, Vout = 2Vpp, Vs = 3V @1MHz		-89		dB
DC PERFORMANCE					
Input Offset Voltage	SELECT = Tri-State or Open, PNP Active		200	800	µV
	SELECT = High NPN Active		240	900	µV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}		1.5		µV/°C
Input Bias Current[1]	V_{CM} = 1.5 V, NPN Active		3.5	5.5	µA
	T_{MIN} to T_{MAX}		3.8		µA
Input Bias Current[1]	V_{CM} = 1.5 V, PNP Active		–7. 5	–10.5	µA
	T_{MIN} to T_{MAX}		–7.7		µA
Input Offset Current			±0.1	±0.9	µA
Open-Loop Gain	V_O = 1 V to 2 V		100		dB
INPUT CHARACTERISTICS					
Input Impedance			6		MΩ
Input Capacitance			2		pF
Input Common-Mode Voltage Range	R_L = 1 kΩ		–0.2 to +3.2		V
Common-Mode Rejection Ratio	V_{CM} = 0 V to 1.5 V	88	100		dB
SELECT PIN					
Crossover Low—Selection Input Voltage	Tri-State < ±20 µA		1.7 to 3		V
Crossover High—Selection Input Voltage			1.1 to 1.7		V
Disable Input Voltage			0 to 1.1		V
DISABLE Switching Speed	50% of Input to <10% of Final V_O		1150		ns
Enable Switching Speed			50		ns
OUTPUT CHARACTERISTICS					
Output Overdrive Recovery Time (Rising/Falling Edge)	V_I = –1 V to +4 V, G = –1		55/55		ns
Output Voltage Swing	R_L = 1 kΩ	$-V_S$ + 0.07		$+V_S$ – 0.07	V
Short Circuit Current	Sinking and Sourcing		72		mA
Off Isolation	V_{IN} = 0.2 V p-p, f = 1 MHz, SELECT = LOW		–49		dB
Capacitive Load Drive	30% Overshoot		20		pF
POWER SUPPLY					
Operating Range		2.7		12	V
Quiescent Current			6.0	8.0	mA
Quiescent Current (Disabled)	SELECT = Low		300	420	µA
Power Supply Rejection Ratio	V_S ± 1 V	88	100		dB

[1] No sign or a plus indicates current into pin, minus indicates current out of pin.

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	12.6 V
Power Dissipation	See Figure 3
Common-Mode Input Voltage	$\pm V_S \pm 0.5$ V
Differential Input Voltage	±1.8 V
Storage Temperature	–65°C to +125°C
Operating Temperature Range	–40°C to +125°C
Lead Temperature Range (Soldering 10 sec)	300°C
Junction Temperature	150°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Maximum Power Dissipation

The maximum safe power dissipation in the AD8028 package is limited by the associated rise in junction temperature (T_J) on the die. The plastic encapsulating the die will locally reach the junction temperature. At approximately 150°C, which is the glass transition temperature, the plastic will change its properties. Even temporarily exceeding this temperature limit may change the stresses that the package exerts on the die, permanently shifting the parametric performance of the AD8028. Exceeding a junction temperature of 175°C for an extended period of time can result in changes in the silicon devices, potentially causing failure.

The still-air thermal properties of the package and PCB (θ_{JA}), ambient temperature (T_A), and the total power dissipated in the package (P_D) determine the junction temperature of the die. The junction temperature can be calculated as:

$$T_J = T_A + (P_D \times \theta_{JA})$$

The power dissipated in the package (P_D) is the sum of the quiescent power dissipation and the power dissipated in the package due to the load drive for all outputs. The quiescent power is the voltage between the supply pins (V_S) times the quiescent current (I_S). Assuming the load (R_L) is referenced to midsupply, then the total drive power is $V_S/2 \times I_{OUT}$, some of which is dissipated in the package and some in the load ($V_{OUT} \times I_{OUT}$). The difference between the total drive power and the load power is the drive power dissipated in the package.

$$P_D = Quiescent\ Power + (Total\ Drive\ Power - Load\ Power)$$

$$P_D = (V_S \times I_S) + \left(\frac{V_S}{2} \times \frac{V_{OUT}}{R_L}\right) - \frac{{V_{OUT}}^2}{R_L}$$

RMS output voltages should be considered. If R_L is referenced to V_{S-}, as in single-supply operation, then the total drive power is $V_S \times I_{OUT}$.

If the rms signal levels are indeterminate, then consider the worst case, when $V_{OUT} = V_S/4$ for R_L to midsupply

$$P_D = (V_S \times I_S) + \frac{(V_S/4)^2}{R_L}$$

In single-supply operation with R_L referenced to V_{S-}, worst case is $V_{OUT} = V_S/2$.

Airflow will increase heat dissipation, effectively reducing θ_{JA}. Also, more metal directly in contact with the package leads from metal traces, through holes, ground, and power planes will reduce the θ_{JA}. Care must be taken to minimize parasitic capacitances at the input leads of high speed op amps as discussed in the board layout section.

Figure 3 shows the maximum safe power dissipation in the package versus the ambient temperature for the SOIC-8 (125°C/W) on a JEDEC standard 4-layer board. θ_{JA} values are approximations.

OUTPUT SHORT CIRCUIT

Shorting the output to ground or drawing excessive current for the AD8028 will likely cause catastrophic failure.

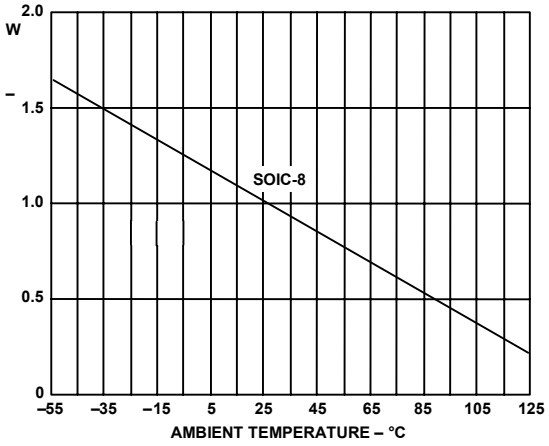

Figure 3. Maximum Power Dissipation

TYPICAL PERFORMANCE CHARACTERISTICS

Default Conditions V_S = +5 V (T_A = +25°C, R_L = 1 kΩ, unless otherwise noted.)

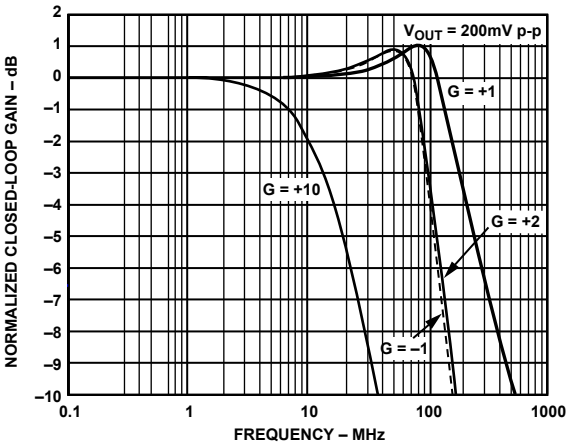

Figure 4. Small Signal Frequency Response for Various Gains

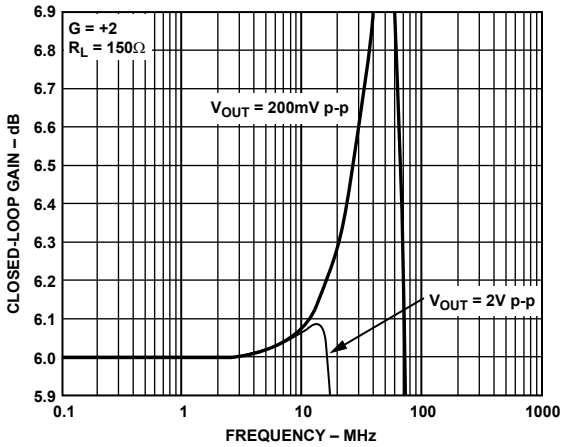

Figure 7. 0.1 dB Flatness Frequency Response

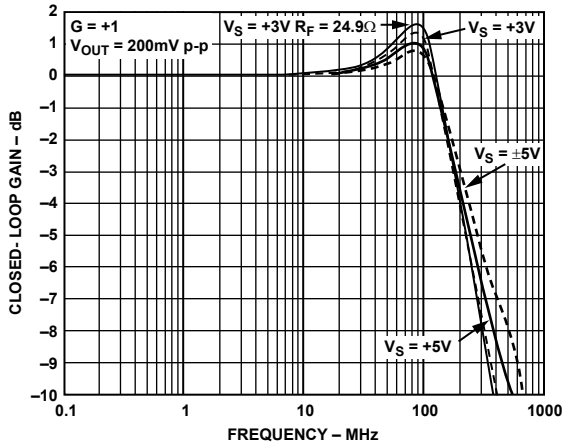

Figure 5. Small Signal Frequency Response for Various Supplies

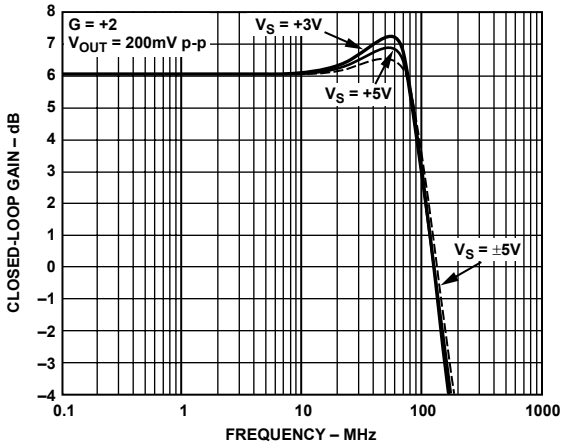

Figure 8. Small Signal Frequency Response for Various Supplies

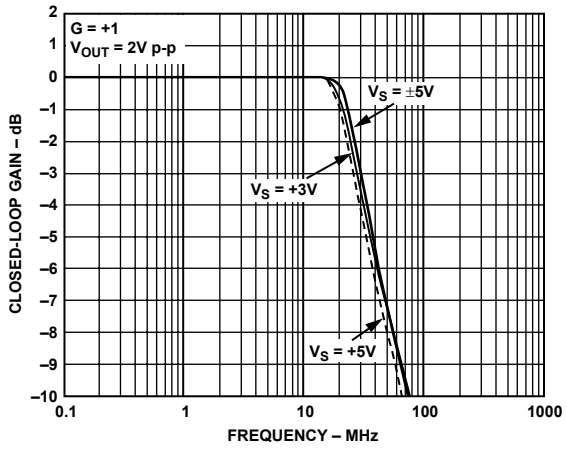

Figure 6. Large Signal Frequency Response for Various Supplies

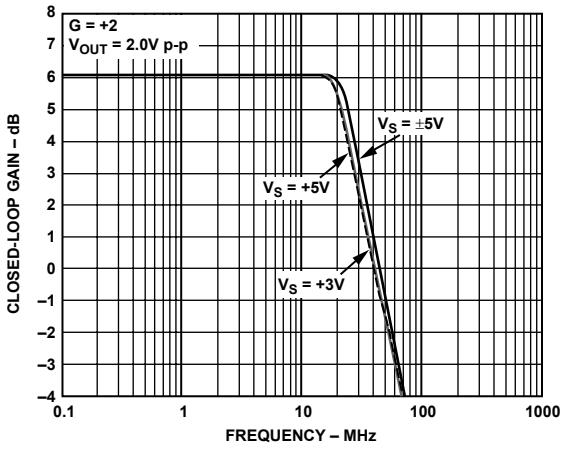

Figure 9. Large Signal Frequency Response for Various Supplies

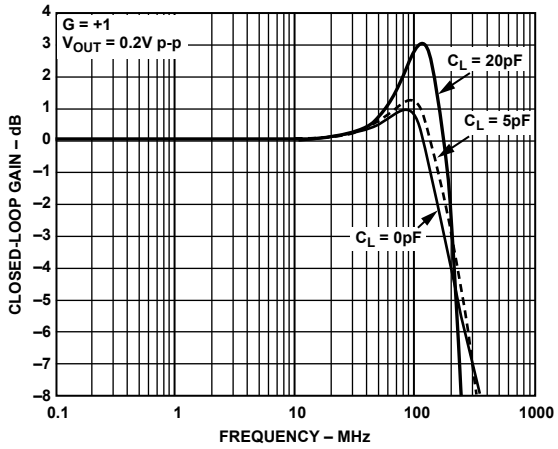

Figure 10. Small Signal Frequency Response for Various C_{LOAD}

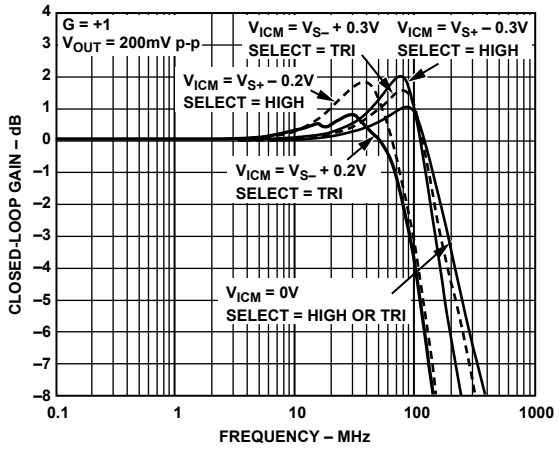

Figure 13. Small Signal Frequency Response for Various Input Common-Mode Votlages

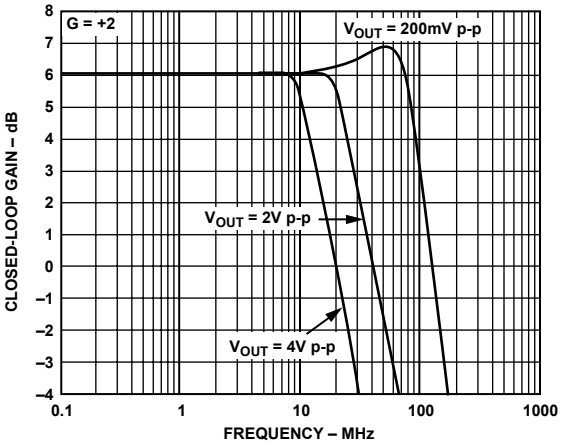

Figure 11. Frequency Response for Various Output Amplitudes

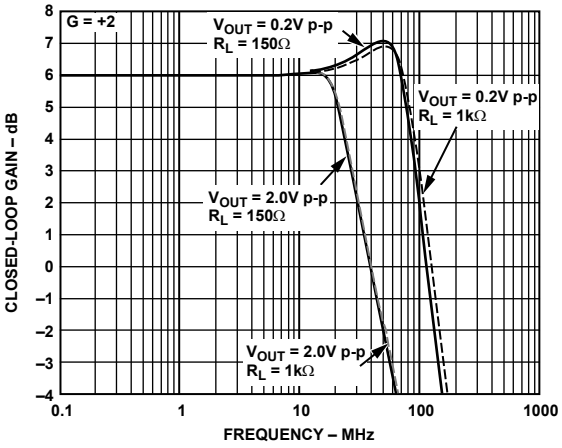

Figure 14. Small Signal Frequency Response for Various R_{LOAD} Values

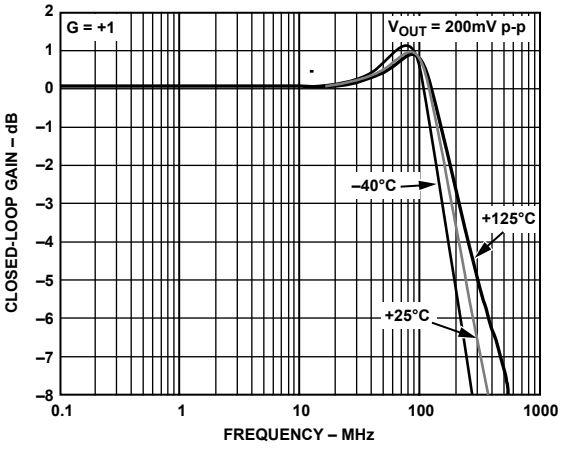

Figure 12. Small Signal Frequency Response vs. Temperature

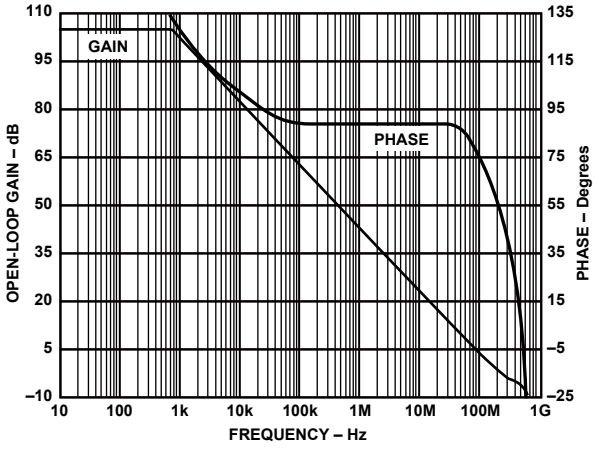

Figure 15. Open-Loop Gain and Phase vs. Frequency

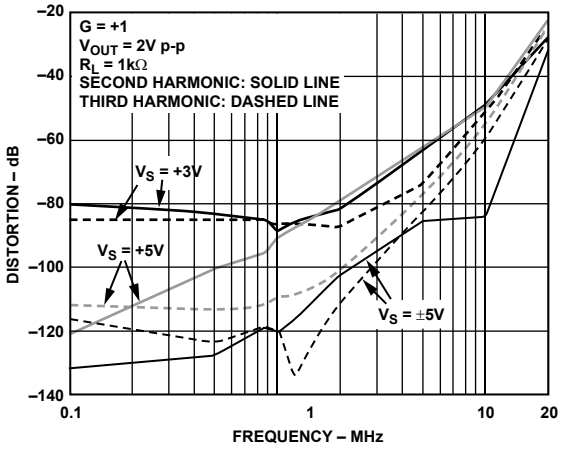

Figure 16. Harmonic Distortion vs. Frequency and Supply Voltage

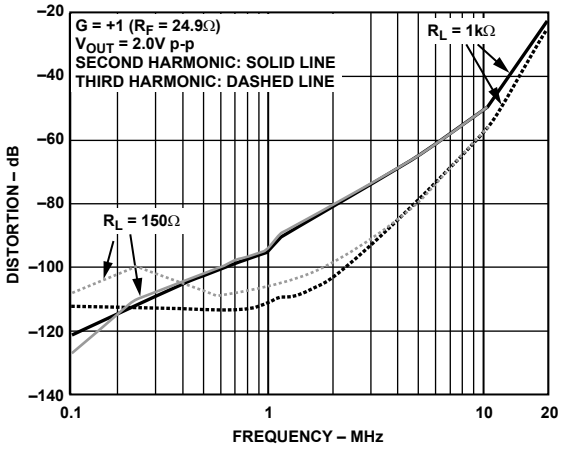

Figure 19. Harmonic Distortion vs. Frequency and Load

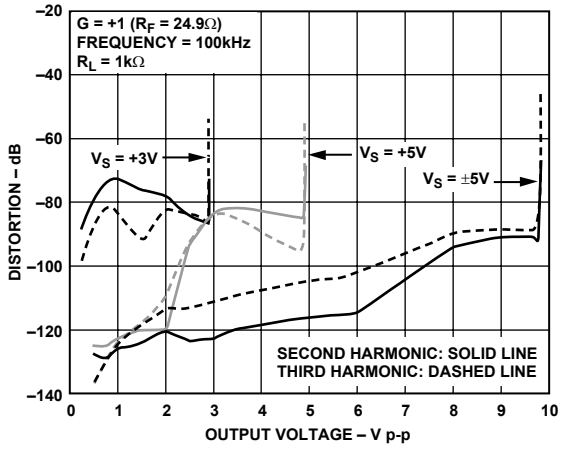

Figure 17. Harmonic Distortion vs. Output Amplitude

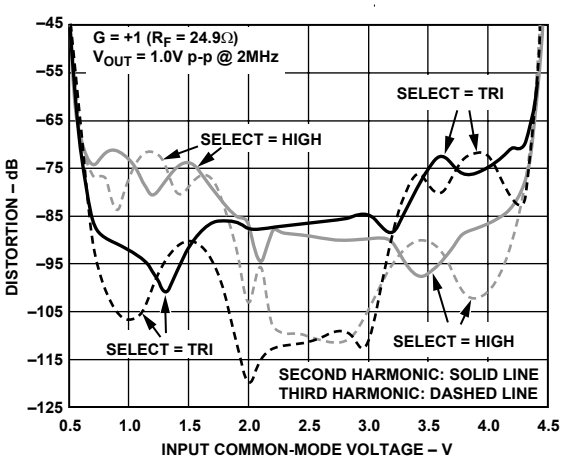

Figure 20. Harmonic Distortion vs. Input Common-Mode Voltage, V_S = +5 V

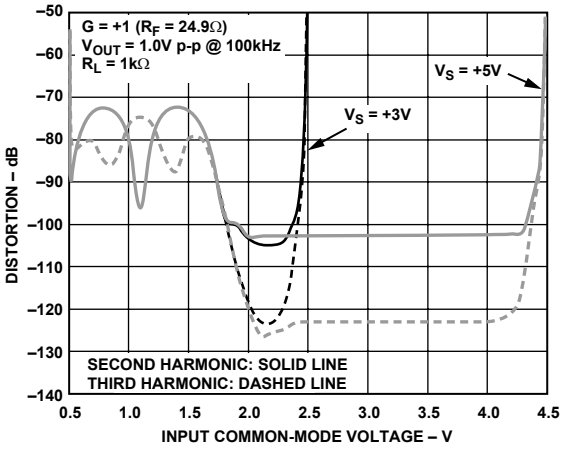

Figure 18. Harmonic Distortion vs. Input Common-Mode Voltage, SELECT = High

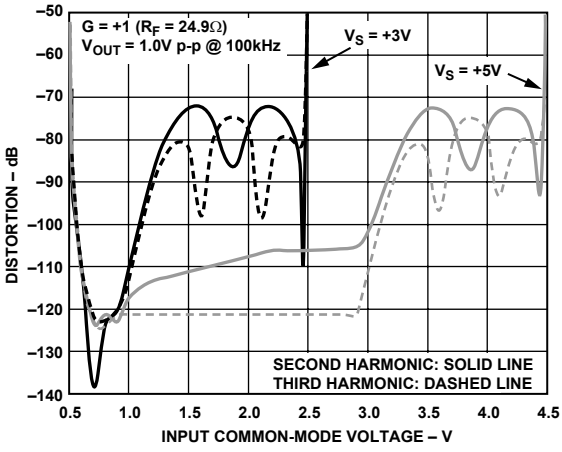

Figure 21. Harmonic Distortion vs. Input Common-Mode Voltage, SELECT = Tri-State or Open

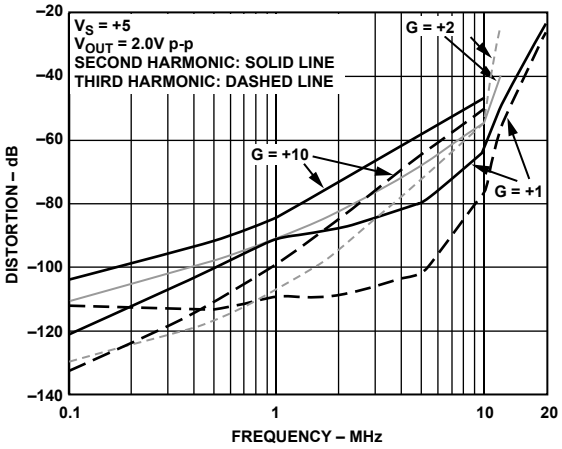

Figure 22. Harmonic Distortion vs. Frequency and Gain

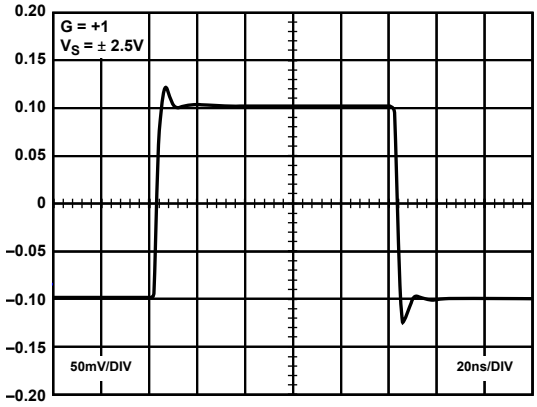

Figure 23. Small Signal Transient Response

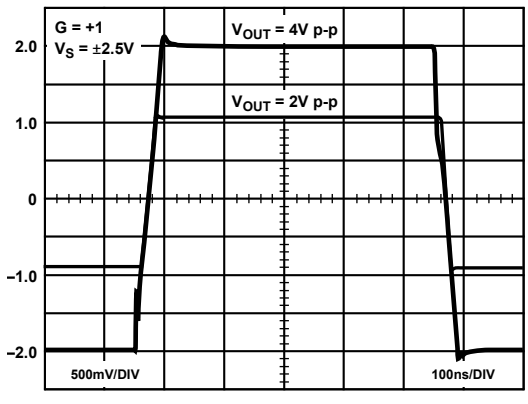

Figure 24. Large Signal Transient Response, G = +1

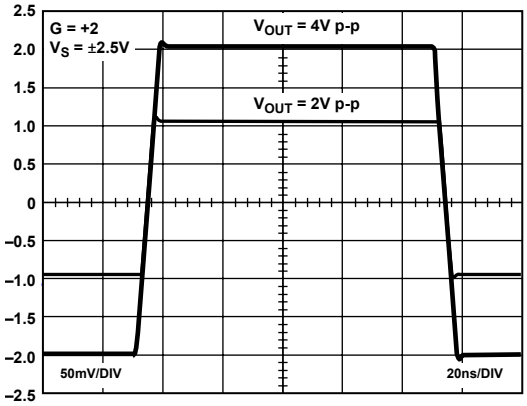

Figure 25. Large Signal Transient Response, G = +2

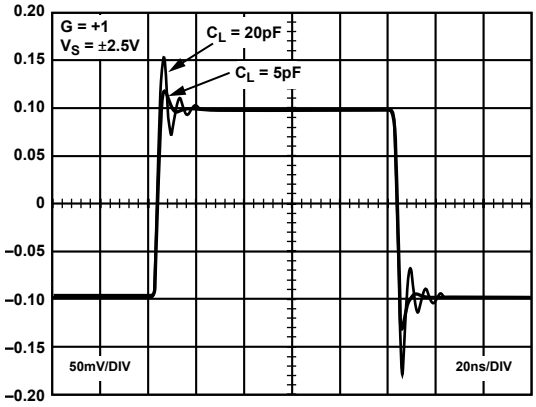

Figure 26. Small Signal Transient Response with Capacitive Load

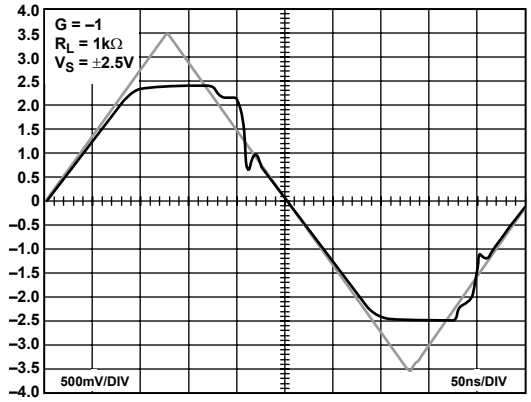

Figure 27. Output Overdrive Recovery

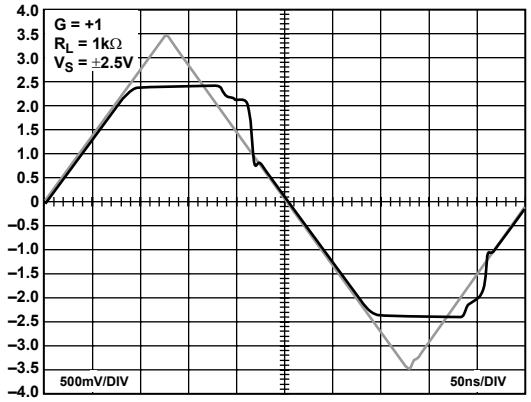

Figure 28. Input Overdrive Recovery

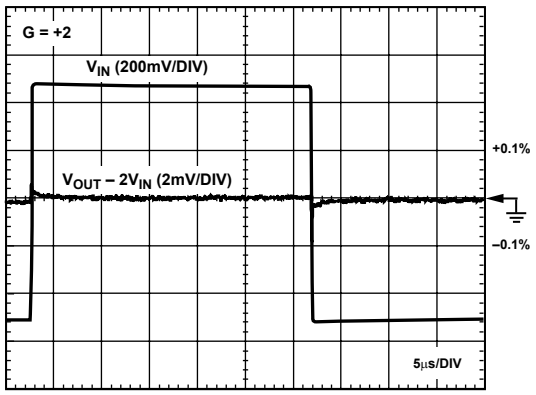

Figure 29. Long-Term Settling Time

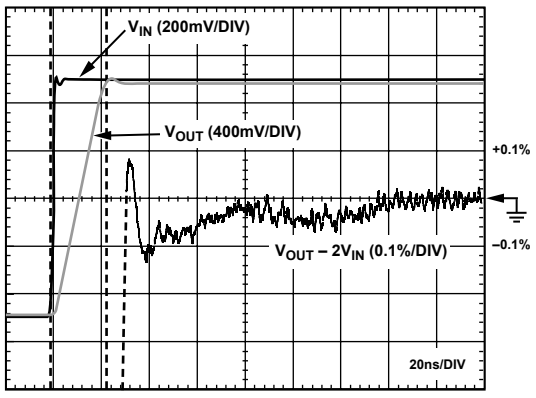

Figure 30. 0.1% Short-Term Settling Time

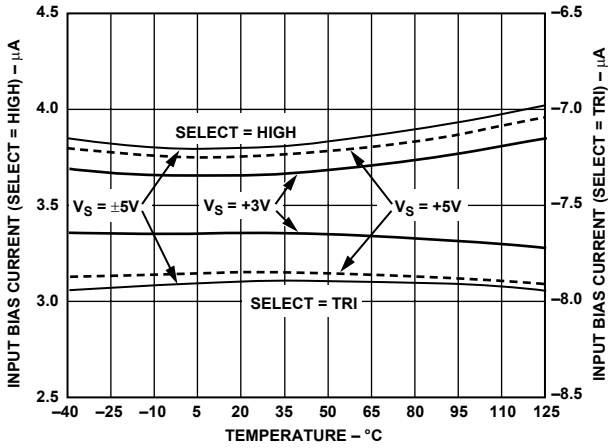

Figure 31. Input Bias Current vs. Temperature

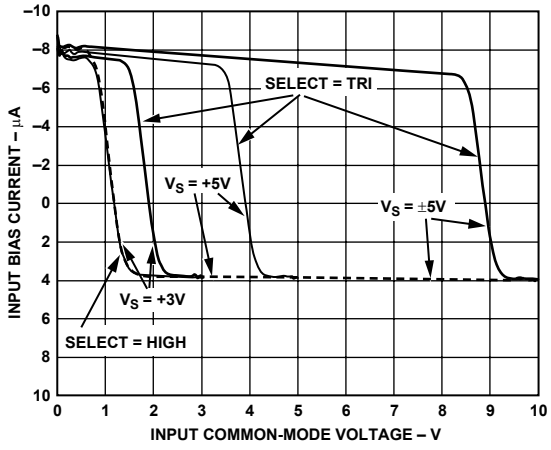

Figure 32. Input Bias Current vs. Input Common-Mode Voltage

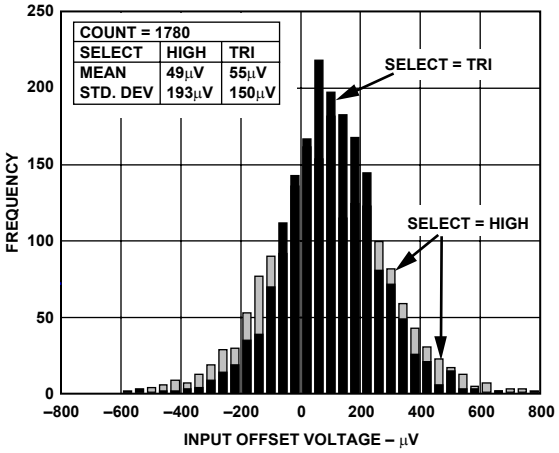

Figure 33. Input Offset Voltage Distribution

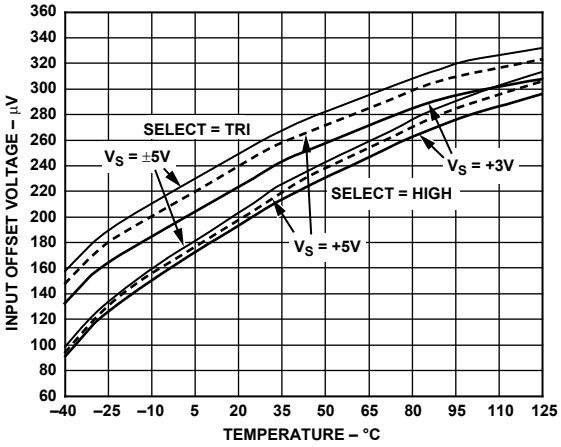

Figure 34. Input Offset Voltage vs. Temperature

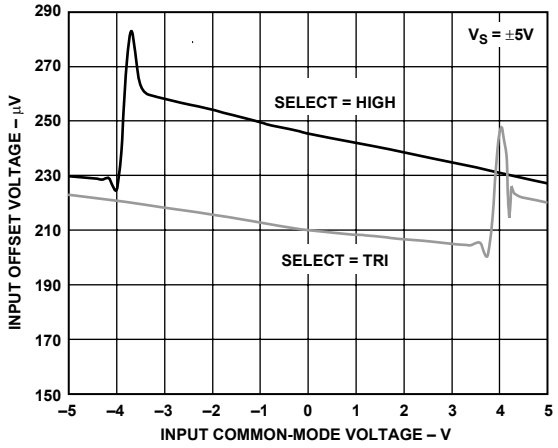

Figure 35. Input Offset Voltage vs. Input Common-Mode Voltage, V_S = ±5

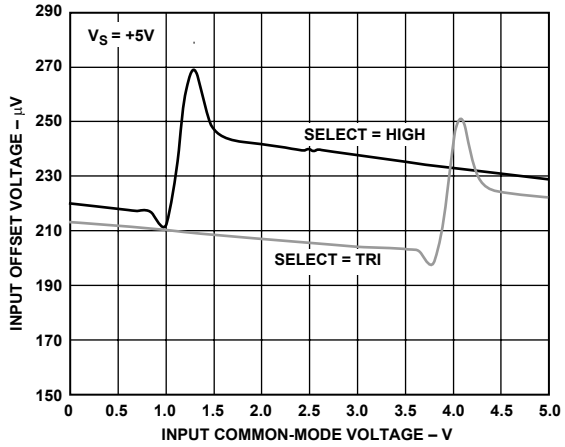

Figure 36. Input Offset Voltage vs. Input Common-Mode Voltage, V_S = +5

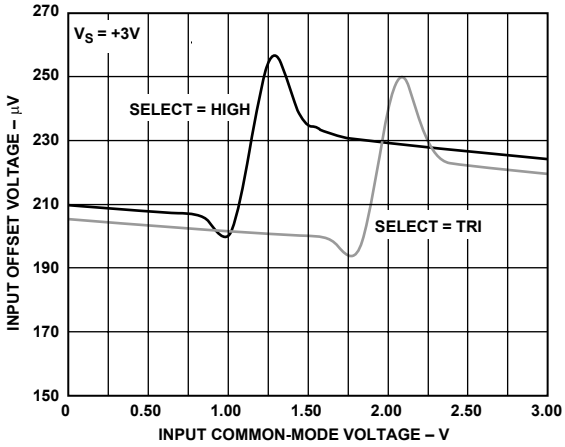

Figure 37. Input Offset Voltage vs. Input Common-Mode Voltage, V_S = +3

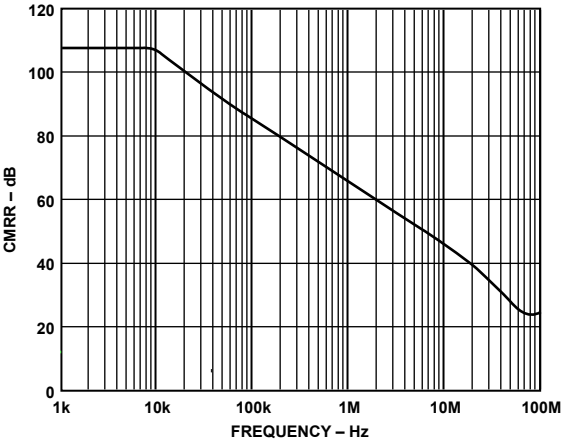

Figure 38. CMRR vs. Frequency

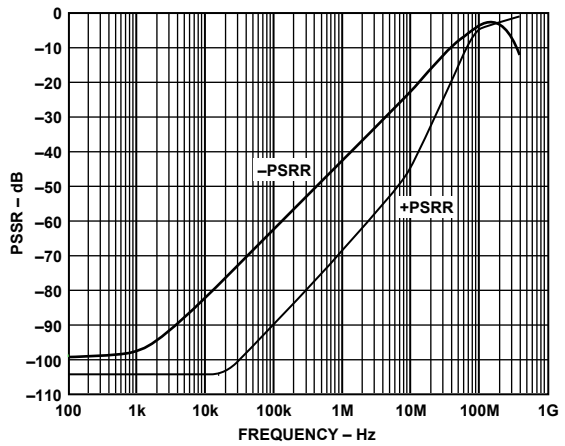

Figure 39. PSRR vs. Frequency

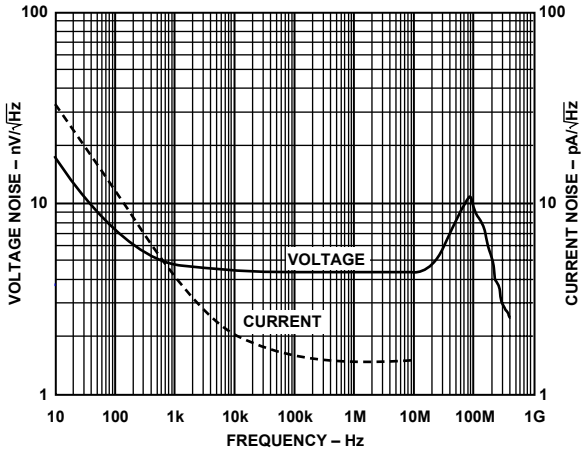

Figure 40. Voltage and Current Noise vs. Frequency

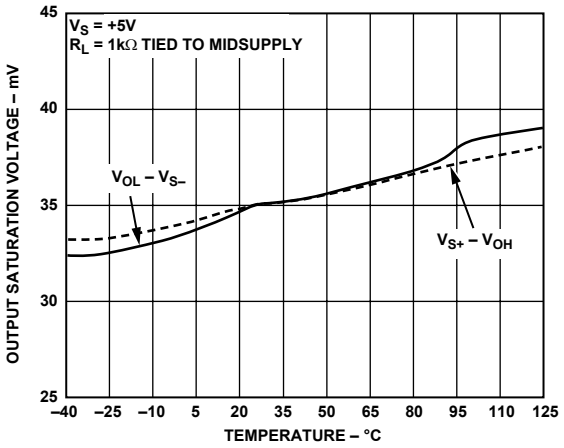

Figure 43. Output Saturation Voltage vs. Temperature

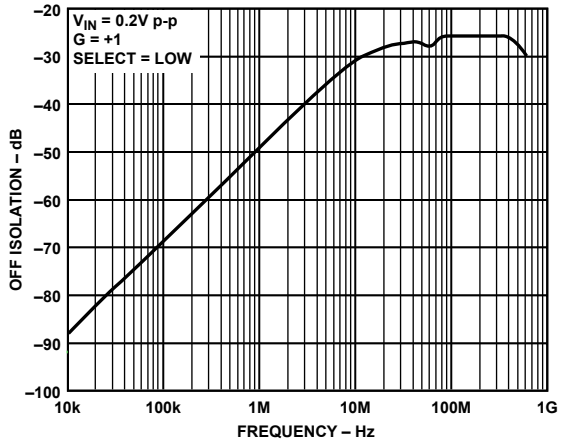

Figure 41. Off Isolation vs. Frequency

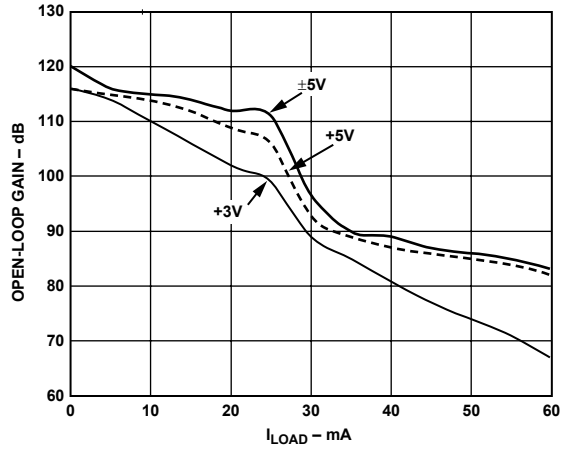

Figure 44. Open-Loop Gain vs. Load Current

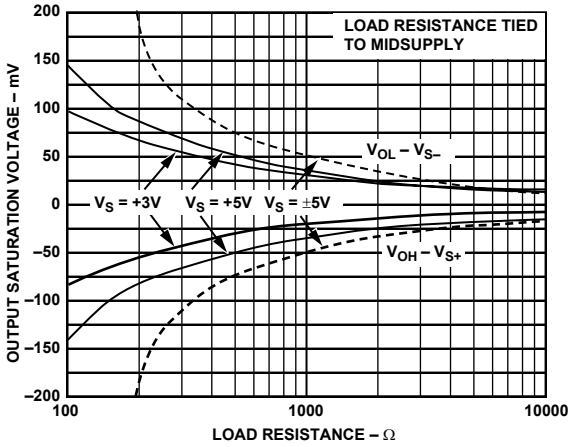

Figure 42. Output Saturation Voltage vs. Output Load

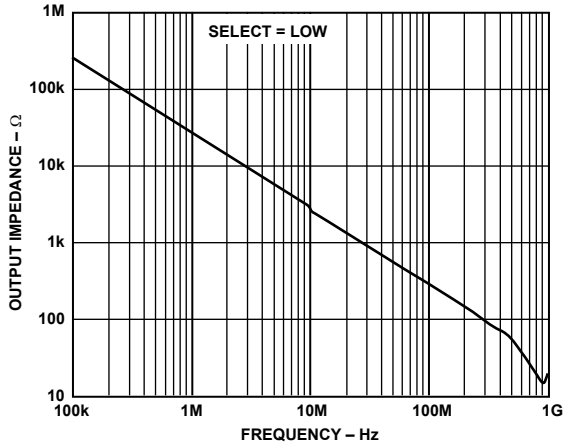

Figure 45. Output Disabled—Impedance vs. Frequency

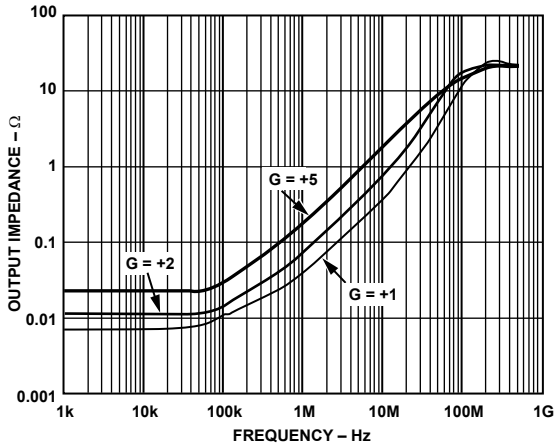

Figure 46. Output Enabled— Impedance vs. Frequency

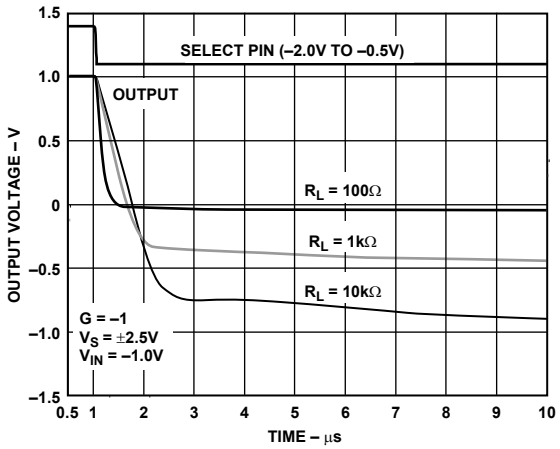

Figure 49. Disable Turn Off Timing

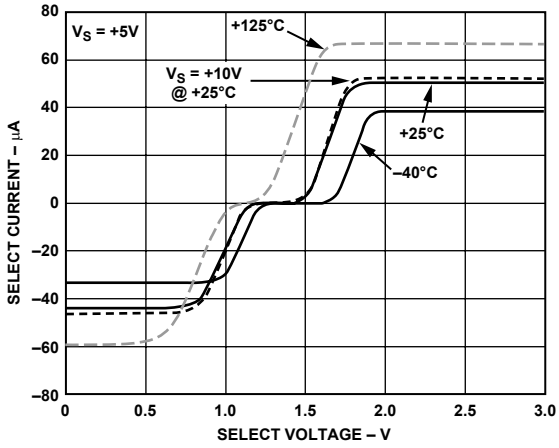

Figure 47. SELECT Pin Current vs. SELECT Pin Voltage and Temperature

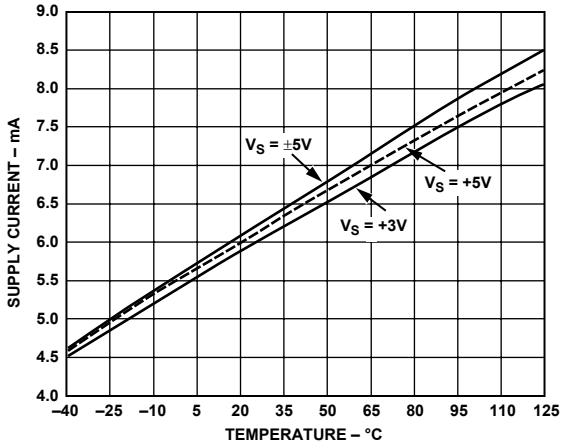

Figure 50. Quiescent Supply Current vs. Supply Voltage and Temperature

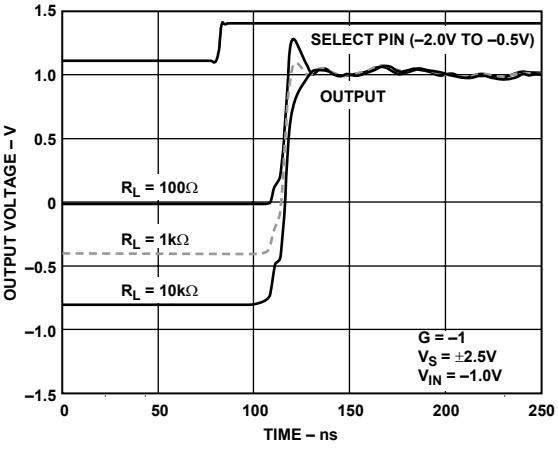

Figure 48. Enable Turn On Timing

THEORY OF OPERATION

The AD8028 is a rail-to-rail input and output amplifier designed in Analog Devices XFCB process. The XFCB process enables the AD8028 to run on 2.7 V to 12 V supplies with 190 MHz of bandwidth and over 100 V/µs of slew rate. The AD8028 has 4.3 nV/√Hz of wideband noise with 17 nV/√Hz noise at 10 Hz. This noise performance, with an offset and drift performance of less than 900 µV maximum and 1.5 µV/°C typical, respectively, makes the AD8028 ideal for high speed precision applications. Additionally, the input stage operates 200 mV beyond the supply rails and shows no phase reversal. The amplifier features over voltage protection on the input stage. Once the inputs exceed the supply rails by 0.7 V, ESD protection diodes will turn on, drawing excessive current through the differential input pins. A series input resistor should be included to limit the input current to less than 10 mA.

Input Stage

The rail-to-rail input performance is achieved by operating complementary input pairs. Which pair is on is determined by the common-mode level of the differential input signal. Looking at the schematic in Figure 51, a tail current (I_{TAIL}) is generated that sources the PNP differential input structure consisting of Q1 and Q2. A reference voltage is generated internally that is connected to the base of Q5. This voltage is continually compared against the common-mode input voltage. When the common-mode level exceeds the internal reference voltage, Q5 diverts the tail current (I_{TAIL}) from the PNP input pair to a current mirror that sources the NPN input pair consisting of Q3 and Q4. The NPN input pair can now operate 200 mV above the positive rail. Both input pairs are protected from differential input signals above 1.4 V by four diodes across the input (see Figure 51). In the event of differential input signals that exceed 1.4 V, the diodes will conduct and excessive current will flow through them. A series input resistor should be included to limit the input current to 10 mA.

Crossover Selection

A new feature available on the AD8028, which is called Crossover Selection, allows the user to choose the crossover point between the PNP/NPN differential pairs. Although the crossover region is small, operating in this region should be avoided since it can introduce offset and distortion to the output signal. To help avoid operating in the crossover region, the AD8028 allows the user to select from two preset crossover locations (i.e., voltage levels) using the SELECT pin. Looking at the schematic in Figure 51, the crossover region is about 200 mV and is defined by the voltage level at the base of Q5. Internally, two separate voltage sources are created approximately 1.2 V from either rail. One or the other is connected to Q5 based on the voltage applied to the SELECT pin. This allows for either dominant PNP pair operation, when the SELECT pin is left open, or dominant NPN pair operation, when the SELECT pin is pulled high. This pin also provides the traditional power-down function when it is pulled low. This allows the designer to achieve the best precision and ac performance for high-side and low-side signal applications. See Figure 45 through Figure 49 for SELECT pin characteristics.

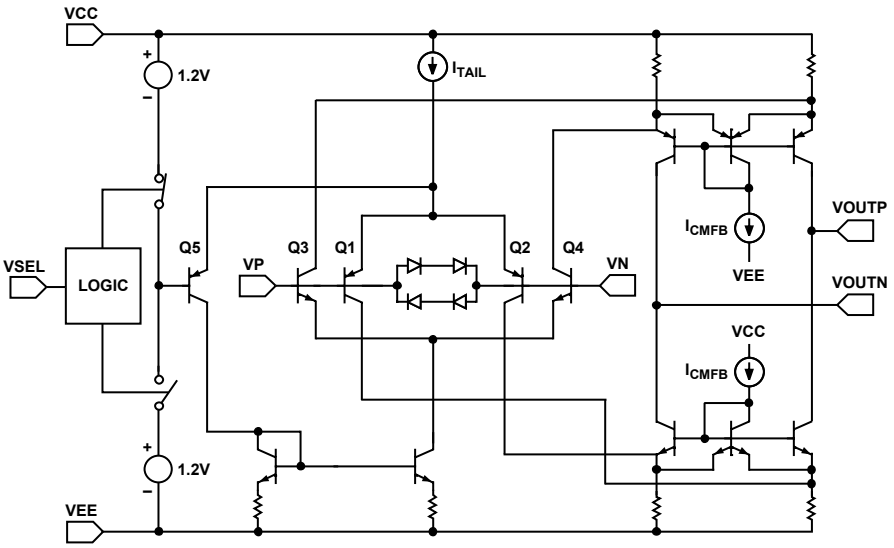

Figure 51. Simplified Input Stage

In the event that the crossover region cannot be avoided, specific attention has been given to the input stage to ensure constant transconductance and minimal offset in all regions of operation. The regions are: PNP input pair running, NPN input pair running, and both running at the same time (in the 200 mV crossover region). Maintaining constant transconductance in all regions ensures the best wideband distortion performance when going between these regions. With this technique the AD8028 can achieve greater than 80 dB SFDR for a 2 V p-p, 1 MHz, G = +1 signal on ±1.5 V supplies. Another requirement in achieving this level of distortion is the offset of each pair must be laser trimmed to achieve greater than 80 dB SFDR, even for low frequency signals.

Output Stage

The AD8028 uses a common-emitter output structure to achieve rail-to-rail output capability. The output stage is designed to drive 50 mA of linear output current, 40 mA within 200 mV of the rail, and 2.5 mA within 35 mV of the rail. Loading of the output stage, including any possible feedback network, will lower the open-loop gain of the amplifier. Refer to Figure 44 for the loading behavior. Capacitive load can degrade the phase margin of the amplifier. The AD8028 can drive up to 20 pF, G = +1 as seen in Figure 10. A series resistor (R_{SNUB}) should be included if the capacitive load is to exceed 20 pF for a gain of one. A small series output resistor (25 Ω to 50 Ω) should be used if the capacitive load exceeds 20 pF. Increasing the closed-loop gain will increase the amount of capacitive load that can be driven before a series resistor will need to be included.

DC Errors

The AD8028 uses two complementary input stages to achieve rail-to-rail input performance as mentioned in the Input Stage section. To use the dc performance over the entire common-mode range, the input bias current and input offset voltage of each pair must be considered.

Referring to Figure 52, the output offset voltage of each pair is calculated by

$$V_{OS,PNP,OUT} = V_{OS,PNP}\left(\frac{R_G + R_F}{R_G}\right),$$

$$V_{OS,NPN,OUT} = V_{OS,NPN}\left(\frac{R_G + R_F}{R_G}\right)$$

where the difference of the two will be the discontinuity experienced when going through the crossover region. The size of the discontinuity is defined as

$$V_{DIS} = \left(V_{OS,PNP} - V_{OS,NPN}\right)\left(\frac{R_G + R_F}{R_G}\right)$$

Using the crossover select feature of the AD8028 helps to avoid this region. In the event that the region cannot be avoided, the quantity ($V_{OS,\,PNP} - V_{OS,\,NPN}$)is trimmed to minimize this effect.

Because the input pairs are complementary, the input bias current will reverse polarity when going through the crossover region shown in Figure 32. The offset between pairs is described by

$$V_{OS,PNP} - V_{OS,NPN} = \left(I_{B,PNP} - I_{B,NPN}\right) \times \left[R_S\left(\frac{R_G + R_F}{R_G}\right) - R_F\right]$$

$I_{B,\,PNP}$ is the input bias current of either input when the PNP input pair is active, and $I_{B,\,NPN}$ is the input bias current or either input pair when the NPN pair is active. If R_S is sized so that when multiplied by the gain factor it equals R_F, this effect will be eliminated. It is strongly recommended to balance the impedances in this manner when traveling through the crossover region to minimize the dc error and distortion. As an example, assuming the PNP input pair has an input bias current of 6 µA and the NPN input pair has an input bias current of –2 µA, a 200 µV shift in offset will occur when traveling through the crossover region with R_F equal to 0 Ω and R_S equal to 25 Ω.

In addition to the input bias current shift between pairs, each input pair has an input bias current offset that will contribute to the total offset in the following manner

$$\Delta V_{OS} = I_{B+} R_S\left(\frac{R_G + R_F}{R_G}\right) - I_{B-} R_F$$

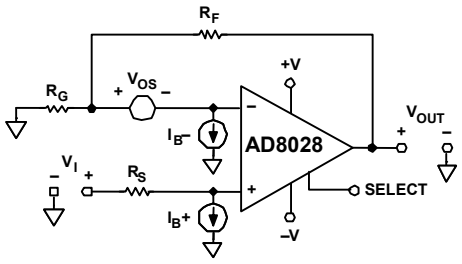

Figure 52. Op Amp DC Error Sources

WIDEBAND OPERATION

Voltage feedback amplifiers can use a wide range of resistor values to set their gain. Proper design of the application's feedback network requires consideration of the following issues:

- Poles formed by the amplifier's input capacitances with the resistances seen at the amplifier's input terminals
- Effects of mismatched source impedances
- Resistor value impact on the application's voltage noise
- Amplifier loading effects

The AD8028 has an input capacitance of 2 pF. This input capacitance will form a pole with the amplifier's feedback network, destabilizing the loop. For this reason, it is generally desirable to keep the source resistances below 500 Ω, unless some capacitance is included in the feedback network. Likewise, keeping the source resistances low will also take advantage of the AD8028's low input referred voltage noise of 4.3 nV/√Hz.

With a wide bandwidth of over 190 MHz, the AD8028 has numerous applications and configurations. The AD8028 shown in Figure 53 is configured as a noninverting amplifier. The inverting configuration is shown in Figure 54 and an easy selection table of gain, resistor values, bandwidth, slew rate, and noise performance is presented in Table 5.

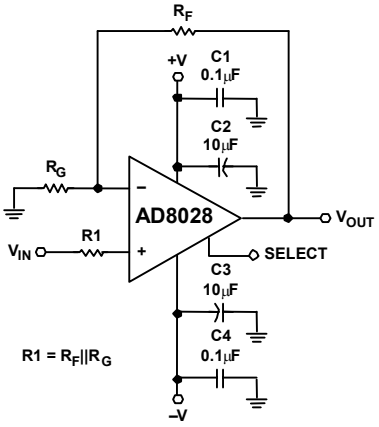

Figure 53. Wideband Noninverting Gain Configuration

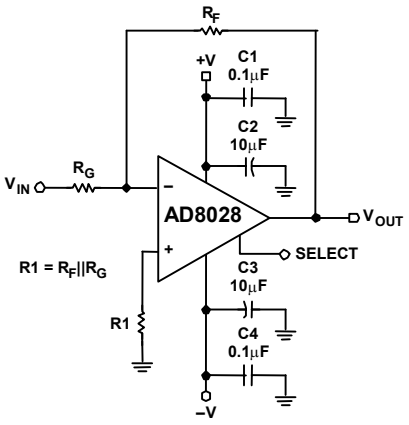

Figure 54. Wideband Inverting Gain Configuration

Table 5. Component Values, Bandwidth, and Noise Performance (V_S = ±2.5 V)

Noise Gain (Noninverting)	R_{SOURCE} (Ω)	R_F (Ω)	R_G (Ω)	–3 dB SS BW (MHz)	Output Noise with Resistors (nV/√Hz)
1	50	0	N/A	190	4.4
2	50	499	499	95	10
10	50	499	54.9	13	45

Circuit Considerations

Balanced Input Impedances

Balanced input impedances can help improve distortion performance. When the amplifier transitions from PNP pair to NPN pair operation, a change in both the magnitude and direction of the input bias current will occur. When multiplied times imbalanced input impedances, a change in offset will result. The key to minimizing this distortion is to keep the input impedances balanced on both inputs. Figure 55 shows the effect of the imbalance and degradation in distortion performance for a 50 Ω source impedance, with and without a 50 Ω balanced feedback path.

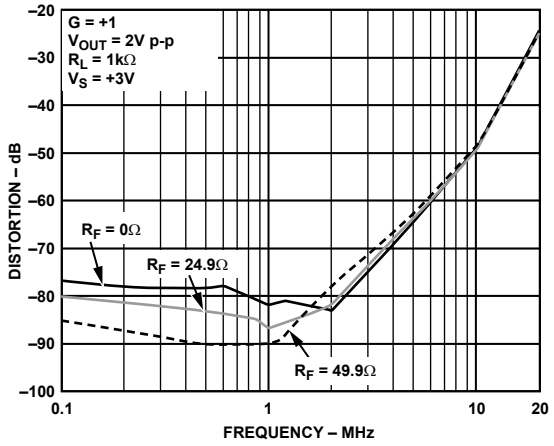

Figure 55. SFDR vs. Frequency and Various R_F

PCB Layout

As with all high speed op amps, achieving optimum performance from the AD8028 requires careful attention to PCB layout. Particular care must be exercised to minimize lead lengths of the bypass capacitors. Excess lead inductance can influence the frequency response and even cause high frequency oscillations. The use of a multilayer board, with an internal ground plane, will reduce ground noise and enable a tighter layout.

To achieve the shortest possible lead length at the inverting input, the feedback resistor, R_F, should be located beneath the board and span the distance from the output, Pin 6, to the input, Pin 2. The return node of the resistor R_G should be situated as closely as possible to the return node of the negative supply bypass capacitor connected to Pin 4.

On multilayer boards, all layers underneath the op amp should be cleared of metal to avoid creating parasitic capacitive elements. This is especially true at the summing junction (i.e., the –input). Extra capacitance at the summing junction can cause increased peaking in the frequency response and lower phase margin.

Grounding

To minimize parasitic inductances and ground loops in high speed, densely populated boards, a ground plane layer is critical. Understanding where the current flows in a circuit is critical in the implementation of high speed circuit design. The length of the current path is directly proportional to the magnitude of the parasitic inductances and thus the high frequency impedance of the path. Fast current changes in an inductive ground return will create unwanted noise and ringing.

The length of the high frequency bypass capacitor pads and traces is critical. A parasitic inductance in the bypass grounding will work against the low impedance created by the bypass capacitor. Because load currents flow from supplies as well as ground, the load should be placed at the same physical location as the bypass capacitor ground. For large values of capacitors, which are intended to be effective at lower frequencies, the current return path length is less critical.

Power Supply Bypassing

Power supply pins are actually inputs and care must be taken to provide a clean, low noise dc voltage source to these inputs. The bypass capacitors have two functions:

1. Provide a low impedance path for unwanted frequencies from the supply inputs to ground, thereby reducing the effect of noise on the supply lines.
2. Provide sufficient localized charge storage, for fast switching conditions and minimizing the voltage drop at the supply pins and the output of the amplifier. This is usually accomplished with larger electrolytic capacitors.

Decoupling methods are designed to minimize the bypassing impedance at all frequencies. This can be accomplished with a combination of capacitors in parallel to ground.

Good quality ceramic chip capacitors should be used and always kept as close to the amplifier package as possible. A parallel combination of a 0.01 µF ceramic and a 10 µF electrolytic covers a wide range of rejection for unwanted noise. The 10 µF capacitor is less critical for high frequency bypassing, and in most cases, one per supply line is sufficient.

APPLICATIONS

Using the AD8028 SELECT Pin

The AD8028 features a unique SELECT pin with two functions. The first is a power-down function that places the AD8028 into low power consumption mode. In the power-down mode, the amplifier draws 450 µA (typ) of supply current.

The second function, as mentioned in the Theory of Operation section, shifts the crossover point (where the NPN/PNP input differential pairs transition from one to the other) closer to either the positive supply rail or the negative supply rail. This selectable crossover point allows the user to minimize distortion based on the input signal and environment. The default state is 1.2 V from the positive power supply, with the SELECT pin left floating or in tri-state.

Table 6 shows the required voltages and modes of the SELECT pin.

Table 6. SELECT Pin Mode Control Table

Mode	SELECT Pin Voltage (V)		
	V_S = ±5 V	V_S = +5 V	V_S = +3 V
Disable	–5 to –4.2	0 to 0.8	0 to 0.8
Crossover Referenced 1.2 V to Positive Supply	–4.2 to –3.3	0.8 to 1.7	0.8 to 1.7
Crossover Referenced 1.2 V to Negative Supply	–3.3 to +5	1.7 to 5.0	1.7 to 3.0

When the input stage transitions from one input differential pair to the other, there is virtually no noticeable change in the output waveform.

The disable time of the AD8028 amplifier is load dependent. Typical data is presented in Table 7, see Figure 48 and Figure 49 for the actual switching measurements.

Table 7. DISABLE Switching Speeds

	Supply Voltages (R_L = 1 kΩ)		
	±5 V	+5 V	+3 V
t_{ON}	45 ns	50 ns	50 ns
t_{OFF}	980 ns	1100 ns	1150 ns

Driving a16-Bit ADC

With the adjustable crossover distortion selection point and low noise, the AD8028 is an ideal amplifier for driving or buffering input signals into high resolution ADCs, such as the **AD7677**. Figure 56 shows the typical schematic for driving the ADC. The AD8028, driving the AD7677, offers performance close to non-rail-to-rail amplifiers and avoids the need for an additional supply, other than the single 5 V supply already used by the ADC. In this application, the SELECT pins are biased to avoid the crossover region of the AD8028 for low distortion operation.

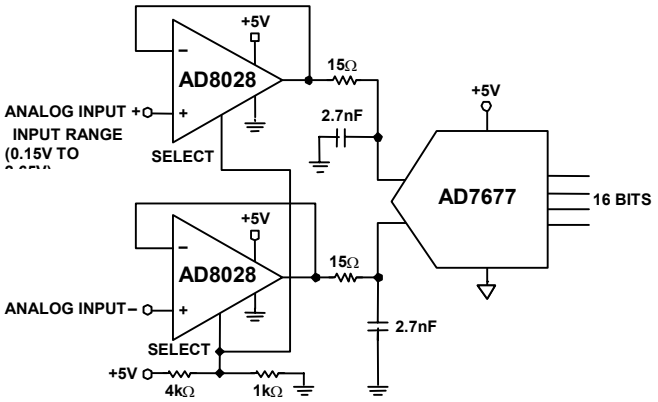

Figure 56. Unity Gain Differential Drive

As seen in Figure 57, the AD8028/AD7677 combination offers excellent integral nonlinearity (INL). Summary test data for the schematic shown in Figure 56 is presented in Table 8.

Table 8. ADC Driver Performance, f_C = 100 KHz, V_{OUT} = 4.7 V p-p

Parameter	Measurement
Second Harmonic Distortion	–105dB
Third Harmonic Distortion	–102dB
THD	–102 dB
SFDR	105 dBc

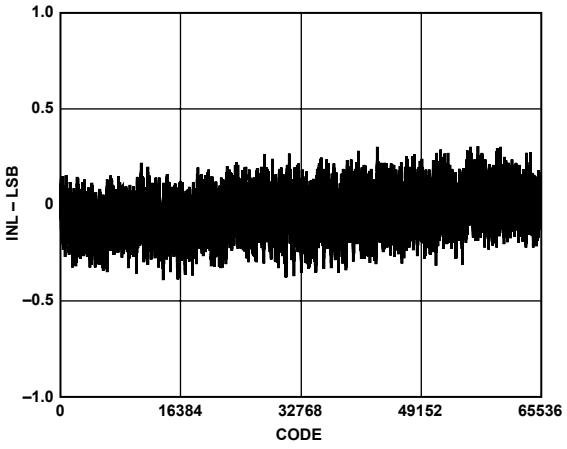

Figure 57. Integral Nonlinearity

Band-Pass Filter

In communication systems, active filters are used extensively in signal processing. The AD8028 is an excellent choice for active filter applications. In realizing this filter, it is important that the amplifier has a large signal bandwidth of at least 10× of the center frequency, f_O, otherwise a phase shift can occur in the amplifier, causing instability and oscillations.

In the schematic shown in Figure 58, the AD8028 is configured as a 1 MHz band-pass filter. The target specifications are f_O = 1 MHz and a –3 dB pass band of 500 kHz. When designing a band-pass filter, the designer must start by selecting the following: f_O, Q, C1, and R4. Then using the equations shown below calculate the remaining variables.

The test data shown in Figure 59 indicates that this design yielded a filter response with a center frequency f_O = 1 MHz and a bandwidth of 450 kHz.

$$Q = \frac{f_o\,(MHz)}{Pass\ Band\,(MHz)}$$

$$k = 2\pi f_O C1$$

$$C2 = 0.5C1$$

$$R1 = 2/k,\ R2 = 2/3k,\ R3 = 4/k$$

$$H = 1/3\left(6.5 - 1/Q\right)$$

$$R5 = R4/\left(H - 1\right)$$

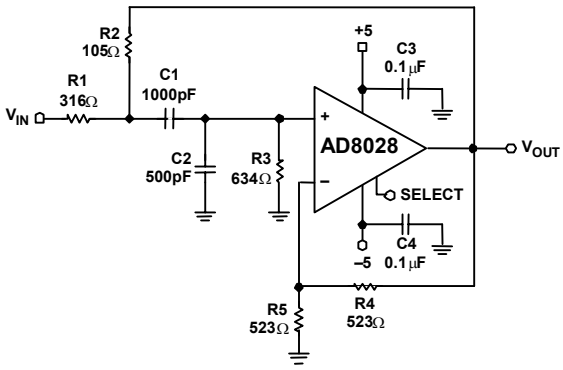

Figure 58. Band-Pass Filter Schematic

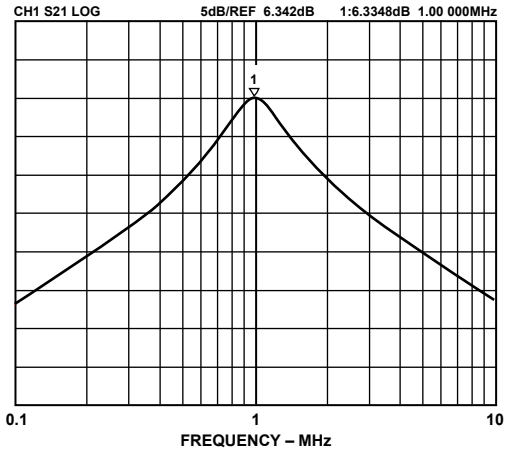

Figure 59. Band-Pass Filter Response

Design Tools and Technical Support

Analog Devices is committed to simplifying the design process by providing technical support and online design tools. We offer technical support via free evaluation boards, sample ICs, interactive evaluation tools, datasheets, application notes, and phone and email support, which is all available at www. analog.com.

OUTLINE DIMENSIONS

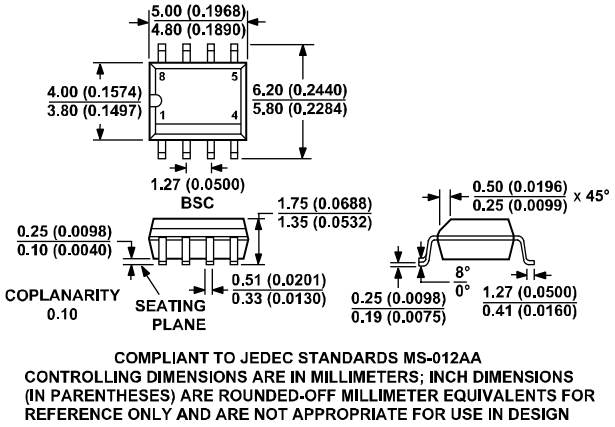

Figure 60. 8-Lead Standard Small Outline Package, Narrow Body [SOIC] (RN-8)—Dimensions shown in millimeters and (inches)

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

Ordering Guide

AD8028 Products	Minimum Ordering Quantity	Temperature Range	Package Description	Package Outline	Branding Information
AD8028AR	1	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8028AR-REEL	2,500	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8028AR-REEL7	1000	–40°C to +125°C	8-Lead SOIC	RN-8	
AD8028ARM	1	–40°C to +125°C	10-Lead SOIC	RM-10	HSB
AD8028ARM-REEL	3,000	–40°C to +125°C	10-Lead SOIC	RM-10	HSB
AD8028ARM-REEL7	1,000	–40°C to +125°C	10-Lead SOIC	RM-10	HSB

C03327-0-2/03(0)