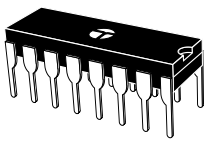
PROTEK DEVICES®
.....Engineered solutions for the transient environment

LCD05C thru LCD24C

HIGH SPEED TVS DIODE ARRAY

APPLICATIONS

- ✓ Ethernet - 10/100 Base T
- ✓ RS-485
- ✓ xDSL & ATM
- ✓ SCSI & USB
- ✓ Audio/Video I/O Ports



16 PIN PLASTIC DIP

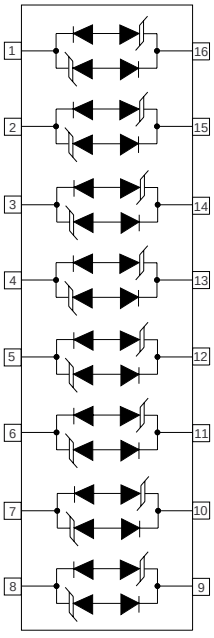
IEC COMPATIBILITY (EN61000-4)

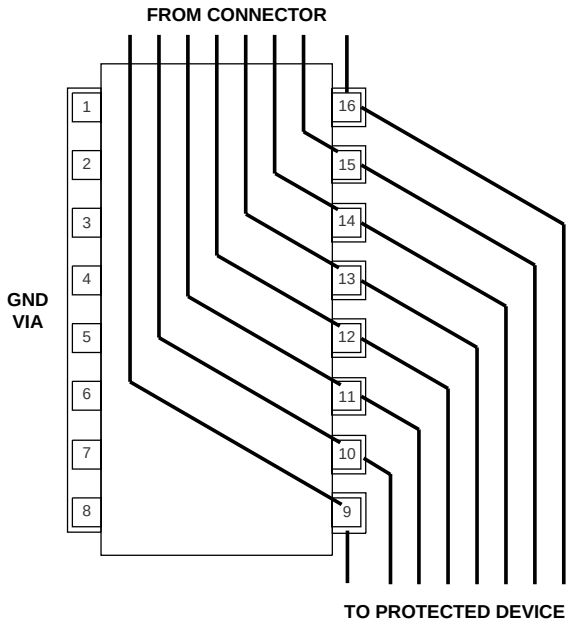
- ✓ 64100-4-2 (ESD): Air - 15kv, Contact - 8kv
- ✓ 64100-4-4 (EFT): 40A - 5/50ns
- ✓ 64100-4-5 (Lightning):

FEATURES

- ✓ Suitable for Low Capacitance High Speed V^2D Protection
- ✓ 500 Watts Peak Pulse Power Dissipation per Line (8/20 μs)
- ✓ Bidirectional Configuration
- ✓ ESD Protection > 40 kilovolts
- ✓ Low Capacitance - 15 pF
- ✓ Available in 5 Voltage Types: 5.0V to 24V
- ✓ Standard Dual-In-Line Package
- ✓ Protects Up to Eight (8) Lines
- ✓ UL 94V-0 Flammability Classification

CIRCUIT DIAGRAM & PCB LAYOUT RECOMMENDATION





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DEVICE CHARACTERISTICS

MECHANICAL CHARACTERISTICS		MAXIMUM RATINGS	
PACKAGE	Molded 16 Pin Dual-in-Line Package	**P_{PP} @ 25°C (SEE FIGURE 1)**	500 Watts, 8/20 µs Waveshape
APPROX. WEIGHT	1.2 grams	**OPERATING & STORAGE TEMPERATURE**	-55°C to +150°C
DEVICE MARKINGS	Logo & Part Number	**REPETITION RATE (DUTY CYCLE)**	0.01%
MISCELLANEOUS	Pin 1 Indicatied by Dot on Top of Package	**$T_{CLAMPING}$ (0 VOLTS TO $V_{(BR)}$ MIN.)**	Bidirectional: < 1 x 10^{-9} seconds

ELECTRICAL CHARACTERISTICS @ 25° C Ambient Temperature

PROTEK PART NUMBER (See Note 1)	RATED STAND-OFF VOLTAGE V_{WM} VOLTS	MINIMUM BREAKDOWN VOLTAGE @ 1 mA $V_{(BR)}$ VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ I_P = 1 A V_C VOLTS	MAXIMUM CLAMPING VOLTAGE (See Fig. 2) @ 8/20 µs V_C @ I_{PP}	MAXIMUM LEAKAGE CURRENT @ V_{WM} I_D µA	MAXIMUM CAPACITANCE @ 0V, 1 MHz C pF	TEMPERATURE COEFFICIENT OF $V_{(BR)}$ $\Theta V_{(BR)}$ mV/°C
LCD05C	5.0	6.0	9.8	22V @ 40A	100	15	3
LCD08C	8.0	8.5	12.3	23.5V @ 22A	10	15	9
LCD12C	12.0	13.3	19.0	28V @ 25A	4	15	16
LCD15C	15.0	16.7	25.5	36V @ 20A	4	15	17
LCD24C	24.0	26.7	40.0	56V @ 12A	4	15	26

Note 1: Tested on pin pairs 1 & 16, 2 & 15, 3 & 14, 4 & 13, 5 & 12, 6 & 11, 7 & 10 and 8 & 9.

FIGURE 1
PEAK PULSE POWER VS PULSE TIME

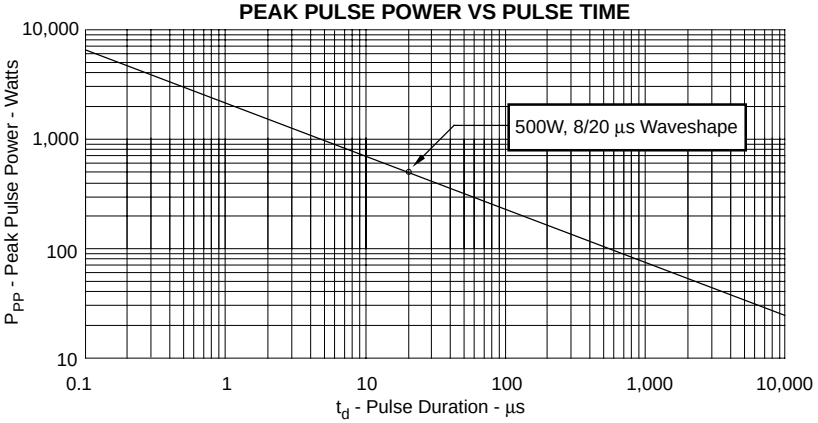
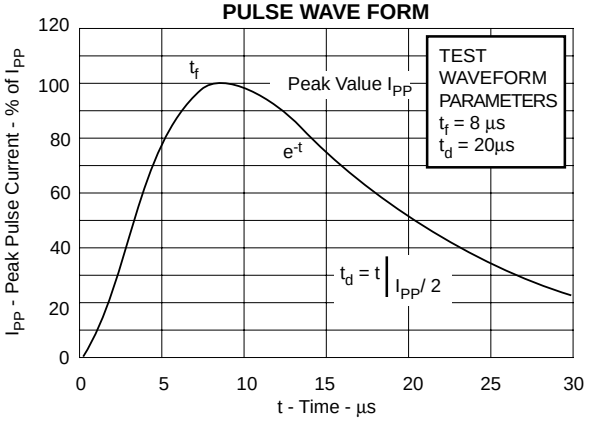


FIGURE 2
PULSE WAVE FORM



DEVICE CHARACTERISTICS

FIGURE 3
POWER DERATING CURVE

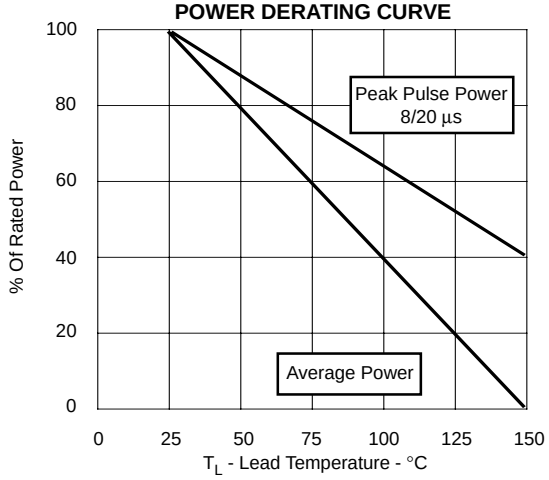
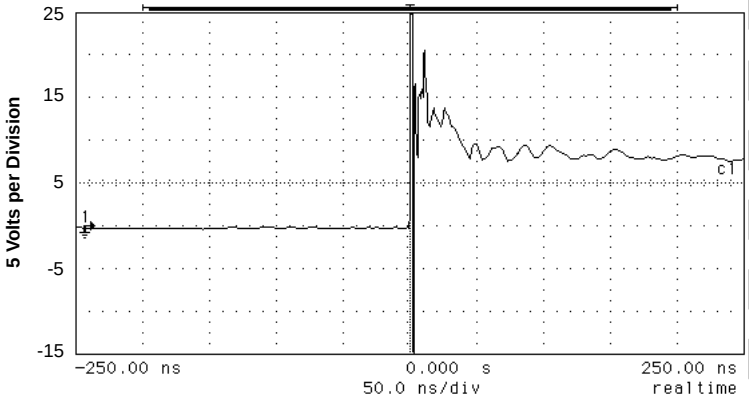
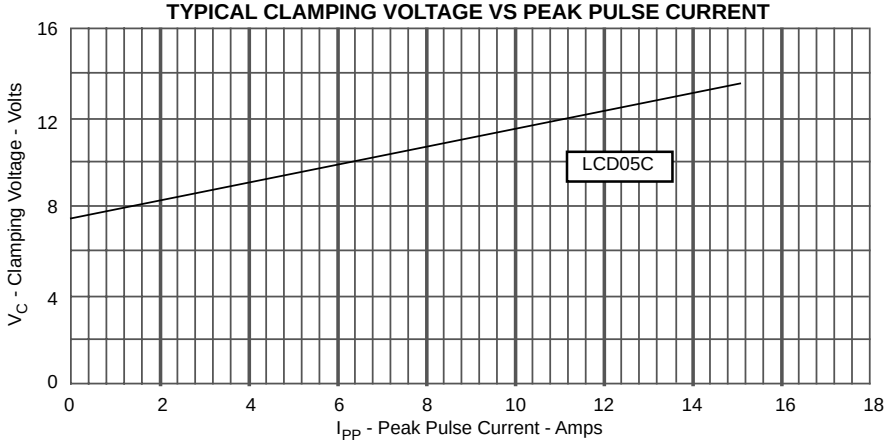


FIGURE 4
OVERSHOOT & CLAMPING VOLTAGE FOR LCD05C



ESD Test Pulse: 12 kilovolt, 1/30ns (waveshape)

FIGURE 5
TYPICAL CLAMPING VOLTAGE VS PEAK PULSE CURRENT



DEVICE SPECIFIC APPLICATION NOTE

The LCD Series are bidirectional, low capacitance, silicon TVS devices designed to protect multiple data or signal lines. This device provides ESD protection > 40kV and has a 500 Watt peak pulse power dissipation for an 8/20 μs pulse per line.

The LCD is ideal for use in protecting multimode transceiver I/O lines and data communications applications such as USB. This low capacitance device allows these types of applications to operate safely without significant signal distortion. When a transient voltage strikes a data line, the device becomes a low impedance path diverting the transient current to ground. TVS devices are capable of clamping both positive and negative transient voltages to a low enough level such that a sensitive IC component will not be damaged.

As shown in Figure 1, a typical RS-485 transceiver application, the LCD protects up to four (4) bidirectional lines where the normal signal voltage is both positive and negative. Each pin pair is symmetrical so that each pair can be connected to both data lines and ground. In order to insure low crosstalk and isolation, each line/ground pin pair is electrically independent of each other. Pins 1, 2, 3, 4, 9, 10, 11 and 12 are connected to ground. Pins 5, 6, 7, 8,13, 14,15 and 16 are connected to the data lines.

In addition, the LCD can protect up to four USB ports. As shown in Figure 2, in order to provide common-mode protection, pins 16 through 10 can be connected to the data lines and pins 1 through 7 can be connected to ground.

Circuit Board Layout Recommendations

Circuit board layout is critical for Electromagnetic Compatibility (EMC) protection. The following guidelines are recommended:

✓ The LCD should be placed near the input terminals or connectors. By placing the TVS close to the connectors, the device will divert the transient current immediately before it can be coupled into the nearby traces.

✓ The path length between the TVS device and the protected line should be minimized.

✓ All conductive loops including power and ground loops should be minimized.

✓ The transient current return path to ground should be kept as short as possible to reduce parasitic inductance.

✓ Ground planes should be used whenever possible. For Multilayer PCBs, use ground vias.

Figure 1. Typical RS-485 Transceiver Protection Circuit (Differential & Common-Mode)

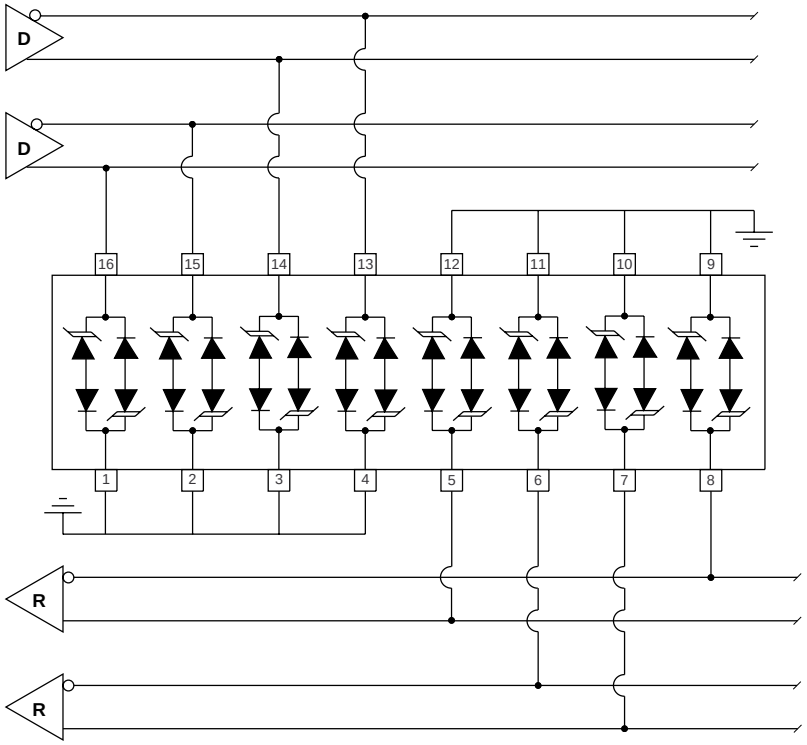
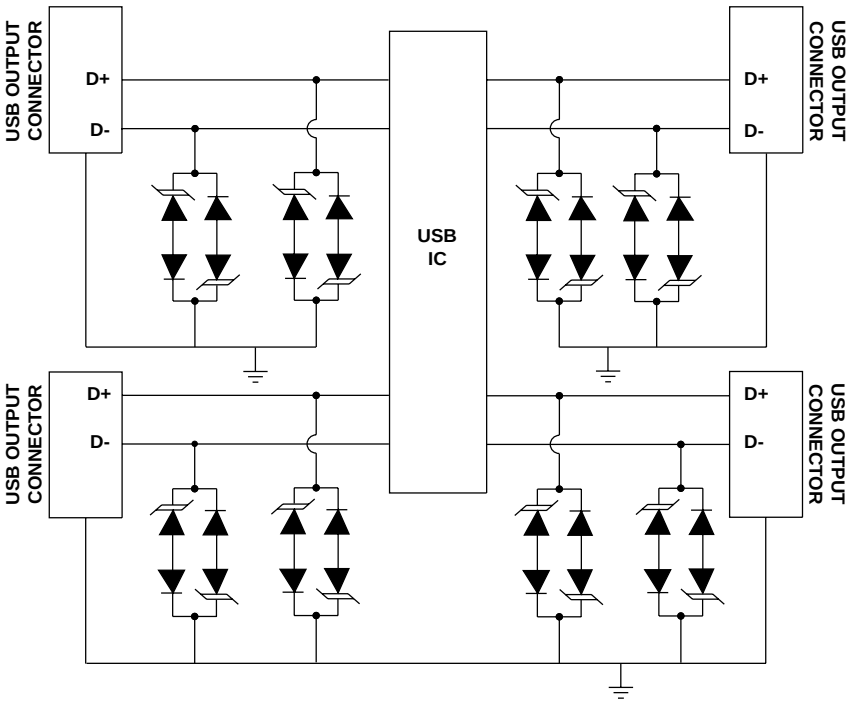
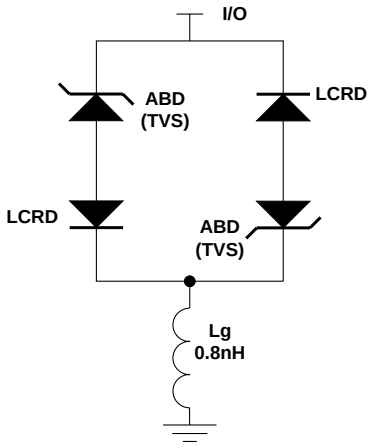


Figure 2. Typical Common-Mode USB Protection Circuit



SPICE MODEL & PARAMETERS

FIGURE 1
SPICE MODEL FOR LCD SERIES



LCRD: LOW CAPACITANCE RECTIFIER DIODE
ABD: AVALANCHE BREAKDOWN DIODE (TVS)
Lg: LEAD INDUCTANCE

TABLE 1 - SPICE PARAMETERS

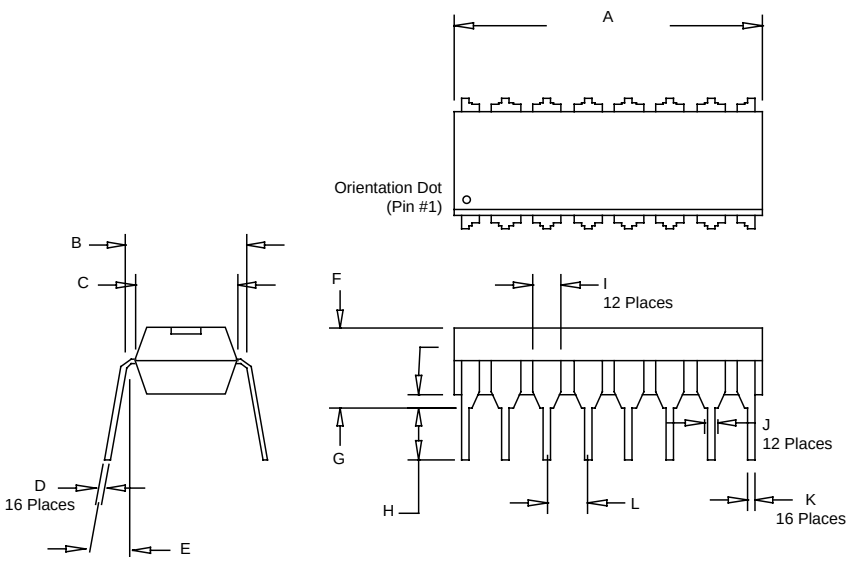
PARAMETER	UNIT	(ABD) TVS	LCRD
BV	V	See Table 2	200
IBV	µA	1	0.01
Cjo	pF	See Table 2	5
Is	A	See Table 2	10E-14
Vj	V	0.6	0.6
M	-	0.33	0.33
N	-	1	1
Rs	Ohms	See Table 2	0.31
TT	µs	0.1	1
EG	eV	1.11	1.11

TABLE 2 - ABD SPECIFIC SPICE PARAMETERS

PART NO.	BV (Volts)	Cjo (pF)	Is (Amps)	Rs (Ohms)
LCD05C	6.0	880	10E-12	0.09
LCD08C	8.5	481	10E-14	0.18
LCD12C	13.3	319	10E-14	0.22
LCD15C	16.7	238	10E-14	0.31
LCD24C	26.7	210	10E-14	0.93

PACKAGE OUTLINES & DIMENSIONS

16 PIN PLASTIC DIP



16 PIN DIP DIMENSIONS

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	-	19.8	-	0.780
B	6.10	6.60	0.240	0.260
C	7.37	7.87	0.290	0.310
D	0.25	0.36	0.010	0.014
E	0°	10°	0°	10°
F	0.51	-	0.020	-
G	-	5.08	-	0.200
H	3.17	-	0.125	-
I	-	1.78	-	0.070
J	0.84 TYP	0.84 TYP	0.033 TYP	0.033 TYP
K	0.381	0.533	0.021	0.051
L	2.54 TYP	2.54 TYP	0.100 TYP	0.100 TYP