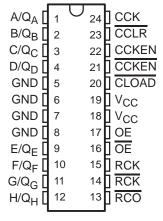
- Parallel 3-State I/O: Register Inputs/ Counter Outputs
- Counter Has Direct Overriding Load and Clear
- Flow-Through Architecture Optimizes PCB Layout
- Center-Pin V_{CC} and GND Configurations Minimize High-Speed Switching Noise
- EPIC™ (Enhanced-Performance Implanted CMOS) 1-μm Process
- 500-mA Typical Latch-Up Immunity at 125°C
- Package Options Include Plastic Small-Outline Packages and Standard Plastic 300-mil DIPs

DW OR NT PACKAGE (TOP VIEW)



description

The 74AC11953 consists of a parallel input, an 8-bit storage register feeding an 8-bit counter, and a 3-state I/O which provides parallel count outputs. Both the register and the counter have individual positive-edge triggered clocks.

The function tables show the operation of the counter clock-enable (CCKEN, $\overline{\text{CCKEN}}$) and output-enable (OE, $\overline{\text{OE}}$) inputs. A register clock-enable ($\overline{\text{RCK}}$) input is also provided.

The counter (\overline{RCO}) input has direct load and clear functions. A low-going \overline{RCO} pulse will be obtained when the counter reaches the hex word FF. Expansion is easily accomplished for two stages by connecting \overline{RCO} of the first stage to \overline{CCKEN} of the second stage. Cascading for larger count chains can be accomplished by connecting \overline{RCO} of each stage to \overline{CCK} of the following stage.

The 74AC11593 is characterized for operation from -40° C to 85°C.

Function Tables

COUNTER CLOCK ENABLE

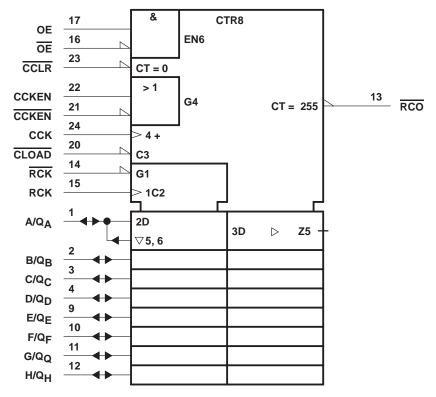
INP	UTS	OUTPUTS
CCKEN	CCKEN	A/Q _A THRU H/Q _H
L	L	Enable
L	Н	Disable
Н	L	Enable
Н	Н	Enable

OUTPUT ENABLE

INP	UTS	OUTPUTS
OE	OE	A/Q _A THRU H/Q _H
L	L	Input mode
L	Н	Input mode
Н	L	Output mode
Н	Н	Input mode

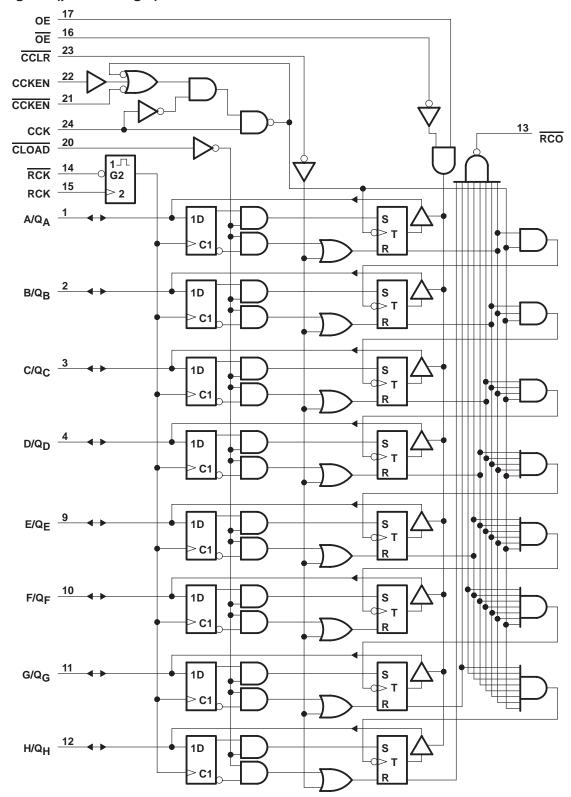
EPIC is a trademark of Texas Instruments Incorporated.

logic symbol†

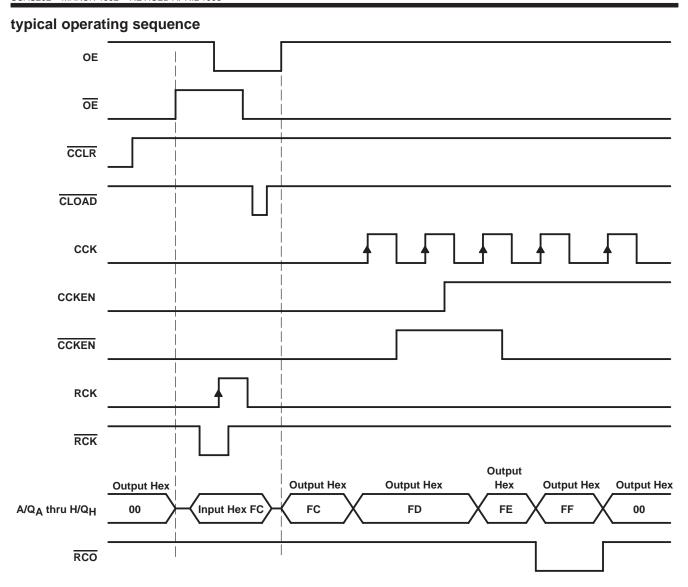


[†] This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)







absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V _{CC}	
Input voltage range, V _I (see Note 1)	0.5 V to V _{CC} + 0.5 V
Output voltage range, VO (see Note 1)	$-0.5 \text{ V to V}_{CC} + 0.5 \text{ V}$
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I _{OK} (V _O < 0 or V _O > V _{CC})	\pm 50 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	\pm 50 mA
Continuous current through V _{CC} or GND	± 225 mA
Storage temperature range	–65°C to 150°C

[†] Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output voltage ratings may be exceeded if the input and output current ratings are observed.



recommended operating conditions (see Note 2)

			MIN	NOM	MAX	UNIT
VCC	Supply voltage		3	5	5.5	V
		VCC = 3 V	2.1			
\vee_{IH}	High-level input voltage	V _{CC} = 4.5 V	3.15			V
		V _{CC} = 5.5 V	3.85			
		V _{CC} = 3 V			0.9	
VIL	Low-level input voltage	V _{CC} = 4.5 V			1.35	V
		V _{CC} = 5.5 V	3 5 5.3 2.1 3.15 3.85 0.9 1.36 0 VCC 0 VCC 0 -4 -2 -2 -2 -2 -2 -2 -2 -2 -2 -2 -2 -2 -2	1.65		
VI	Input voltage		0		Vcc	V
VO	Output voltage		0		Vcc	V
		V _{CC} = 3 V			- 4	
lOH	High-level output current	V _{CC} = 4.5 V			- 24	mA
		V _{CC} = 5.5 V			-24	
		V _C C = 3 V			12	
lOL	Low-level output current	V _{CC} = 4.5 V			24	mA
		V _{CC} = 5.5 V			24	
$\Delta t/\Delta v$	Input transition rise or fall rate		0		10	ns/V
TA	Operating free-air temperature		- 40		85	°C

NOTE 2: Unused or floating inputs must be held high or low.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

DADAMETER	TEGT CONDITIONS	.,	T,	4 = 25°C	;	BAINI	MAY	
PARAMETER	TEST CONDITIONS	v _{CC}	MIN	TYP	MAX	MIN	MAX	UNIT
	I _{OH} = - 50 μA		2.9			2.9		
			4.4			4.4		
		5.5 V	5.4			5.4		V
∨он	I _{OH} = -4 mA	3 V	2.58			2.48		
-	Jan. 24 mA	4.5 V	3.94			3.8		
	I _{OH} = – 24 mA	5.5 V	4.94			4.8		
	$I_{OH} = -75 \text{ mA}^{\dagger}$	5.5 V				3.85		
					0.1		0.1	
	$I_{OL} = 50 \mu A$	4.5 V			0.1		0.1	
					0.1		0.1	
VOL	I _{OL} = 12 mA	3 V			0.36		0.44	V
-	1 24 m4	4.5 V			0.36		0.44	
	I _{OL} = 24 mA	5.5 V			0.36		0.44	
	$I_{OL} = 75 \text{ mA}^{\dagger}$	5.5 V					1.65	
IJ	$V_I = V_{CC}$ or GND	5.5 V			± 0.1		± 1	μΑ
loz	$V_O = V_{CC}$ or GND	5.5 V			± 0.5		± 5	μΑ
Icc	$V_I = V_{CC}$ or GND, $I_O = 0$	5.5 V			8		80	μΑ
Ci	$V_I = V_{CC}$ or GND	5 V		4.5				pF

[†] Not more than one output should be tested at a time, and the duration of the test should not exceed 10 ms.



timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

			$T_A = 3$	T _A = 25°C				
			MIN MAX		MIN	MAX	UNIT	
f _{clock}	Clock frequency, CCK or RCK			40		40	MHz	
		CCK high or low	6		6			
	Pulse duration	RCK high or low	6		6			
t _W		RCK high or low	4.5		4.5		ns	
		CCLR low	7.5		7.5			
		CLOAD low	6.1		6.1			
		CCKEN low before CCK↑	5.2		5.2			
		CCKEN high before CCK↑	6.4		6.4			
	Outon the	CCLR high before CCK↑	1.7		1.7			
t _{su}	Setup time	CLOAD high before CCK↑	8.2		8.2		ns	
		RCK↑ before CLOAD↑†	11.1		11.1			
		Data A thru H before RCK↑	2.3		2.3			
	11.110	Data A thru H after RCK↑	0.5		0.5			
th	Hold time	All others	0.2		0.2		ns	

timing requirements over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

			T _A =	25°C			
			MIN MAX 70		MIN	MAX	UNIT
f _{clock}	Clock frequency, CCK or RCK			70		70	MHz
3.00.1	Pulse duration	CCK high or low	5		5		
		RCK high or low	5		5		
t_{W}		RCK high or low	4.5		4.5		ns
		CCLR low	5		5		
		CLOAD low	4.7		4.7		
		CCKEN low before CCK↑	3.1		3.1		
		CCKEN high before CCK↑	4.3		4.3		
	0	CCLR high before CCK↑	1.1		1.1		
t _{su}	Setup time	CLOAD high before CCK↑	5.4		5.4		ns
		RCK↑ before CLOAD↑†	7.8		7.8		
		Data A thru H before RCK↑	2		2		
		Data A thru H after RCK↑	1.1		1.1		
th	Hold time	All others	0.8		0.8		ns

[†] This time insures the data saved by RCK↑ will also be loaded into the counter.



switching characteristics over recommended operating free-air temperature range, V_{CC} = 3.3 V \pm 0.3 V (unless otherwise noted) (see Figure 1)

	FROM	то	T,	4 = 25°C	;	MIN		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	MAX	UNIT
f _{max}			40			40		MHz
^t PLH	CCK	0	6.8	14.4	19.3	6.8	22.4	20
^t PHL	CCK	Q	6.4	14.1	18.8	6.4	21.1	ns
^t PLH	CLOAD	0	6.7	17.3	23.6	6.7	27.1	20
t _{PHL}	CLOAD	Q	3.9	18.9	29.1	3.9	32.3	ns
^t PHL	CCLR	Q	5.4	13	17.6	5.4	19.8	ns
^t PZH	OE	_	7.3	15.7	20.8	7.3	24.1	
t _{PZL}	OE	Q	8	17.7	23.2	8	26.7	ns
^t PZH	ŌĒ	Q	6.9	15.2	20.2	6.9	23.3	
t _{PZL}	OE		7.8	17.3	22.7	7.8	26.1	ns
^t PHZ	OE	0	6.4	10.3	13.8	6.4	15.2	20
t _{PLZ}	OE	Q	6.6	10.8	14.1	6.6	16.1	ns
^t PHZ	ŌĒ	Q	5.7	9.6	12.8	5.7	14.1	20
t _{PLZ}	OE	Q	5.9	10.2	13.4	5.9	15.2	ns
^t PLH	ССК	RCO	5.3	12	16	5.3	18.6	20
^t PHL	CCK	RCO	7.1	15.4	20.3	7.1	23.1	ns
^t PLH	CLOAD	RCO	5.9	12.4	16.5	5.9	18.8	
^t PHL			10.1	19.6	25.5	10.1	29.4	ns
^t PLH	CCLR	RCO	5.6	12.3	16.6	5.6	19.2	ns
tPLH	POK	RCO	8.6	17.3	22.2	8.6	25.8	
t _{PHL}	RCK	KCO	10.3	20.3	26.2	10.3	30.3	ns

74AC11593 **8-BIT BINARY COUNTER** WITH 3-STATE I/O INPUT REGISTERS SCAS202 - MARCH 1992 - REVISED APRIL 1993

switching characteristics over recommended operating free-air temperature range, V_{CC} = 5 V \pm 0.5 V (unless otherwise noted) (see Figure 1)

DADAMETED	FROM	то	T,	4 = 25°C	;	MIN MAX		
PARAMETER	(INPUT)	(OUTPUT)	MIN	TYP	MAX	MIN	WAX	UNIT
f _{max}			70			70		MHz
t _{PLH}	CCK	Q	4.1	8.7	12.4	4.1	14.3	20
^t PHL	CCK	Q	4.2	8.9	12.6	4.2	14.2	ns
^t PLH	CLOAD	Q	3.7	10	15.3	3.7	17.4	20
^t PHL	CLOAD	Q	3.4	11.4	18.3	3.4	20.6	ns
^t PHL	CCLR	Q	3.3	7.9	11.8	3.3	13.4	ns
^t PZH	OE	Q	4.1	9.1	13.2	4.1	15.3	20
t _{PZL}	OE .	ų ,	4.1	9.4	13.8	4.1	16	ns
^t PZH	tPZH OE	Q	3.8	8.7	13	3.8	15	ns
^t PZL			3.9	9.1	13.4	3.9	15.4	
^t PHZ	OE	Q	4.2	7.6	10.6	4.2	11.6	ns
t _{PLZ}	OE .		5.3	8.8	11.8	5.3	13.1	
^t PHZ	ŌĒ	Q	4.4	7.3	10.1	4.4	11	ns
t _{PLZ}	OE .	Q	5.2	8.5	11.6	5.2	13	115
^t PLH	ССК	RCO	3.5	7.6	11.2	3.5	12.8	
^t PHL	CCK	RCO	4.1	9.2	13.4	4.1	15.4	ns
^t PLH	CLOAD	RCO	3.5	7.8	11.2	3.5	12.8	
^t PHL	t _{PHL} CLOAD		5.6	11.7	16.6	5.6	19	ns
^t PLH	CCLR	RCO	3.6	8	11.6	3.6	13.4	ns
^t PLH	RCK	RCO	5	10.3	14.4	5	16.7	
^t PHL	RUN	RCO	5.5	11.7	16.6	5.5	19.2	ns

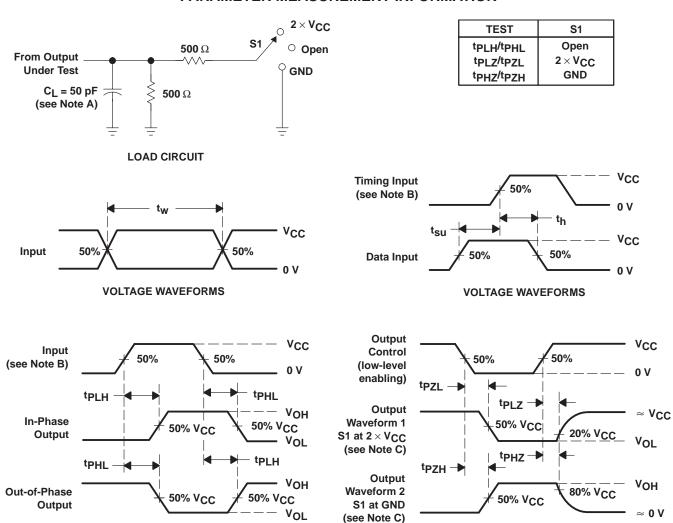
operating characteristics, V_{CC} = 5 V, T_A = 25°C

	PARAMETER					
		Outputs enabled	0 50 5		66	_
Cpd	Power dissipation capacitance	Outputs disabled	$C_L = 50 \text{ pF},$	f = 1 MHz	15	pF

VOLTAGE WAVEFORMS

SCAS202 - MARCH 1992 - REVISED APRIL 1993

PARAMETER MEASUREMENT INFORMATION



NOTES: A. C_L includes probe and jig capacitance.

VOLTAGE WAVEFORMS

B. All input pulses are supplied by generators having the following characteristics: PRR \leq 10 MHz, $Z_{O} = 50 \Omega$, $t_{f} = 3 \text{ ns}$, $t_{f} = 3 \text{ ns}$.

(see Note C)

- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms





i.com 24-Jun-2005

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
74AC11593DW	OBSOLETE	SOIC	DW	24	TBD	Call TI	Call TI
74AC11593DWR	OBSOLETE	SOIC	DW	20	TBD	Call TI	Call TI
74AC11593DWR	OBSOLETE	SOIC	DW	20	TBD	Call TI	Call TI
74AC11593NT	OBSOLETE	PDIP	NT	24	TBD	Call TI	Call TI
74AC11593NT	OBSOLETE	PDIP	NT	24	TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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74AC11593DWR	OBSOLETE	SOIC	DW	20	TBD	Call TI	Call TI
74AC11593DWR	OBSOLETE	SOIC	DW	20	TBD	Call TI	Call TI
74AC11593NT	OBSOLETE	PDIP	NT	24	TBD	Call TI	Call TI
74AC11593NT	OBSOLETE	PDIP	NT	24	TBD	Call TI	Call TI

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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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		Wireless	www.ti.com/wireless-apps