

14-Bit and 16-Bit Parallel Low Glitch Multiplying DACs with 4-Quadrant Resistors

FEATURES

- **True 16-Bit Performance Over Industrial Temperature Range**
- **DNL and INL: 1LSB Max**
- **On-Chip 4-Quadrant Resistors Allow Precise 0V to 10V, 0V to -10V or $\pm 10V$ Outputs**
- **Pin Compatible 14- and 16-Bit Parts**
- **Asynchronous Clear Pin**
 - LTC1591/LTC1597: Reset to Zero Scale
 - LTC1591-1/LTC1597-1: Reset to Mid-Scale
- **Glitch Impulse < 2nV-s**
- **Low Power Consumption: 10 μ W Typ**
- **Power-On Reset**
- **28-Lead SSOP Package**

APPLICATIONS

- Process Control and Industrial Automation
- Direct Digital Waveform Generation
- Software-Controlled Gain Adjustment
- Automatic Test Equipment

DESCRIPTION

The **LTC®1591/LTC1597** are pin compatible, parallel input 14-bit and 16-bit multiplying current output DACs that operate from a single 5V supply. INL and DNL are accurate to 1LSB over the industrial temperature range in both 2- and 4-quadrant multiplying modes. True 16-bit 4-quadrant multiplication is achieved with on-chip 4-quadrant multiplication resistors.

These DACs include an internal deglitcher circuit that reduces the glitch impulse to less than 2nV-s (typ). The asynchronous $\overline{\text{CLR}}$ pin resets the LTC1591/LTC1597 to zero scale and LTC1591-1/LTC1597-1 to mid-scale.

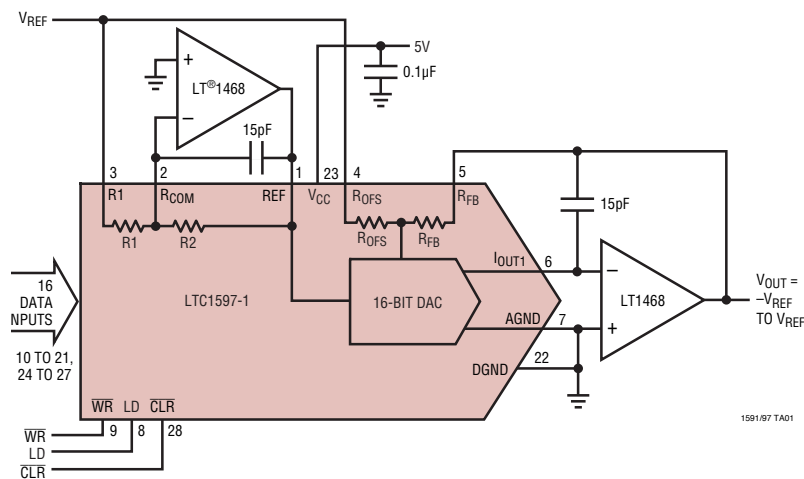
The LTC1591/LTC1597 are available in the 28-pin SSOP package and are specified over the industrial temperature range.

For serial interface 16-bit current output DACs refer to the LTC1595/LTC1596 data sheet.

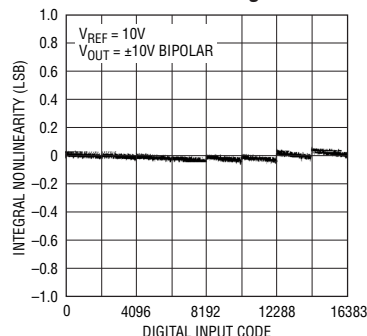
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TYPICAL APPLICATION

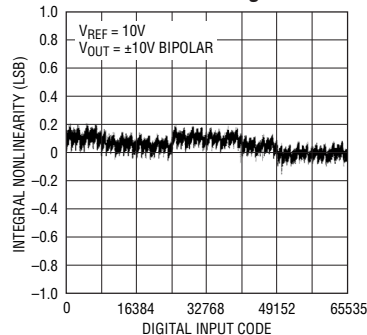
16-Bit, 4-Quadrant Multiplying DAC with a Minimum of External Components



LTC1591/LTC1591-1 Integral Nonlinearity



LTC1597/LTC1597-1 Integral Nonlinearity



LTC1591/LTC1597

ABSOLUTE MAXIMUM RATINGS (Note 1)

V_{CC} to AGND	–0.5V to 7V
V_{CC} to DGND	–0.5V to 7V
AGND to DGND	$V_{CC} + 0.5V$
DGND to AGND	$V_{CC} + 0.5V$
REF, R _{0FS} , R _{FB} , R1, R _{COM} to AGND, DGND	±25V
Digital Inputs to DGND	–0.5V to ($V_{CC} + 0.5V$)
I _{OUT1} to AGND	–0.5V to ($V_{CC} + 0.5V$)
Maximum Junction Temperature	125°C

Operating Temperature Range	
LTC1591C/LTC1591-1C	
LTC1597C/LTC1597-1C	0°C to 70°C
LTC1591I/LTC1591-1I	
LTC1597I/LTC1597-1I	–40°C to 85°C
Storage Temperature Range	–65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

PIN CONFIGURATION

LTC1591 TOP VIEW G PACKAGE 28-LEAD PLASTIC SSOP $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 95^{\circ}C/W$	LTC1591 TOP VIEW N PACKAGE 28-LEAD NARROW PDIP $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 70^{\circ}C/W$ OBSOLETE PACKAGE
LTC1597 TOP VIEW G PACKAGE 28-LEAD PLASTIC SSOP $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 95^{\circ}C/W$	LTC1597 TOP VIEW N PACKAGE 28-LEAD NARROW PDIP $T_{JMAX} = 125^{\circ}C, \theta_{JA} = 70^{\circ}C/W$ OBSOLETE PACKAGE

ORDER INFORMATION

LEAD FREE FINISH	TAPE AND REEL	PART MARKING	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTC1591CG#PBF	LTC1591CG#TRPBF	LTC1591CG	28-Lead Plastic SSOP	0°C to 70°C
LTC1591-1CG#PBF	LTC1591-1CG#TRPBF	LTC1591-1CG	28-Lead Plastic SSOP	0°C to 70°C
LTC1591IG#PBF	LTC1591IG#TRPBF	LTC1591IG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1591-1IG#PBF	LTC1591-1IG#TRPBF	LTC1591-1IG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1597ACG#PBF	LTC1597ACG#TRPBF	LTC1597ACG	28-Lead Plastic SSOP	0°C to 70°C
LTC1597-1ACG#PBF	LTC1597-1ACG#TRPBF	LTC1597-1ACG	28-Lead Plastic SSOP	0°C to 70°C
LTC1597BCG#PBF	LTC1597BCG#TRPBF	LTC1597BCG	28-Lead Plastic SSOP	0°C to 70°C
LTC1597-1BCG#PBF	LTC1597-1BCG#TRPBF	LTC1597-1BCG	28-Lead Plastic SSOP	0°C to 70°C
LTC1597AIG#PBF	LTC1597AIG#TRPBF	LTC1597AIG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1597-1AIG#PBF	LTC1597-1AIG#TRPBF	LTC1597-1AIG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1597BIG#PBF	LTC1597BIG#TRPBF	LTC1597BIG	28-Lead Plastic SSOP	-40°C to 85°C
LTC1597-1BIG#PBF	LTC1597-1BIG#TRPBF	LTC1597-1BIG	28-Lead Plastic SSOP	-40°C to 85°C
OBSOLETE PACKAGE				
LTC1591CN#PBF	LTC1591CN#TRPBF	LTC1591CN	28-Lead Narrow PDIP	0°C to 70°C
LTC1591-1CN#PBF	LTC1591-1CN#TRPBF	LTC1591-1CN	28-Lead Narrow PDIP	0°C to 70°C
LTC1591IN#PBF	LTC1591IN#TRPBF	LTC1591IN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1591-1IN#PBF	LTC1591-1IN#TRPBF	LTC1591-1IN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1597ACN#PBF	LTC1597ACN#TRPBF	LTC1597ACN	28-Lead Narrow PDIP	0°C to 70°C
LTC1597-1ACN#PBF	LTC1597-1ACN#TRPBF	LTC1597-1ACN	28-Lead Narrow PDIP	0°C to 70°C
LTC1597BCN#PBF	LTC1597BCN#TRPBF	LTC1597BCN	28-Lead Narrow PDIP	0°C to 70°C
LTC1597-1BCN#PBF	LTC1597-1BCN#TRPBF	LTC1597-1BCN	28-Lead Narrow PDIP	0°C to 70°C
LTC1597AIN#PBF	LTC1597AIN#TRPBF	LTC1597AIN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1597-1AIN#PBF	LTC1597-1AIN#TRPBF	LTC1597-1AIN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1597BIN#PBF	LTC1597BIN#TRPBF	LTC1597BIN	28-Lead Narrow PDIP	-40°C to 85°C
LTC1597-1BIN#PBF	LTC1597-1BIN#TRPBF	LTC1597-1BIN	28-Lead Narrow PDIP	-40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges.

Consult LTC Marketing for information on nonstandard lead based finish parts.

For more information on lead free part markings, go to: <http://www.linear.com/leadfree/>

For more information on tape and reel specifications, go to: <http://www.linear.com/tapeandreel/>

ELECTRICAL CHARACTERISTICS

$V_{CC} = 5V \pm 10\%$, $V_{REF} = 10V$, $I_{OUT1} = AGND = DGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

				LTC1591/-1			LTC1597B/-1B			LTC1597A/-1A				
SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	UNITS	
Accuracy														
	Resolution		●	14			16			16			Bits	
	Monotonicity		●	14			16			16			Bits	
INL	Integral Nonlinearity	(Note 2) T _A = 25°C T _{MIN} to T _{MAX}	●			±1 ±1			±2 ±2			±0.25 ±0.35	±1 ±1	LSB LSB
DNL	Differential Nonlinearity	T _A = 25°C T _{MIN} to T _{MAX}	●			±1 ±1			±1 ±1			±0.2 ±0.2	±1 ±1	LSB LSB
GE	Gain Error	Unipolar Mode (Note 3) T _A = 25°C T _{MIN} to T _{MAX}	●			±4 ±6			±16 ±24			2 3	±16 ±16	LSB LSB
		Bipolar Mode (Note 3) T _A = 25°C T _{MIN} to T _{MAX}	●			±4 ±6			±16 ±24			2 3	±16 ±16	LSB LSB
	Gain Temperature Coefficient	(Note 4) ΔGain/ΔTemperature	●		1	2			1	2		1	2	ppm/°C
	Bipolar Zero-Scale Error	T _A = 25°C T _{MIN} to T _{MAX}	●			±3 ±5			±10 ±16				±5 ±8	LSB LSB
I _{LKG}	OUT1 Leakage Current	(Note 5) T _A = 25°C T _{MIN} to T _{MAX}	●			±5 ±15			±5 ±15				±5 ±15	nA nA
PSRR	Power Supply Rejection Ratio	V _{CC} = 5V ±10	●		±0.1	±1			±0.4	±2		±0.4	±2	LSB/V

$V_{CC} = 5V \pm 10\%$, $V_{REF} = 10V$, $I_{OUT1} = AGND = DGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Reference Input							
R _{REF}	DAC Input Resistance (Unipolar)	(Note 6)	●	4.5	6	10	kΩ
R1/R2	R1/R2 Resistance (Bipolar)	(Notes 6, 13)	●	9	12	20	kΩ
R _{OFS} , R _{FB}	Feedback and Offset Resistances	(Note 6)	●	9	12	20	kΩ

AC Performance (Note 4)

	Output Current Settling Time	(Notes 7, 8)			1	μs
	Mid-Scale Glitch Impulse	(Note 12)			2	nV-s
	Digital-to-Analog Glitch Impulse	(Note 9)			1	nV-s
	Multiplying Feedthrough Error	$V_{REF} = \pm 10V$, 10kHz Sine Wave			1	mV _{P-P}
THD	Total Harmonic Distortion	(Note 10)			108	dB
	Output Noise Voltage Density	(Note 11)			10	nV/ $\sqrt{Hz}$
	Harmonic Distortion (Digital Waveform Generation)	Unipolar Mode (Note 14)				
		2nd Harmonic			94	dB
		3rd Harmonic			101	dB
		SFDR			94	dB
		Bipolar Mode (Note 14)				
		2nd Harmonic			94	dB
		3rd Harmonic			101	dB
		SFDR			94	dB

ELECTRICAL CHARACTERISTICS

The ● denotes specifications that apply over the full operating temperature range. $V_{CC} = 5V \pm 10\%$, $V_{REF} = 10V$, $I_{OUT1} = AGND = DGND = 0V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Analog Outputs (Note 4)							
C _{OUT}	Output Capacitance (Note 4)	DAC Register Loaded to All 1s: C _{OUT1}	●		115	130	pF
		DAC Register Loaded to All 0s: C _{OUT1}	●		70	80	pF
Digital Inputs							
V _{IH}	Digital Input High Voltage		●	2.4			V
V _{IL}	Digital Input low Voltage		●			0.8	V
I _{IN}	Digital Input Current		●	0.001		±1	μA
C _{IN}	Digital Input Capacitance	(Note 4) V _{IN} = 0V	●			8	pF
Timing Characteristics							
t _{DS}	Data to $\overline{WR}$ Setup Time		●	60			ns
t _{DH}	Data to $\overline{WR}$ Hold Time		●	0			ns
t _{WR}	$\overline{WR}$ Pulse Width		●	60			ns
t _{LD}	LD Pulse Width		●	110			ns
t _{CLR}	Clear Pulse Width		●	60			ns
t _{LWD}	$\overline{WR}$ to LD Delay Time		●	0			ns
Power Supply							
V _{DD}	Supply Voltage		●	4.5	5	5.5	V
I _{DD}	Supply Current	Digital Inputs = 0V or V _{CC}	●			10	μA

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: $\pm 1LSB = \pm 0.006\%$ of full scale = $\pm 61ppm$ of full scale for the LTC1591/LTC1591-1. $\pm 1LSB = \pm 0.0015\%$ of full scale = $\pm 15.3ppm$ of full scale for the LTC1597/LTC1597-1.

Note 3: Using internal feedback resistor.

Note 4: Guaranteed by design, not subject to test.

Note 5: $I_{(OUT1)}$ with DAC register loaded to all 0s.

Note 6: Typical temperature coefficient is 100ppm/°C.

Note 7: I_{OUT1} load = 100 Ω in parallel with 13pF.

Note 8: To 0.006% for a full-scale change, measured from the rising edge of LD for the LTC1591/LTC1591-1. To 0.0015% for a full-scale change, measured from the rising edge of LD for the LTC1597/LTC1597-1.

Note 9: $V_{REF} = 0V$. DAC register contents changed from all 0s to all 1s or all 1s to all 0s.

Note 10: $V_{REF} = 6V_{RMS}$ at 1kHz. DAC register loaded with all 1s.

Note 11: Calculation from $e_n = \sqrt{4kTRB}$ where: k = Boltzmann constant (J/°K), R = resistance (Ω), T = temperature (°K), B = bandwidth (Hz).

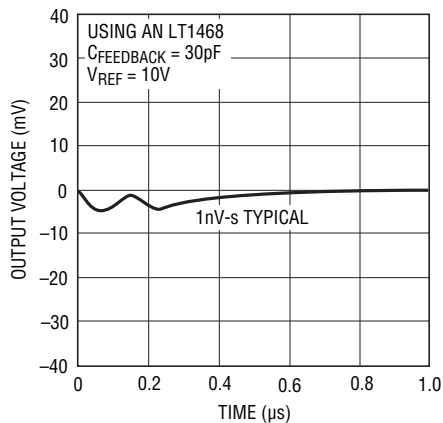
Note 12: Mid-scale transition code: 01 1111 1111 1111 to 10 0000 0000 0000 for the LTC1591/LTC1591-1 and 0111 1111 1111 1111 to 1000 0000 0000 0000 for the LTC1597/LTC1597-1.

Note 13: R1 and R2 are measured between R1 and R_{COM} , REF and R_{COM} .

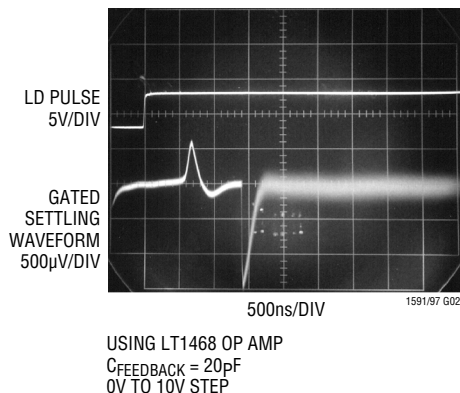
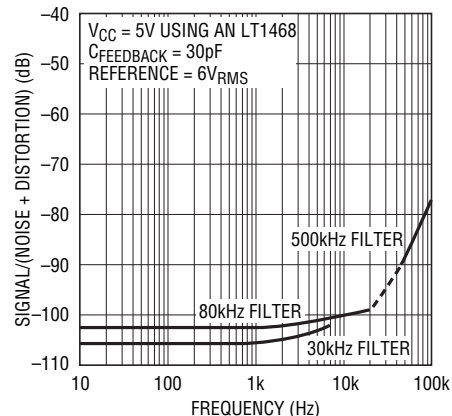
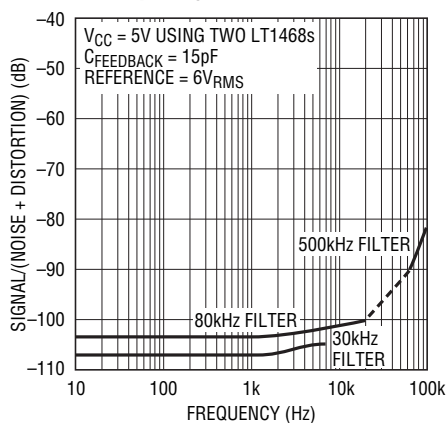
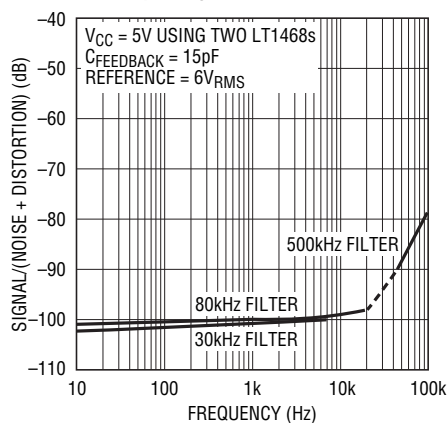
Note 14: Measured using the LT1468 op amp in unipolar mode for I/V converter and LT1468 I/V and LT1001 reference inverter in bipolar mode. Sample Rate = 50kHz, Signal Frequency = 1kHz, $V_{REF} = 5V$, $T_A = 25^\circ C$.

TYPICAL PERFORMANCE CHARACTERISTICS (LTC1591/LTC1597)

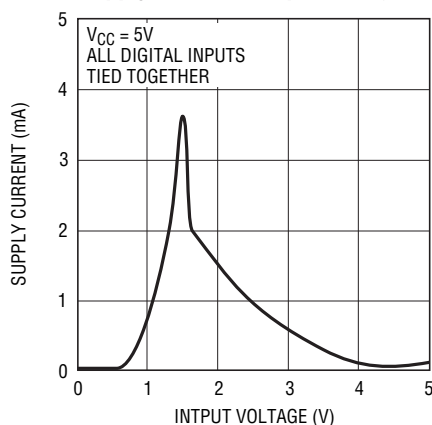
Mid-Scale Glitch Impulse



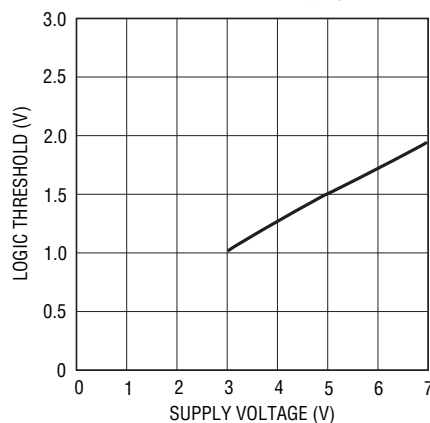
Full-Scale Settling Waveform

Unipolar Multiplying Mode
Signal-to-(Noise + Distortion)
vs FrequencyBipolar Multiplying Mode
Signal-to-(Noise + Distortion)
vs Frequency, Code = All ZerosBipolar Multiplying Mode
Signal-to-(Noise + Distortion)
vs Frequency, Code = All Ones

Supply Current vs Input Voltage

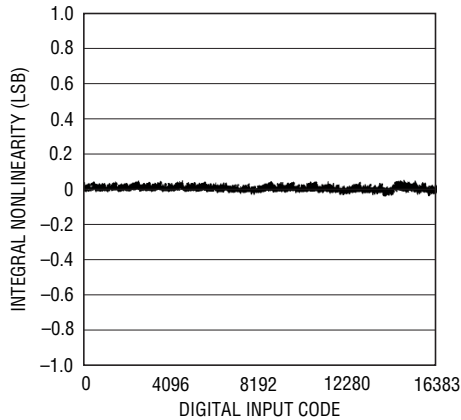


Logic Threshold vs Supply Voltage



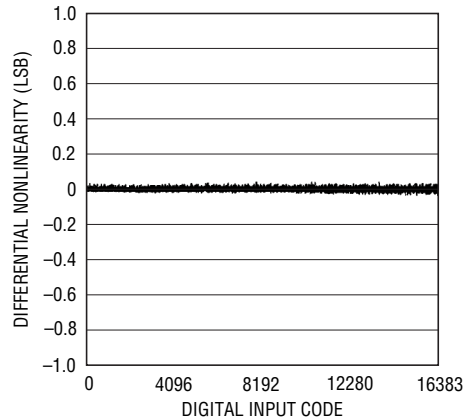
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1591)

Integral Nonlinearity (INL)



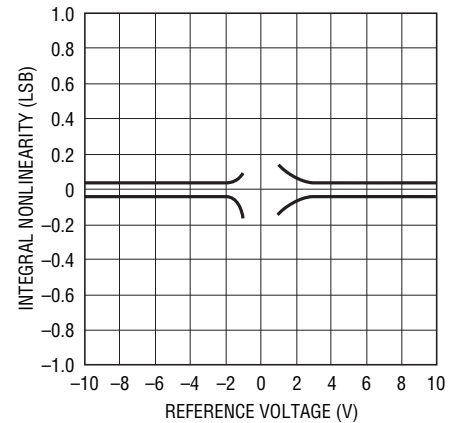
1591 G01

Differential Nonlinearity (DNL)



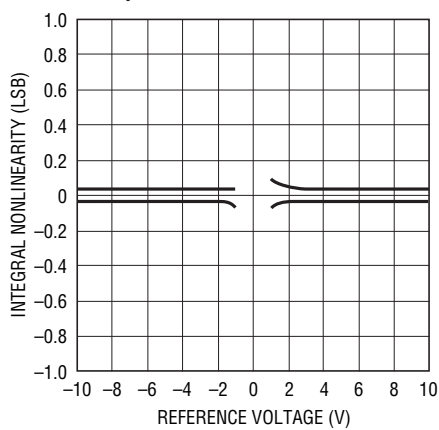
1591 G02

Integral Nonlinearity vs Reference Voltage in Unipolar Mode



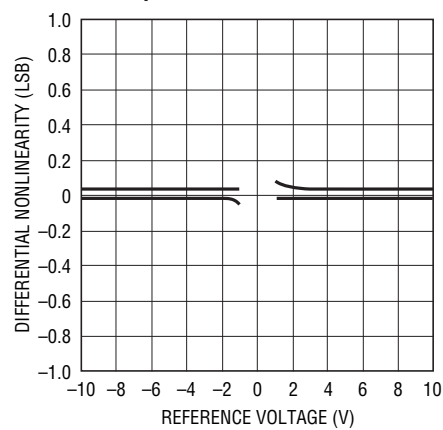
1591 G03

Integral Nonlinearity vs Reference Voltage in Bipolar Mode



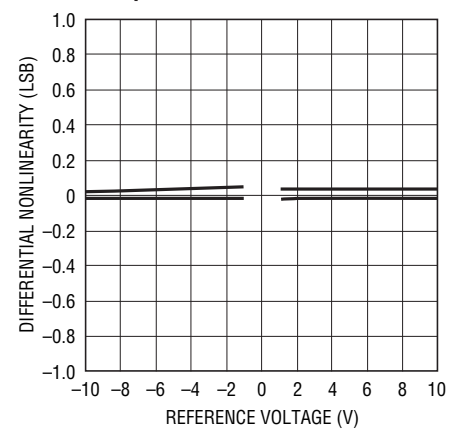
1591 G04

Differential Nonlinearity vs Reference Voltage in Unipolar Mode



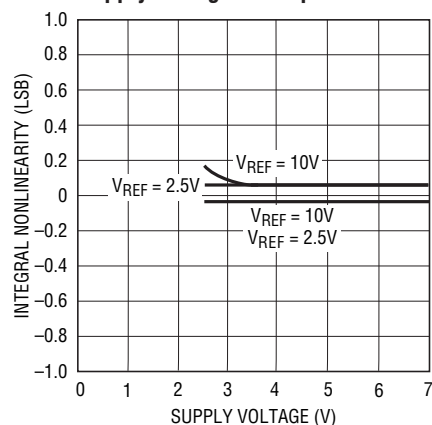
1591 G05

Differential Nonlinearity vs Reference Voltage in Bipolar Mode



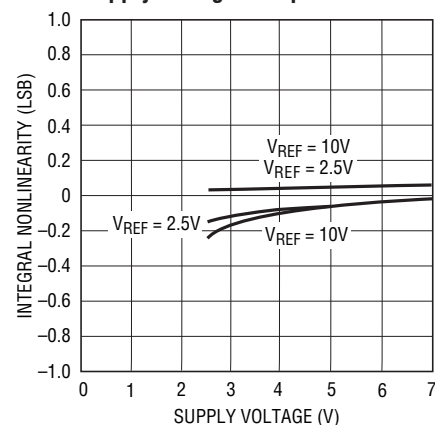
1591 G06

Integral Nonlinearity vs Supply Voltage in Unipolar Mode



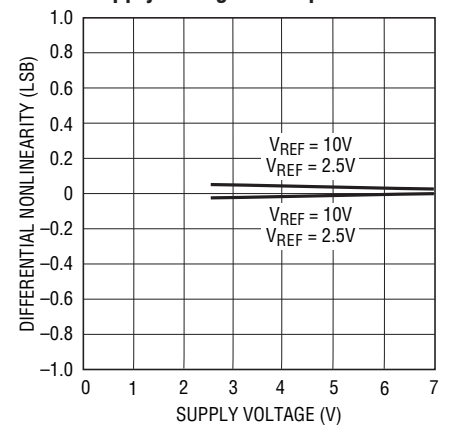
1591 G07

Integral Nonlinearity vs Supply Voltage in Bipolar Mode



1591 G08

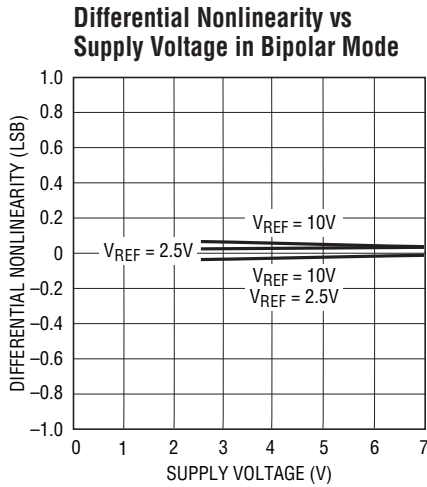
Differential Nonlinearity vs Supply Voltage in Unipolar Mode



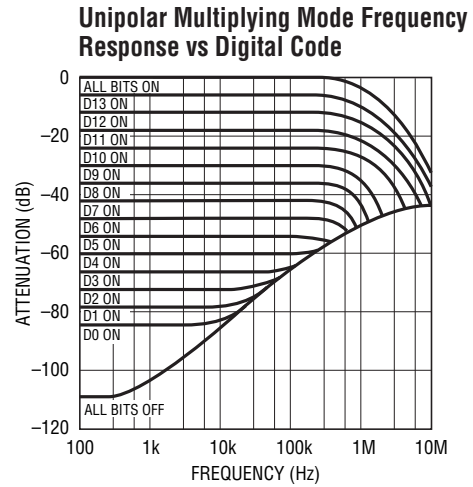
1591 G09

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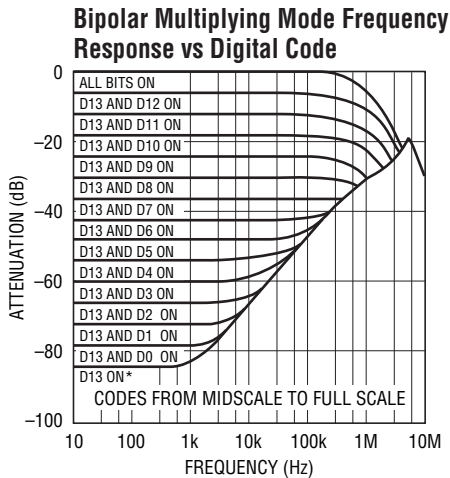
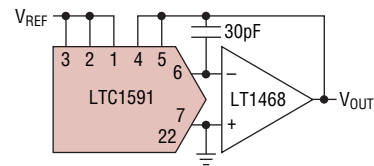
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1591)



1591 G10

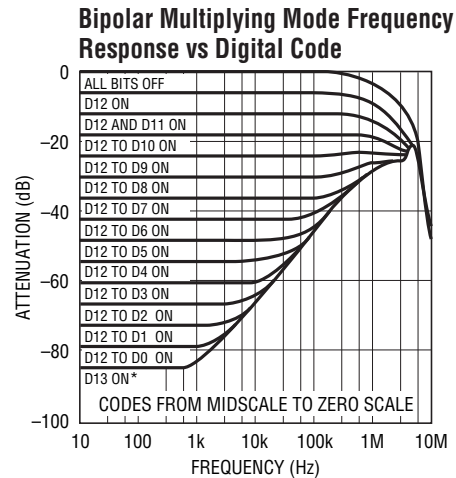
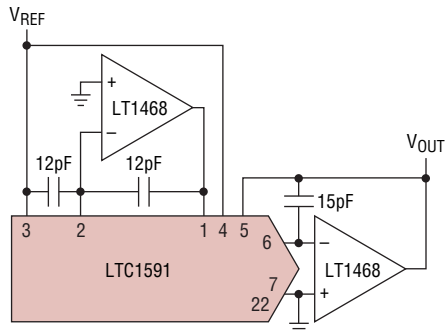


1591 G11



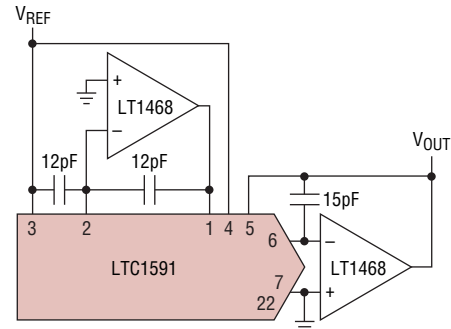
1591 G12

*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO -84dB TYPICAL (-70dB MAX)



1591 G13

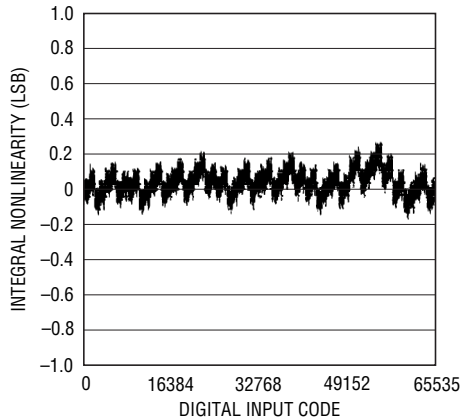
*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO -84dB TYPICAL (-70dB MAX)



15917fb

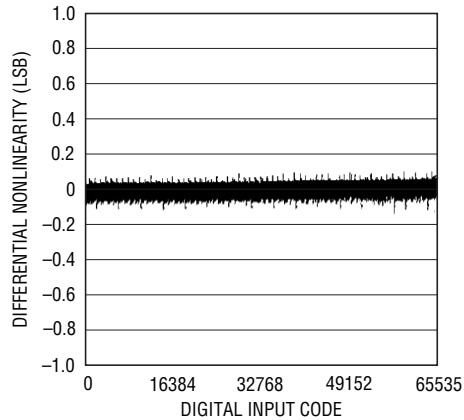
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1597)

Integral Nonlinearity (INL)



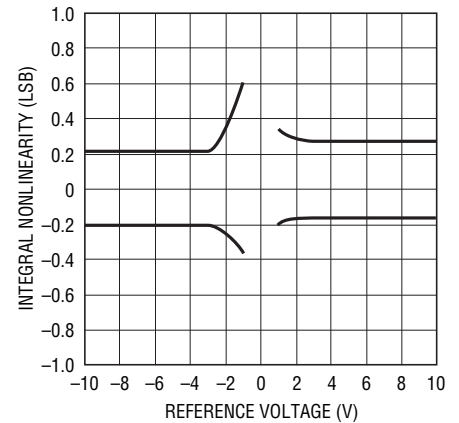
1597 G01

Differential Nonlinearity (DNL)



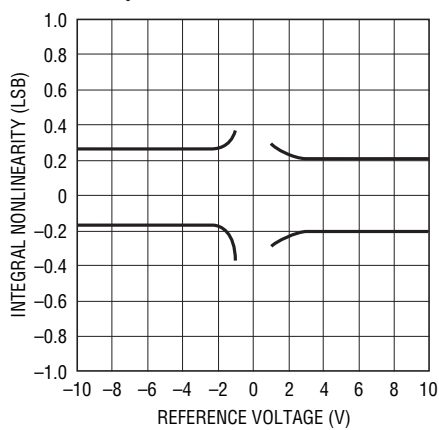
1597 G02

Integral Nonlinearity vs Reference Voltage in Unipolar Mode



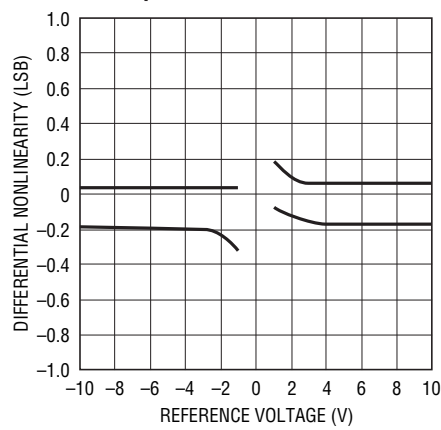
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Integral Nonlinearity vs Reference Voltage in Bipolar Mode



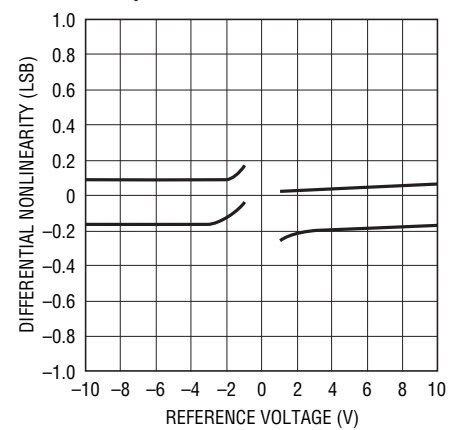
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Differential Nonlinearity vs Reference Voltage in Unipolar Mode



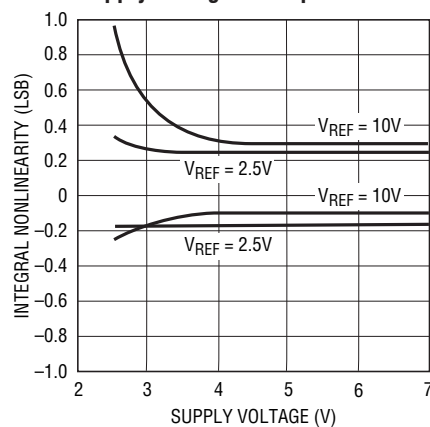
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Differential Nonlinearity vs Reference Voltage in Bipolar Mode



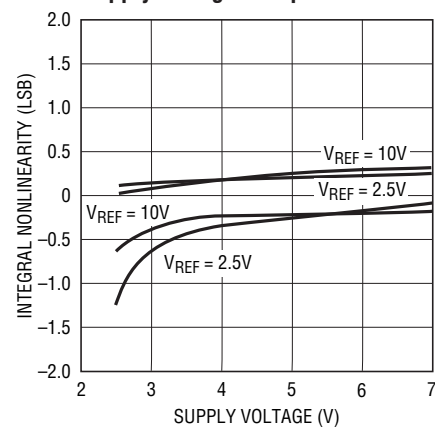
1597 G06

Integral Nonlinearity vs Supply Voltage in Unipolar Mode



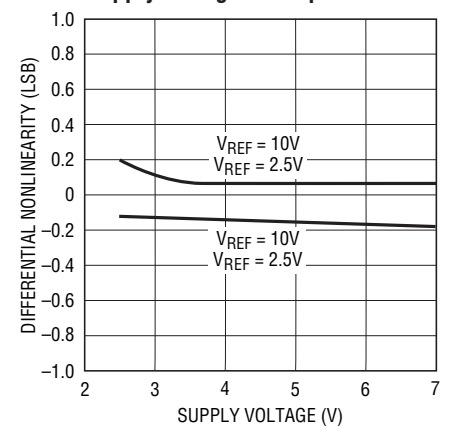
1597 G07

Integral Nonlinearity vs Supply Voltage in Bipolar Mode



1597 G08

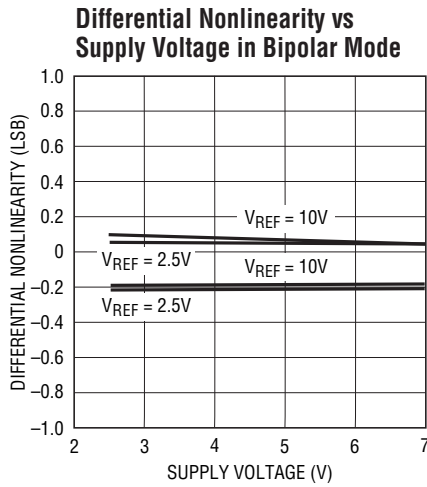
Differential Nonlinearity vs Supply Voltage in Unipolar Mode



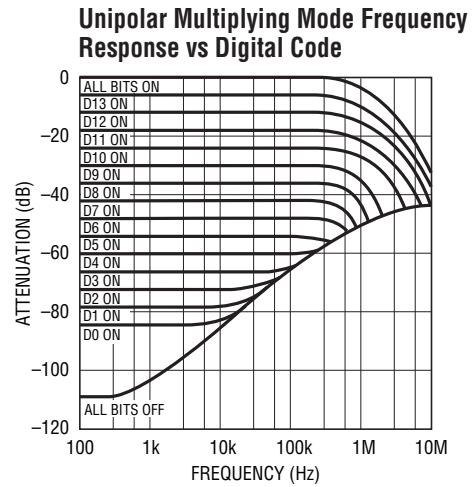
1597 G09

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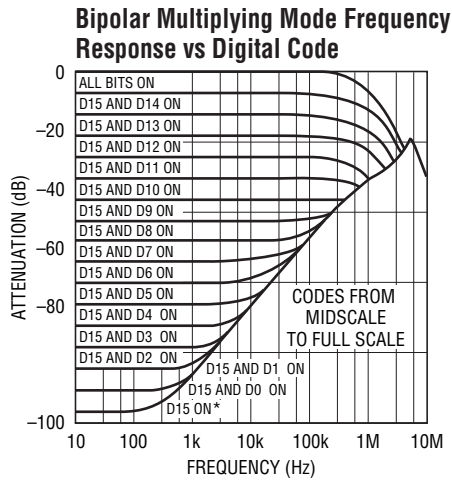
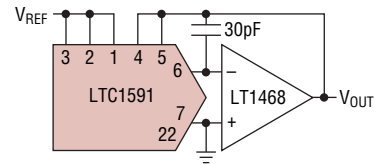
TYPICAL PERFORMANCE CHARACTERISTICS (LTC1597)



1597 G10

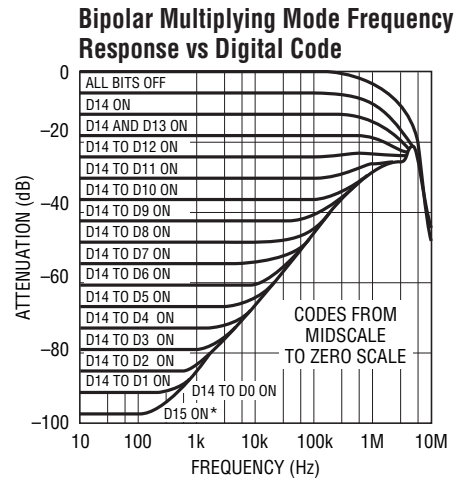
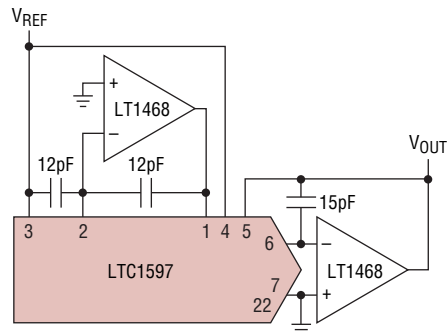


1591 G11



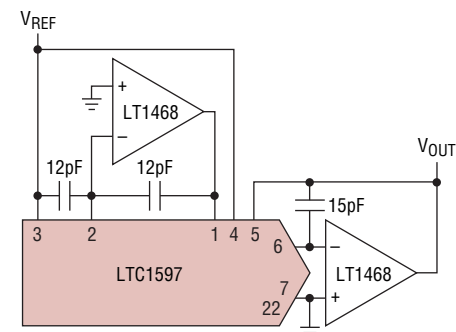
1597 G12

*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO -96dB TYPICAL (-78dB MAX, A GRADE)



1597 G13

*DAC ZERO VOLTAGE OUTPUT LIMITED BY BIPOLAR ZERO ERROR TO -96dB TYPICAL (-78dB MAX, A GRADE)



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PIN FUNCTIONS

LTC1591

REF (Pin 1): Reference Input and 4-Quadrant Resistor R2. Typically $\pm 10V$, accepts up to $\pm 25V$. In 2-Quadrant mode this is the reference input. In 4-quadrant mode, this pin is driven by external inverting reference amplifier.

R_{COM} (Pin 2): Center Tap Point of the Two 4-Quadrant Resistors R1 and R2. Normally tied to the inverting input of an external amplifier in 4-quadrant operation, otherwise shorted to the REF pin. See Figures 1a and 2a.

R1 (Pin 3): 4-Quadrant Resistor R1. In 2-quadrant operation short to the REF pin. In 4-quadrant mode tie to R_{OFFS} (Pin 4).

R_{OFFS} (Pin 4): Bipolar Offset Resistor. Typically swings $\pm 10V$, accepts up to $\pm 25V$. In 2-quadrant operation tie to R_{FB}. In 4-quadrant operation tie to R1.

R_{FB} (Pin 5): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp. Swings to $\pm V_{REF}$. V_{REF} is typically $\pm 10V$.

I_{OUT1} (Pin 6): DAC Current Output. Tie to the inverting input of the current to voltage converter op amp.

AGND (Pin 7): Analog Ground. Tie to ground.

LD (Pin 8): DAC Digital Input Load Control Input. When LD is taken to a logic high, data is loaded from the input register into the DAC register, updating the DAC output.

WR (Pin 9): DAC Digital Write Control Input. When $\overline{WR}$ is taken to a logic low, data is loaded from the digital input pins into the 14-bit wide input register.

DB13 to D2 (Pins 10 to 21): Digital Input Data Bits.

DGND (Pin 22): Digital Ground. Tie to ground.

V_{CC} (Pin 23): The Positive Supply Input. $4.5V \leq V_{CC} \leq 5.5V$. Requires a bypass capacitor to ground.

DB1, DB0 (Pins 24, 25): Digital Input Data Bits.

NC (Pins 26, 27): No Connect.

CLR (Pin 28): Digital Clear Control Function for the DAC. When $\overline{CLR}$ is taken to a logic low, it sets the DAC output and all internal registers to zero code for the LTC1591 and mid-scale code for the LTC1591-1.

PIN FUNCTIONS

LTC1597

REF (Pin 1): Reference Input and 4-Quadrant Resistor R2. Typically $\pm 10V$, accepts up to $\pm 25V$. In 2-Quadrant mode this is the reference input. In 4-quadrant mode, this pin is driven by external inverting reference amplifier.

R_{COM} (Pin 2): Center Tap Point of the Two 4-Quadrant Resistors R1 and R2. Normally tied to the inverting input of an external amplifier in 4-quadrant operation, otherwise shorted to the REF pin. See Figures 1b and 2b.

R1 (Pin 3): 4-Quadrant Resistor R1. In 2-quadrant operation short to the REF pin. In 4-quadrant mode tie to R_{OFFS} (Pin 4).

R_{OFFS} (Pin 4): Bipolar Offset Resistor. Typically swings $\pm 10V$, accepts up to $\pm 25V$. In 2-quadrant operation tie to R_{FB}. In 4-quadrant operation tie to R1.

R_{FB} (Pin 5): Feedback Resistor. Normally tied to the output of the current to voltage converter op amp. Swings to $\pm V_{REF}$. V_{REF} is typically $\pm 10V$.

I_{OUT1} (Pin 6): DAC Current Output. Tie to the inverting input of the current to voltage converter op amp.

AGND (Pin 7): Analog Ground. Tie to ground.

LD (Pin 8): DAC Digital Input Load Control Input. When LD is taken to a logic high, data is loaded from the input register into the DAC register, updating the DAC output.

WR (Pin 9): DAC Digital Write Control Input. When $\overline{WR}$ is taken to a logic low, data is loaded from the digital input pins into the 16-bit wide input register.

DB15 to D4 (Pins 10 to 21): Digital Input Data Bits.

DGND (Pin 22): Digital Ground. Tie to ground.

V_{CC} (Pin 23): The Positive Supply Input. $4.5V \leq V_{CC} \leq 5.5V$. Requires a bypass capacitor to ground.

DB3 to DB0 (Pins 24 to 27): Digital Input Data Bits.

CLR (Pin 28): Digital Clear Control Function for the DAC. When $\overline{CLR}$ is taken to a logic low, it sets the DAC output and all internal registers to zero code for the LTC1597 and mid-scale code for the LTC1597-1.

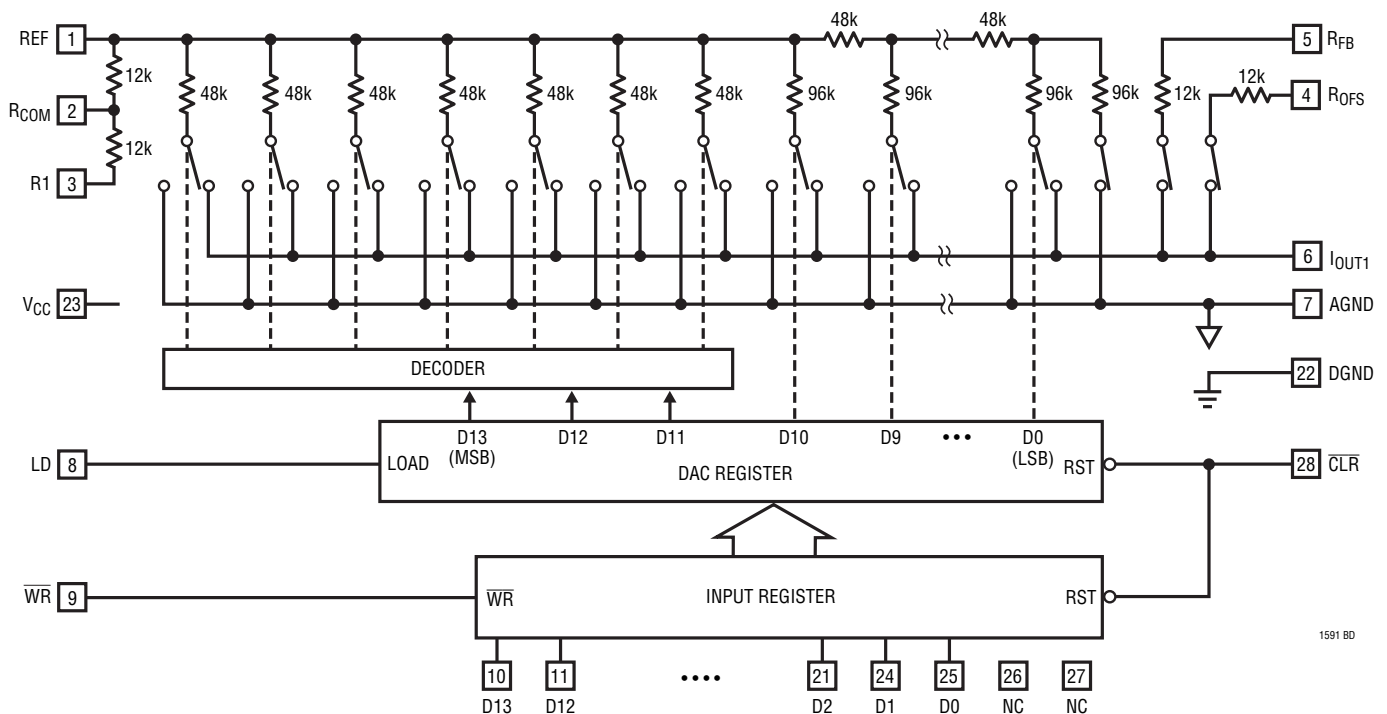
TRUTH TABLE

Table 1

CONTROL INPUTS			REGISTER OPERATION
CLR	WR	LD	
0	X	X	Reset Input and DAC Register to All 0s for LTC1591/LTC1597 and Mid-Scale for LTC1591-1/LTC1597-1 (Asynchronous Operation)
1	0	0	Load Input Register with All 14/16 Data Bits
1	1	1	Load DAC Register with the Contents of the Input Register
1			Input and DAC Register Are Transparent
1			CLK = LD and WR Tied Together. The 14/16 Data Bits Are Loaded into the Input Register on the Falling Edge of the CLK and Then Loaded into the DAC Register on the Rising Edge of the CLK
1	1	0	No Register Operation

BLOCK DIAGRAMS

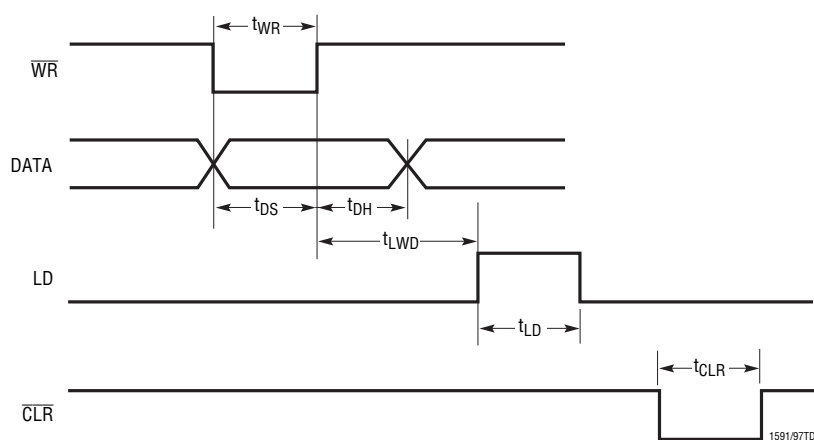
LTC1591



1591 BD

The schematic diagram illustrates the internal architecture of the DAC0808. It features a DAC REGISTER (D0-D15) and an INPUT REGISTER (D0-D15). The DAC core consists of a ladder network of resistors (48k, 96k, 12k) and switches. The output is taken from IOUT1. The diagram also shows the connection of the DAC to the microcontroller via the LD (8) and WR (9) pins, and the CLR (28) pin. The DAC is powered by REF (1) and RCOM (2) pins, and the output is connected to RFB (5) and ROFS (4) pins. The DAC is also connected to the microcontroller via the IOUT1 (6) and AGND (7) pins. The DAC is connected to the microcontroller via the DGND (22) pin. The DAC is connected to the microcontroller via the CLR (28) pin.

TIMING DIAGRAM



APPLICATIONS INFORMATION

Description

The LTC1591/LTC1597 are 14-/16-bit multiplying, current output DACs with a full parallel 14-/16-bit digital interface. The devices operate from a single 5V supply and provide both unipolar 0V to -10V or 0V to 10V and bipolar $\pm 10\text{V}$ output ranges from a 10V or -10V reference input. They have three additional precision resistors on chip for bipolar operation. Refer to the block diagrams regarding the following description.

The 14-/16-bit DACs consist of a precision R-2R ladder for the 11/13LSBs. The 3MSBs are decoded into seven segments of resistor value R. Each of these segments and the R-2R ladder carries an equally weighted current of one eighth of full scale. The feedback resistor R_{FB} and 4-quadrant resistor R_{OFS} have a value of $R/4$. 4-quadrant resistors R_1 and R_2 have a magnitude of $R/4$. R_1 and R_2 together with an external op amp (see Figure 2) invert the reference input voltage and applies it to the 14-/16-bit DAC input REF, in 4-quadrant operation. The REF pin presents a constant input impedance of $R/8$ in unipolar mode and $R/12$ in bipolar mode. The output impedance of the current output pin I_{OUT1} varies with DAC input code. The I_{OUT1} capacitance due to the NMOS current steering switches also varies with input code from 70pF to 115pF. An added feature of these devices, especially for waveform generation, is a proprietary deglitcher that reduces glitch energy to below 2nV-s over the DAC output voltage range.

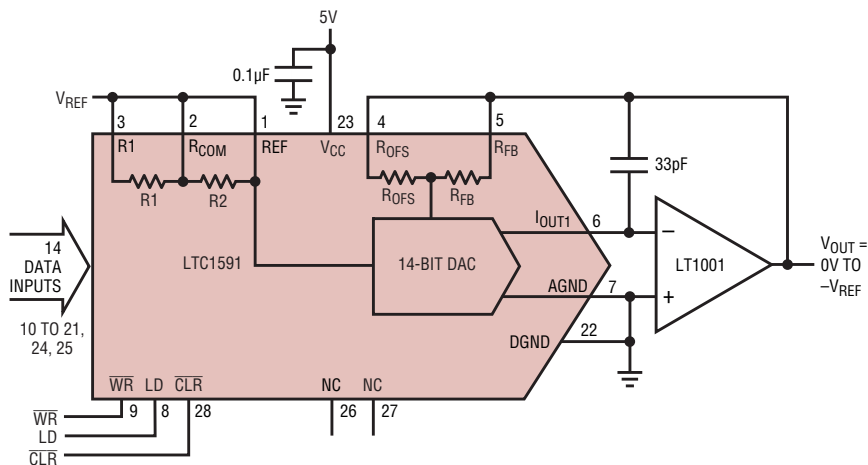
Digital Section

The LTC1591/LTC1597 are 14-/16-bit wide full parallel data bus inputs. The devices are double-buffered with two 14-/16-bit registers. The double-buffered feature permits the update of several DACs simultaneously. The input register is loaded directly from a 16-bit microprocessor bus when the $\overline{\text{WR}}$ pin is brought to a logic low level. The second register (DAC register) is updated with the data from the input register when the $\overline{\text{LD}}$ pin is brought to a logic high level. Updating the DAC register updates the DAC output with the new data. To make both registers transparent for flowthrough mode, tie $\overline{\text{WR}}$ low and $\overline{\text{LD}}$ high. However, this defeats the deglitcher operation and output glitch impulse may increase. The deglitcher is activated on the rising edge of the $\overline{\text{LD}}$ pin. The versatility of the interface also allows the use of the input and DAC registers in a master slave or edge-triggered configuration. This mode of operation occurs when $\overline{\text{WR}}$ and $\overline{\text{LD}}$ are tied together. The asynchronous clear pin resets the LTC1591/LTC1597 to zero scale and the LTC1591-1/LTC1597-1 to mid-scale. $\overline{\text{CLR}}$ resets both the input and DAC registers. These devices also have a power-on reset. Table 1 shows the truth table for the LTC1591/LTC1597.

Unipolar Mode

(2-Quadrant Multiplying, $V_{OUT} = 0\text{V}$ to $-V_{REF}$)

The LTC1591/LTC1597 can be used with a single op amp to provide 2-quadrant multiplying operation as shown in Figure 1. With a fixed -10V reference, the circuits shown give a precision unipolar 0V to 10V output swing.



Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB		LSB		
1111	1111	1111	11	$-V_{REF}$ (16,383/16,384)
1000	0000	0000	00	$-V_{REF}$ (8,192/16,384) = $-V_{REF}/2$
0000	0000	0000	01	$-V_{REF}$ (1/16,384)
0000	0000	0000	00	0V

1591/97 F01a

Figure 1a. Unipolar Operation (2-Quadrant Multiplication) $V_{OUT} = 0\text{V}$ to $-V_{REF}$

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APPLICATIONS INFORMATION

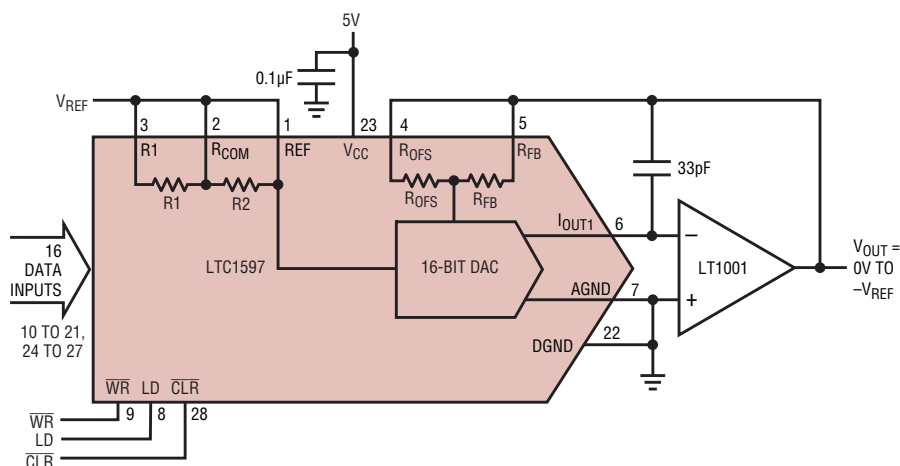


Figure 1b. Unipolar Operation (2-Quadrant Multiplication) $V_{OUT} = 0V$ to $-V_{REF}$

Unipolar Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V _{OUT}
MSB		LSB		
1111	1111	1111	1111	-V _{REF} (65,535/65,536)
1000	0000	0000	0000	-V _{REF} (32,768/65,536) = -V _{REF} /2
0000	0000	0000	0001	-V _{REF} (1/65,536)
0000	0000	0000	0000	0V

1591/97 F01b

Bipolar Mode

(4-Quadrant Multiplying, $V_{OUT} = -V_{REF}$ to V_{REF})

The LTC1591/LTC1597 contain on chip all the 4-quadrant resistors necessary for bipolar operation. 4-quadrant multiplying operation can be achieved with a minimum of external components, a capacitor and a dual op amp, as shown in Figure 2. With a fixed 10V reference, the circuit shown gives a precision bipolar -10V to 10V output swing.

Op Amp Selection

Because of the extremely high accuracy of the 14-/16-bit LTC1591/LTC1597, thought should be given to op amp selection in order to achieve the exceptional performance of which the part is capable. Fortunately, the sensitivity of INL and DNL to op amp offset has been greatly reduced compared to previous generations of multiplying DACs.

Op amp offset will contribute mostly to output offset and gain and will have minimal effect on INL and DNL. For the LTC1597, a 500 μ V op amp offset will cause about 0.55LSB INL degradation and 0.15LSB DNL degradation with a 10V full-scale range. The main effects of op amp offset will be a degradation of zero-scale error equal to the op amp offset, and a degradation of full-scale error

equal to twice the op amp offset. For the LTC1597, the same 500 μ V op amp offset (2mV offset for LTC1591) will cause a 3.3LSB zero-scale error and a 6.5LSB full-scale error with a 10V full-scale range.

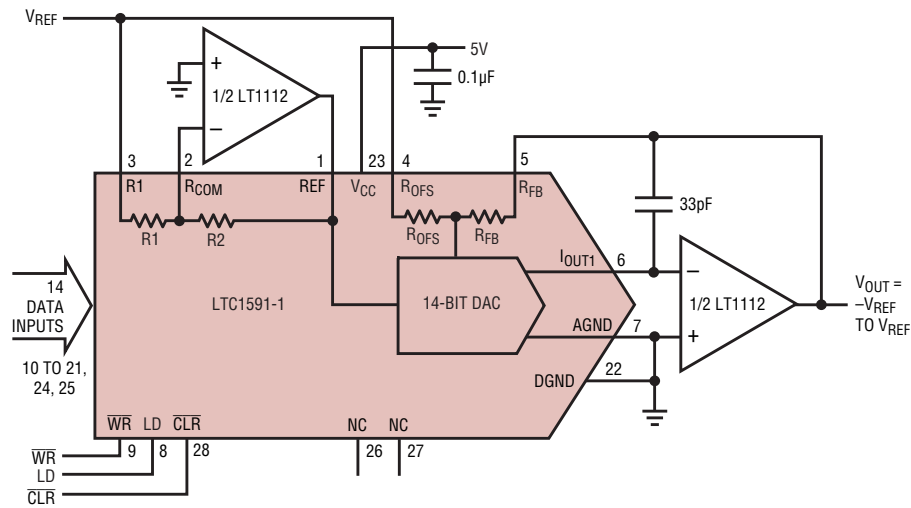
Op amp input bias current (I_{BIAS}) contributes only a zero-scale error equal to $I_{BIAS}(R_{FB}/R_{OFS}) = I_{BIAS}(6k)$. For a thorough discussion of 16-bit DAC settling time and op amp selection, refer to Application Note 74, “*Component and Measurement Advances Ensure 16-Bit DAC Settling Time*.”

Reference Input and Grounding

For optimum performance the reference input of the LTC1597 should be driven by a source impedance of less than 1k Ω . However, these DACs have been designed to minimize source impedance effects. An 8k Ω source impedance degrades both INL and DNL by 0.2LSB.

As with any high resolution converter, clean grounding is important. A low impedance analog ground plane and star grounding should be used. AGND must be tied to the star ground with as low a resistance as possible.

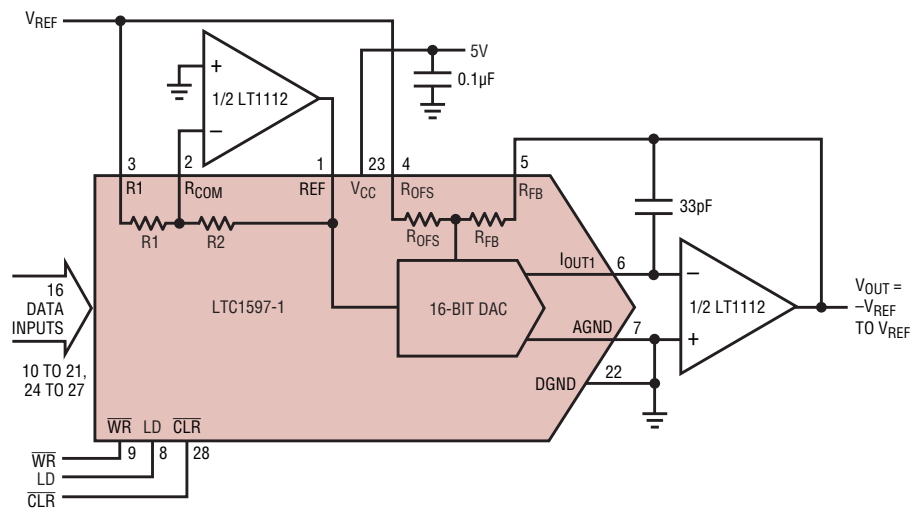
APPLICATIONS INFORMATION



Bipolar Offset Binary Code Table

DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB		LSB		
1111	1111	1111	11	V_{REF} (8,191/8,192)
1000	0000	0000	01	V_{REF} (1/8,192)
1000	0000	0000	00	0V
0111	1111	1111	11	$-V_{REF}$ (1/8,192)
0000	0000	0000	00	$-V_{REF}$

1591/97 F02a

Figure 2a. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF} 

Bipolar Offset Binary Code Table

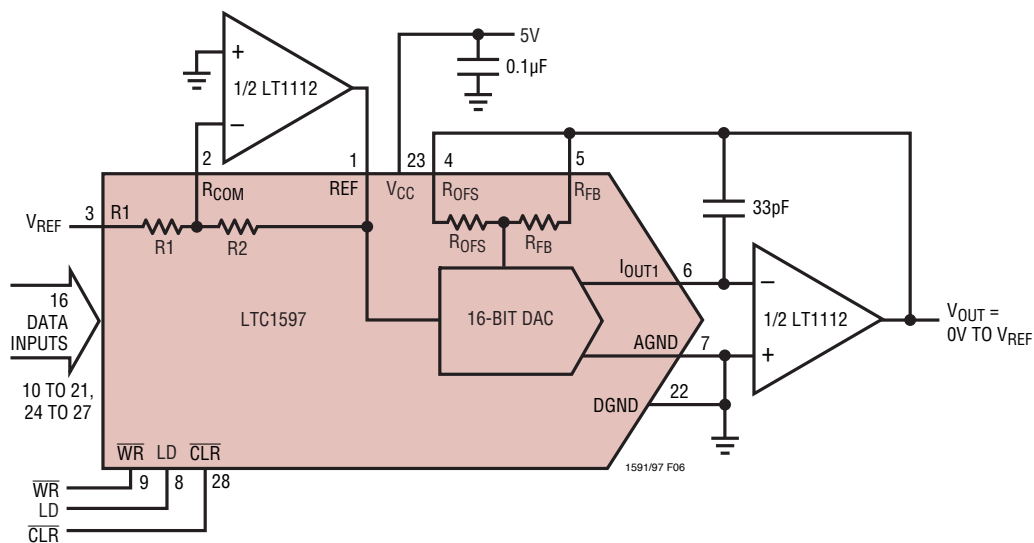
DIGITAL INPUT BINARY NUMBER IN DAC REGISTER				ANALOG OUTPUT V_{OUT}
MSB		LSB		
1111	1111	1111	1111	V_{REF} (32,767/32,768)
1000	0000	0000	0001	V_{REF} (1/32,768)
1000	0000	0000	0000	0V
0111	1111	1111	1111	$-V_{REF}$ (1/32,768)
0000	0000	0000	0000	$-V_{REF}$

1591/97 F02b

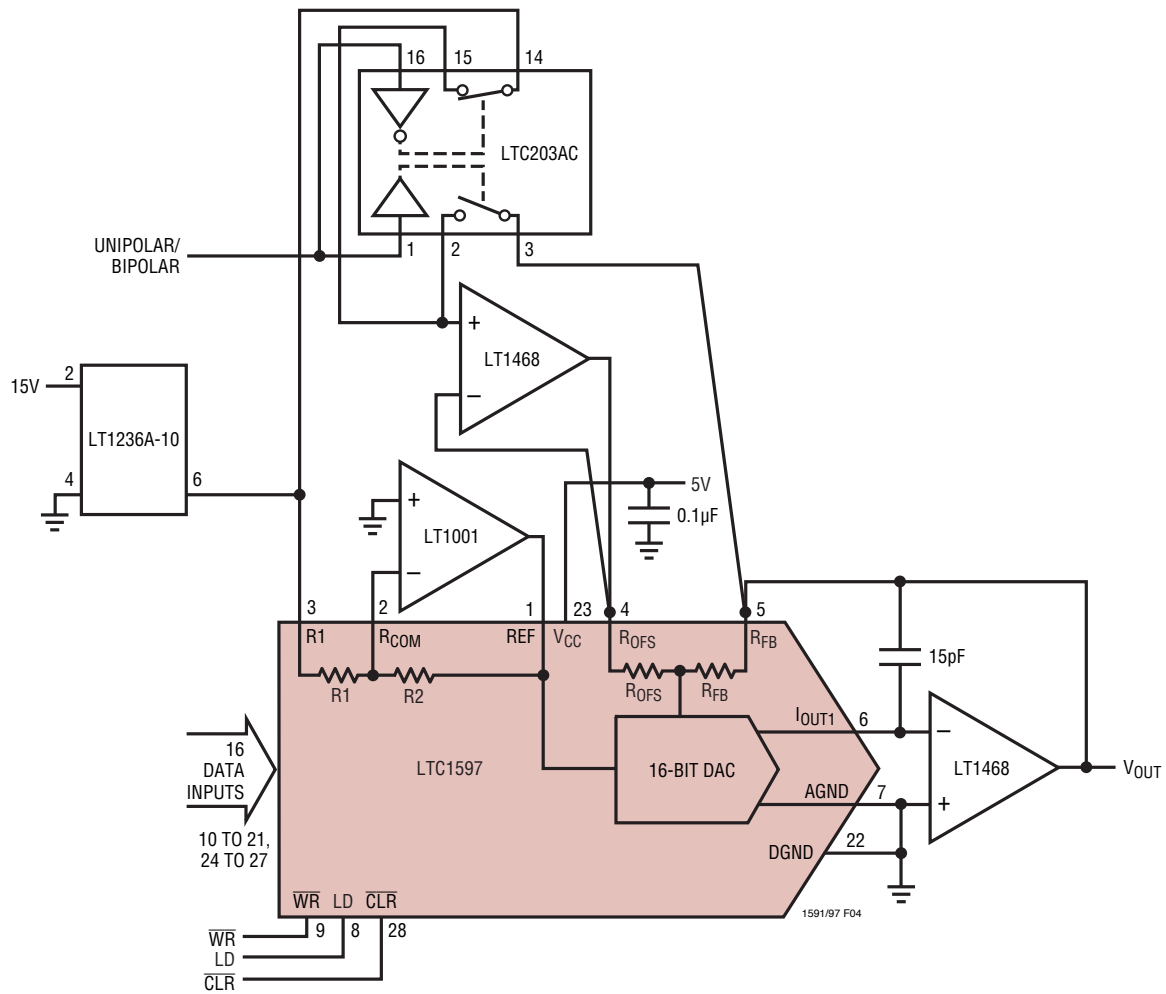
Figure 2b. Bipolar Operation (4-Quadrant Multiplication) $V_{OUT} = -V_{REF}$ to V_{REF}

TYPICAL APPLICATIONS

Noninverting Unipolar Operation (2-Quadrant Multiplication) $V_{OUT} = 0V$ to V_{REF}



TYPICAL APPLICATIONS

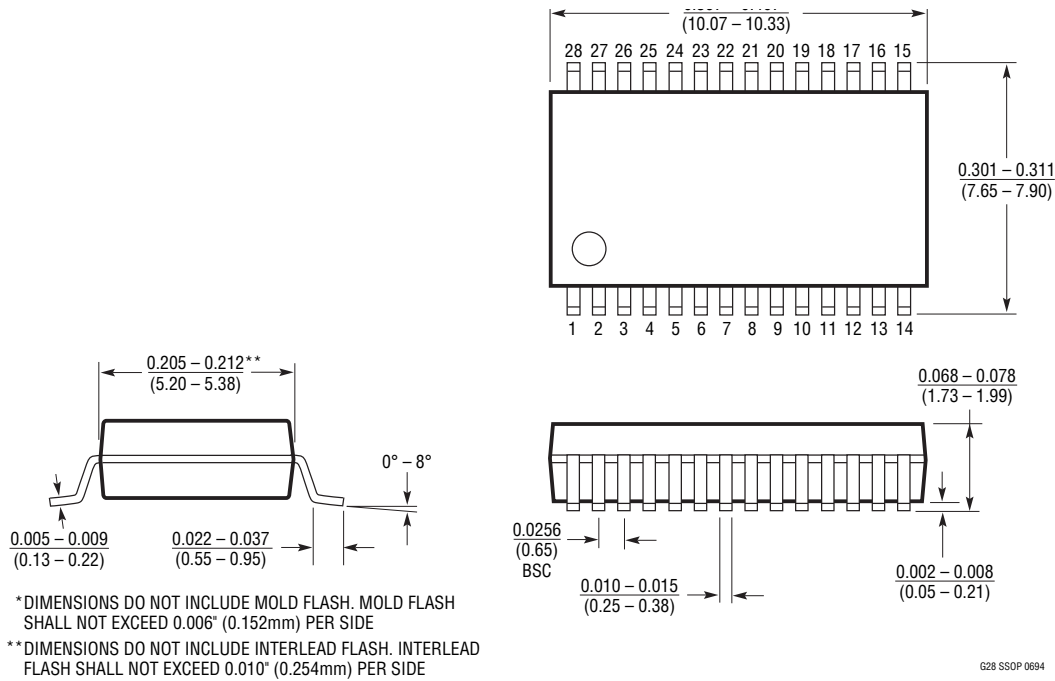
16-Bit V_{OUT} DAC Programmable Unipolar/Bipolar Configuration

The block diagram illustrates a digital PLL system. It begins with a **FREQUENCY CONTROL** section consisting of a **SERIAL OR BYTE LOAD REGISTER** and a **PARALLEL DELTA PHASE REGISTER M**. The output of the parallel register (n bits) is summed with the output of the serial register (n bits) at a summation node (Σ). This sum is fed into the **CLOCK** input of the **PHASE REGISTER**, which also receives an external **CLOCK** signal. The phase register's output (n bits) goes through **PHASE TRUNCATION 16 BITS** before entering the **SIN ROM LOOKUP TABLE**. The lookup table provides **16 DATA INPUTS** (bits 10 to 21 and 24 to 27) to the **LTC1597** DAC. The LTC1597 is configured as a 16-bit DAC with inputs **R1**, **R2**, **REF**, **VCC**, **R_OFS**, and **R_FB**. Its output **IOUT1** is connected to a feedback network consisting of resistors **R_OFS** and **R_FB**, and capacitors **15pF** and **0.1μF**. The feedback signal is fed back to the **LT1001** op-amp and the **LTC1597**'s **R_FB** input. The LT1001 op-amp is powered by a 5V supply and its non-inverting input is grounded. The output of the LT1001 is filtered by a **LOWPASS FILTER** to produce the final output frequency $f_0 = \frac{(M)(f_c)}{2^n}$.

PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.
Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

G Package 28-Lead Plastic SSOP (0.209) (LTC DWG # 05-08-1640)

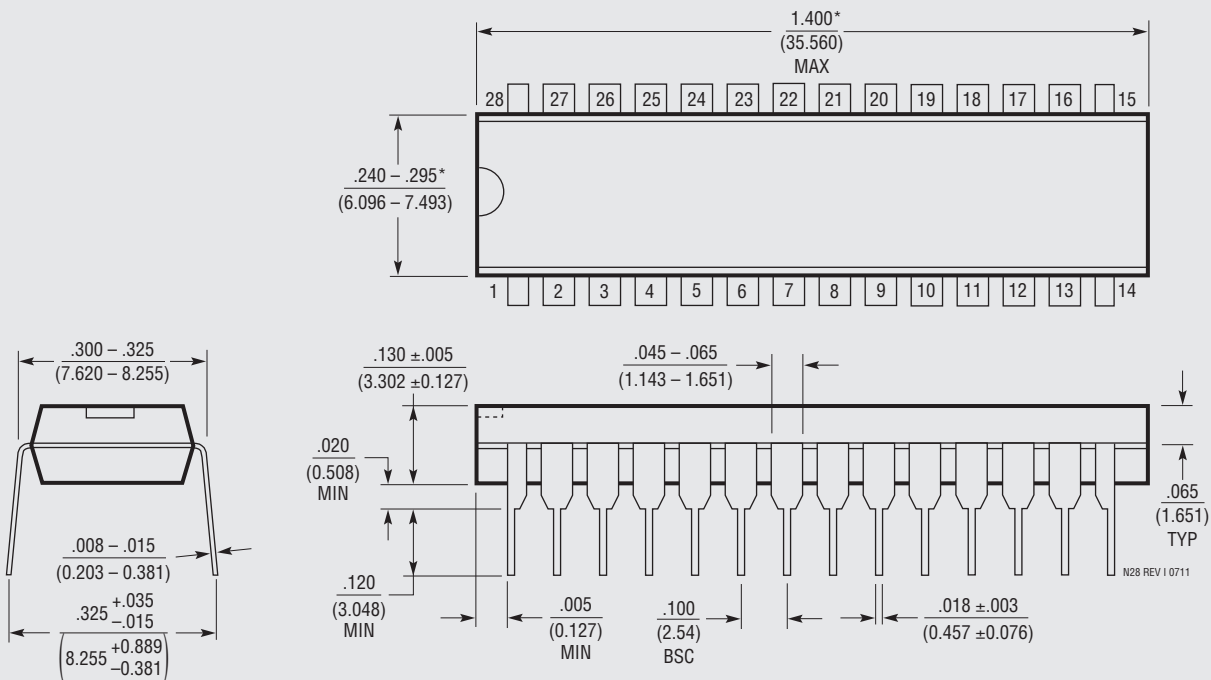


PACKAGE DESCRIPTION

Dimensions in inches (millimeters) unless otherwise noted.

Please refer to <http://www.linear.com/designtools/packaging/> for the most recent package drawings.

N Package
28-Lead Plastic PDIP (Narrow 0.300 Inch)
 (LTC DWG # 05-08-1510 Rev I)



NOTE:
1. DIMENSIONS ARE $\frac{\text{INCHES}}{\text{MILLIMETERS}}$

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

OBSOLETE PACKAGE

REVISION HISTORY (Revision history begins at Rev B)

REV	DATE	DESCRIPTION	PAGE NUMBER
B	07/15	Obsoleted 28-Lead PDIP Package	2, 3, 22

The schematic diagram illustrates the internal structure of the LTC1597 16-bit DAC. The main component is the LTC1597 chip, which contains a 16-BIT DAC core. The chip's pins are connected as follows:

- Power and Ground:** V_{CC} (pin 23) is connected to a 5V supply with a 0.1μF capacitor. AGND (pin 7) and DGND (pin 22) are connected to ground. A 20pF capacitor is connected between V_{CC} and AGND.
- Feedback and Output:** The feedback network consists of R_{FB} (pin 5) and R_{OFS} (pin 4). The output of the DAC core (I_{OUT1}, pin 6) is connected to the non-inverting input of an external LT1468 op-amp. The op-amp's output (V_{OUT}) is connected back to the feedback network.
- Reference and Input:** The reference voltage (REF, pin 1) is connected to a 15V supply through a network of resistors (R1, R2, RCOM) and a 15pF capacitor. The input data (16 DATA INPUTS, pins 10 to 21, 24 to 27) is connected to the DAC core.
- Control and Status:** The chip includes control pins (WR, LD, CLR, pins 9, 8, 28) and a status pin (SIGN BIT, pin 3).

The LTC1597 chip is shown in a red-shaded box, and the external 16-BIT DAC core is shown in a white box. The overall circuit is designed to provide a high-precision 16-bit digital-to-analog conversion.

RELATED PARTS

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