



74HC1G86-Q100; 74HCT1G86-Q100

2-input EXCLUSIVE-OR gate

Rev. 5 — 9 September 2025

Product data sheet

1. General description

The 74HC1G86-Q100; 74HCT1G86-Q100 is a single 2-input EXCLUSIVE-OR gate. Inputs include clamp diodes. This enables the use of current limiting resistors to interface inputs to voltages in excess of V_{CC} .

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 1) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 1)
 - Specified from -40 °C to +85 °C and from -40 °C to +125 °C
- Wide supply voltage range from 2.0 V to 6.0 V
- Input levels:
 - For 74HC1G86-Q100: CMOS level
 - For 74HCT1G86-Q100: TTL level
- CMOS low power dissipation
- High noise immunity
- Symmetrical output impedance
- Balanced propagation delays
- Latch-up performance exceeds 100 mA per JESD 78 Class II Level B
- Complies with JEDEC standards:
 - JESD8C (2.7 V to 3.6 V)
 - JESD7A (2.0 V to 6.0 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V

3. Ordering information

Table 1. Ordering information

Type number	Package				Version
	Temperature range	Name	Description		
74HC1G86GW-Q100 74HCT1G86GW-Q100	-40 °C to +125 °C	TSSOP5	plastic thin shrink small outline package; 5 leads; body width 1.25 mm		SOT353-1
74HC1G86GV-Q100 74HCT1G86GV-Q100	-40 °C to +125 °C	SC-74A	plastic surface-mounted package; 5 leads		SOT753
74HC1G86GZ-Q100 74HCT1G86GZ-Q100	-40 °C to +125 °C	XSON5	plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body 1.1 × 0.85 × 0.5 mm		SOT8065-1

4. Marking

Table 2. Marking codes

Type number	Marking[1]
74HC1G86GW-Q100	HH
74HCT1G86GW-Q100	TH
74HC1G86GV-Q100	H86
74HCT1G86GV-Q100	T86
74HC1G86GZ-Q100	HH
74HCT1G86GZ-Q100	TH

[1] The pin 1 indicator is located on the lower left corner of the device, below the marking code.

5. Functional diagram

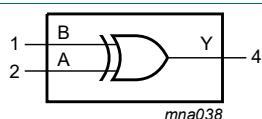


Fig. 1. Logic symbol

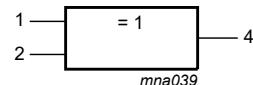


Fig. 2. IEC logic symbol

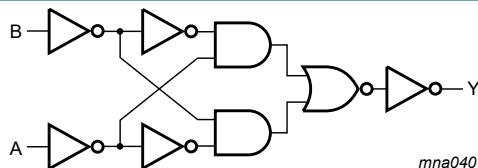
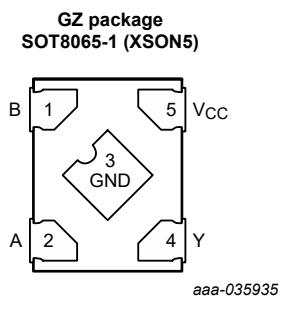
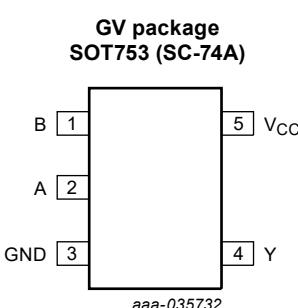
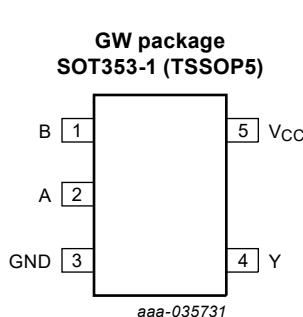


Fig. 3. Logic diagram

6. Pinning information

6.1. Pinning



6.2. Pin description

Table 3. Pin description

Symbol	Pin	Description
B	1	data input
A	2	data input
GND	3	ground (0 V)
Y	4	data output
V _{CC}	5	supply voltage

7. Functional description

Table 4. Function table

H = HIGH voltage level; *L* = LOW voltage level

Inputs		Output
A	B	Y
L	L	L
L	H	H
H	L	H
H	H	L

8. Limiting values

Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7.0	V
I _{IK}	input clamping current	V _I < -0.5 V or V _I > V _{CC} + 0.5 V	-	±20	mA
I _{OK}	output clamping current	V _O < -0.5 V or V _O > V _{CC} + 0.5 V	-	±20	mA
I _O	output current	-0.5 V < V _O < V _{CC} + 0.5 V	[1]	-	±12.5 mA
I _{CC}	supply current			-	25 mA
I _{GND}	ground current		-25	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C	[2]	-	250 mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] For SOT353-1 (TSSOP5) package: P_{tot} derates linearly with 3.3 mW/K above 74 °C.

For SOT753 (SC-74A) package: P_{tot} derates linearly with 3.8 mW/K above 85 °C.

For SOT8065-1 (XSON5) package: P_{tot} derates linearly with 3.2 mW/K above 72 °C.

9. Recommended operating conditions

Table 6. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	74HC1G86-Q100			74HCT1G86-Q100			Unit
			Min	Typ	Max	Min	Typ	Max	
V_{CC}	supply voltage		2.0	5.0	6.0	4.5	5.0	5.5	V
V_I	input voltage		0	-	V_{CC}	0	-	V_{CC}	V
V_O	output voltage		0	-	V_{CC}	0	-	V_{CC}	V
T_{amb}	ambient temperature		-40	+25	+125	-40	+25	+125	°C
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 2.0$ V	-	-	625	-	-	-	ns/V
		$V_{CC} = 4.5$ V	-	-	139	-	-	139	ns/V
		$V_{CC} = 6.0$ V	-	-	83	-	-	-	ns/V

10. Static characteristics

Table 7. Static characteristics

Voltages are referenced to GND (ground = 0 V). All typical values are measured at $T_{amb} = 25$ °C.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G86-Q100								
V_{IH}	HIGH-level input voltage	$V_{CC} = 2.0$ V	1.5	1.2	-	1.5	-	V
		$V_{CC} = 4.5$ V	3.15	2.4	-	3.15	-	V
		$V_{CC} = 6.0$ V	4.2	3.2	-	4.2	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 2.0$ V	-	0.8	0.5	-	0.5	V
		$V_{CC} = 4.5$ V	-	2.1	1.35	-	1.35	V
		$V_{CC} = 6.0$ V	-	2.8	1.8	-	1.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = -20 \mu A; V_{CC} = 2.0$ V	1.9	2.0	-	1.9	-	V
		$I_O = -20 \mu A; V_{CC} = 4.5$ V	4.4	4.5	-	4.4	-	V
		$I_O = -20 \mu A; V_{CC} = 6.0$ V	5.9	6.0	-	5.9	-	V
		$I_O = -2.0 mA; V_{CC} = 4.5$ V	4.13	4.32	-	3.7	-	V
		$I_O = -2.6 mA; V_{CC} = 6.0$ V	5.63	5.81	-	5.2	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 20 \mu A; V_{CC} = 2.0$ V	-	0	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 4.5$ V	-	0	0.1	-	0.1	V
		$I_O = 20 \mu A; V_{CC} = 6.0$ V	-	0	0.1	-	0.1	V
		$I_O = 2.0 mA; V_{CC} = 4.5$ V	-	0.15	0.33	-	0.4	V
		$I_O = 2.6 mA; V_{CC} = 6.0$ V	-	0.16	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 6.0$ V	-	-	1.0	-	1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 A; V_{CC} = 6.0$ V	-	-	10	-	20	μA
C_I	input capacitance		-	1.5	-	-	-	pF

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HCT1G86-Q100								
V_{IH}	HIGH-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	2.0	1.6	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$	-	1.2	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = -20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	4.4	4.5	-	4.4	-	V
		$I_O = -2.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	4.13	4.32	-	3.7	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}$ or V_{IL}						
		$I_O = 20 \mu\text{A}; V_{CC} = 4.5 \text{ V}$	-	0	0.1	-	0.1	V
		$I_O = 2.0 \text{ mA}; V_{CC} = 4.5 \text{ V}$	-	0.15	0.33	-	0.4	V
I_I	input leakage current	$V_I = V_{CC}$ or GND; $V_{CC} = 5.5 \text{ V}$	-	-	1.0	-	1.0	μA
I_{CC}	supply current	$V_I = V_{CC}$ or GND; $I_O = 0 \text{ A}; V_{CC} = 5.5 \text{ V}$	-	-	10	-	20	μA
ΔI_{CC}	additional supply current	per input; $V_{CC} = 4.5 \text{ V to } 5.5 \text{ V}$; $V_I = V_{CC} - 2.1 \text{ V}; I_O = 0 \text{ A}$	-	-	500	-	850	μA
C_I	input capacitance		-	1.5	-	-	-	pF

11. Dynamic characteristics

Table 8. Dynamic characteristics

$GND = 0 \text{ V}; t_r = t_f \leq 6.0 \text{ ns}$; All typical values are measured at $T_{amb} = 25 \text{ }^\circ\text{C}$. For test circuit see Fig. 5

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ	Max	Min	Max	
74HC1G86-Q100								
t_{pd}	propagation delay	A and B to Y; see Fig. 4	[1]					
		$V_{CC} = 2.0 \text{ V}; C_L = 50 \text{ pF}$	-	22	115	-	135	ns
		$V_{CC} = 4.5 \text{ V}; C_L = 50 \text{ pF}$	-	11	23	-	27	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	9	-	-	-	ns
		$V_{CC} = 6.0 \text{ V}; C_L = 50 \text{ pF}$	-	9	20	-	23	ns
C_{PD}	power dissipation capacitance	$V_I = GND$ to V_{CC}	[2]	-	23	-	-	pF
74HCT1G86-Q100								
t_{pd}	propagation delay	A and B to Y; see Fig. 4	[1]					
		$V_{CC} = 4.5 \text{ V}; C_L = 50 \text{ pF}$	-	13	23	-	27	ns
		$V_{CC} = 5.0 \text{ V}; C_L = 15 \text{ pF}$	-	10	-	-	-	ns
C_{PD}	power dissipation capacitance	$V_I = GND$ to $V_{CC} - 1.5 \text{ V}$	[2]	-	23	-	-	pF

[1] t_{pd} is the same as t_{PLH} and t_{PHL} .

[2] C_{PD} is used to determine the dynamic power dissipation P_D (μW).

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz

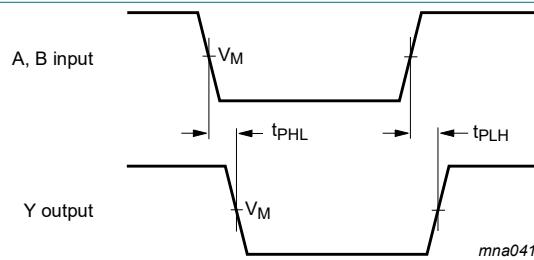
f_o = output frequency in MHz

C_L = output load capacitance in pF

V_{CC} = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

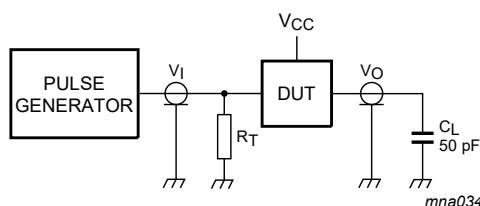
11.1. Waveforms and test circuit



For 74HC1G86-Q100: $V_M = 0.5 \times V_{CC}$; $V_I = \text{GND to } V_{CC}$.

For 74HCT1G86-Q100: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3.0 \text{ V}$.

Fig. 4. The input (A and B) to output (Y) propagation delays



Test data is given in [Table 8](#). Definitions for test circuit:

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 5. Test circuit for measuring switching times

12. Package outline

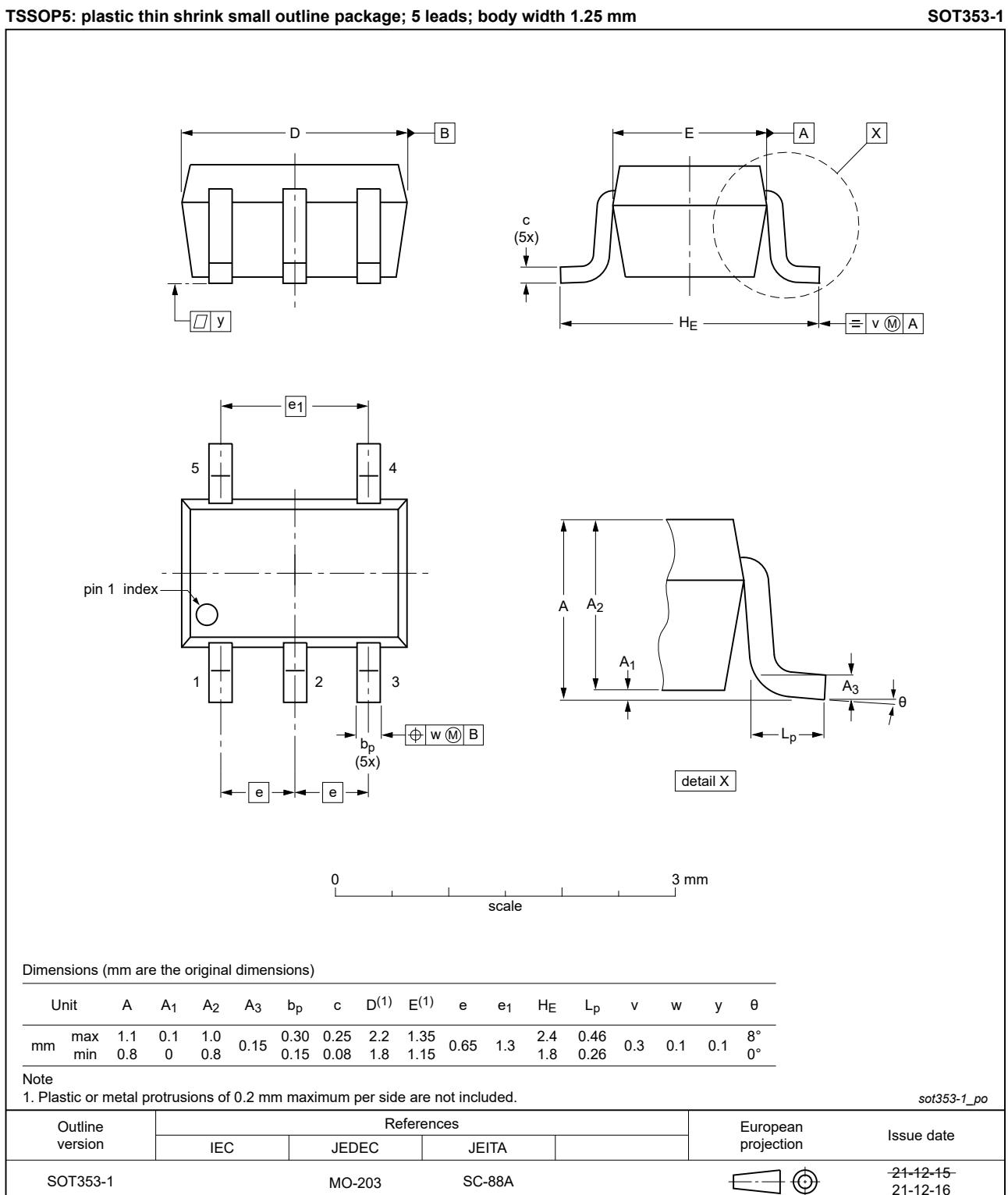


Fig. 6. Package outline SOT353-1 (TSSOP5)

Plastic surface-mounted package; 5 leads

SOT753

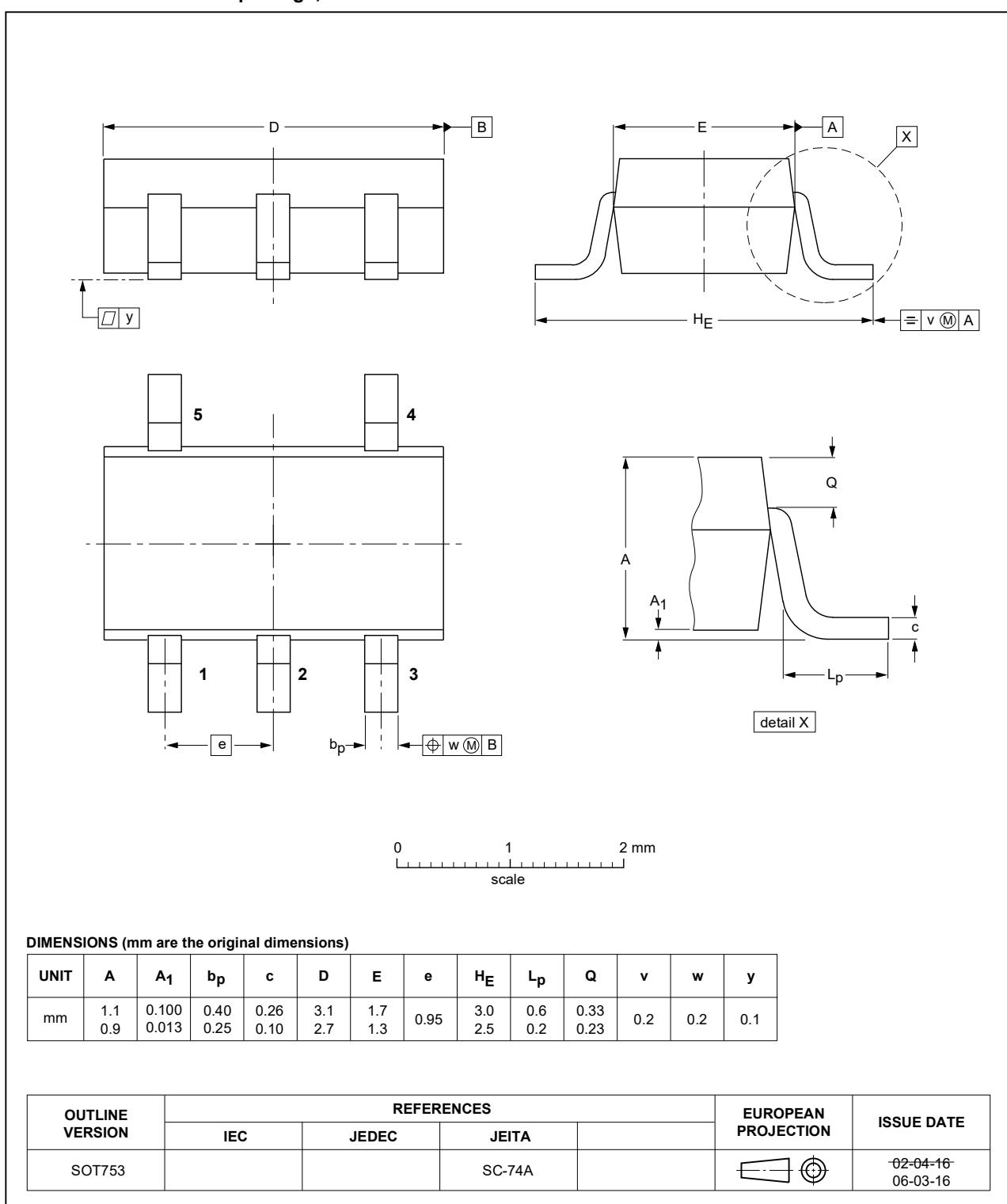


Fig. 7. Package outline SOT753 (SC-74A)

XSON5: Plastic thermal enhanced extremely thin small outline package with side-wettable flanks (SWF); no leads; 5 terminals; body $1.1 \times 0.85 \times 0.5$ mm

SOT8065-1

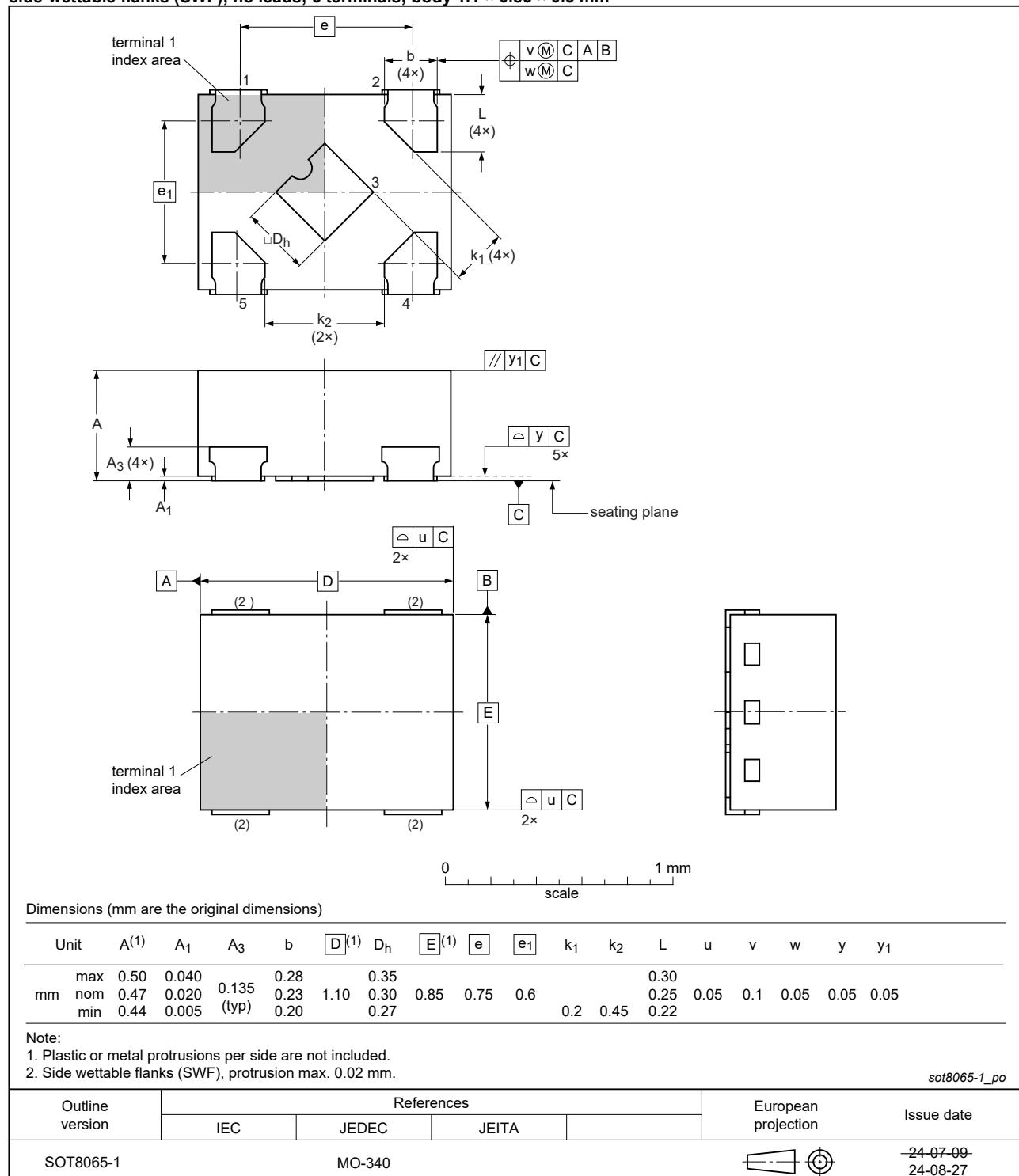


Fig. 8. Package outline SOT8065-1 (XSON5)

13. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

14. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74HC_HCT1G86_Q100 v.5	20250909	Product data sheet	-	74HC_HCT1G86_Q100 v.4
Modifications:	<ul style="list-style-type: none"> Type numbers 74HC1G86GZ-Q100 and 74HCT1G86GZ-Q100 (SOT8065-1/XSON5) added. 			
74HC_HCT1G86_Q100 v.4	20240625	Product data sheet	-	74HC_HCT1G86_Q100 v.3
Modifications:	<ul style="list-style-type: none"> Section 2 : ESD specification updated according to the latest JEDEC standard. 			
74HC_HCT1G86_Q100 v.3	20220127	Product data sheet	-	74HC_HCT1G86_Q100 v.2
Modifications:	<ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. Legal texts have been adapted to the new company name where appropriate. Section 1 and Section 2 updated. Table 5: Derating values for P_{tot} total power dissipation updated. Fig. 6: Package outline drawing for SOT353-1 (TSSOP5) has changed. 			
74HC_HCT1G86_Q100 v.2	20131216	Product data sheet	-	74HC_HCT1G86_Q100 v.1
Modifications:	<ul style="list-style-type: none"> Features and benefits updated (errata). 			
74HC_HCT1G86_Q100 v.1	20130326	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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