# 18-bit universal bus driver with 30Ω termination resistors and 5V tolerant inputs (3-State)

# 74ALVC162835

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Complies with JEDEC standard no. 8-1A.
- CMOS low power consumption
- Direct interface with TTL levels
- Current drive ± 24 mA at 3.0 V
- MULTIBYTE™ flow-through standard pin-out architecture
- Low inductance multiple $V_{CC}$ and GND pins for minimum noise and ground bounce
- Output drive capability 50Ω transmission lines @ 85°C
- Current drive ±24 mA at 3.0 V
- Integrated 30 Ω termination resistors

## DESCRIPTION

The 74ALVC162835 is an 18-bit universal bus driver. Data flow is controlled by output enable (OE), latch enable (LE) and clock inputs (CP).

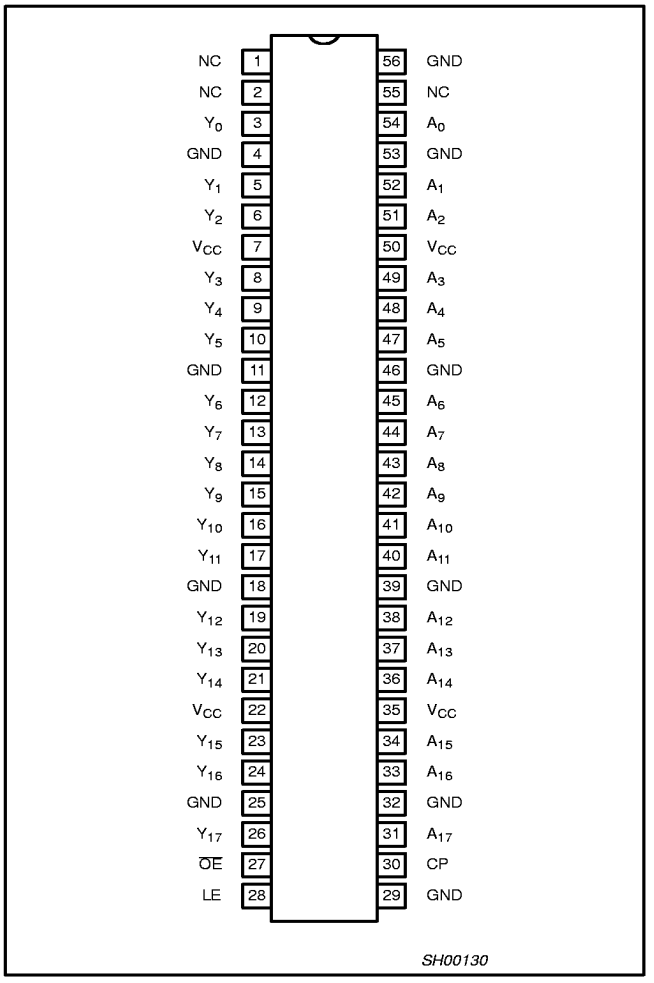
When LE is HIGH, the A to Y data flow is transparent. When LE is LOW and CP is held at LOW or HIGH, the data is latched; on the LOW to HIGH transient of CP the A-data is stored in the latch/flip-flop.

The 74ALVC162835 is designed with 30 Ω_series resistors in both HIGH or LOW output stages.

When $\overline{OE}$ is LOW the outputs are active. When $\overline{OE}$ is HIGH, the outputs go to the high impedance OFF-state. Operation of the $\overline{OE}$ input does not affect the state of the latch/flip -flop.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## PIN CONFIGURATION




## QUICK REFERENCE DATA

GND = 0V; $T_{amb}$ = 25°C; $t_r = t_f \leq 2.5$ns

| SYMBOL | PARAMETER | CONDITIONS | | TYPICAL | UNIT |
|---|---|---|---|---|---|
| $t_{PHL}/t_{PLH}$ | Propagation delay<br>An to Yn;<br>LE to Yn;<br>CP to Yn | $V_{CC}$ = 3.3V, $C_L$ = 50pF | | 2.9<br>3.5<br>3.3 | ns |
| $F_{max}$ | Maximum clock frequency | $V_{CC}$ = 3.3V, $C_L$ = 50pF | | 240 | MHz |
| $C_I$ | Input capacitance | | | 4.0 | pF |
| $C_{I/O}$ | Input/Output capacitance | | | 8.0 | pF |
| $C_{PD}$ | Power dissipation capacitance per buffer | $V_I$ = GND to $V_{CC}$[1] | transparent mode<br>Output enabled<br>Output disabled | 10<br>3 | pF |
| | | | Clocked mode<br>Output enabled<br>Output disabled | 21<br>15 | |

**NOTES:**

1. $C_{PD}$ is used to determine the dynamic power dissipation ($P_D$ in µW):
   $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$ where: $f_i$ = input frequency in MHz; $C_L$ = output load capacitance in pF; $f_o$ = output frequency in MHz; $V_{CC}$ = supply voltage in V; $\Sigma (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

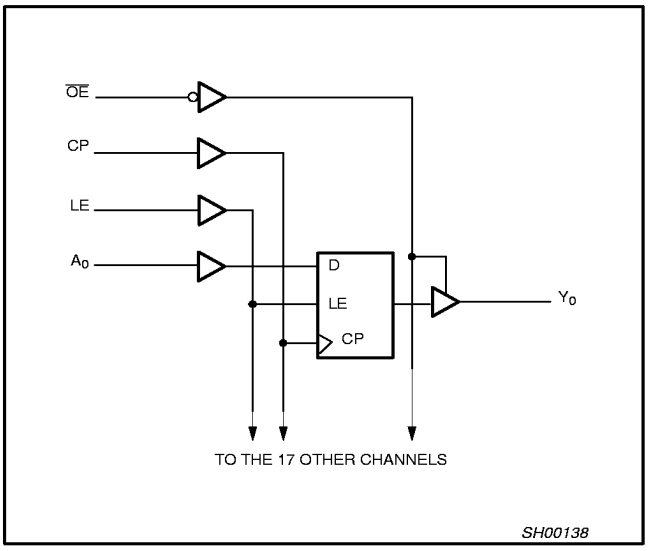
## ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | DRAWING NUMBER |
|---|---|---|---|---|
| 56-Pin Plastic Thin Shrink Small Outline (TSSOP) Type II | –40°C to +85°C | 74ALVC162835 DGG | AC162835 DGG | SOT364-1 |

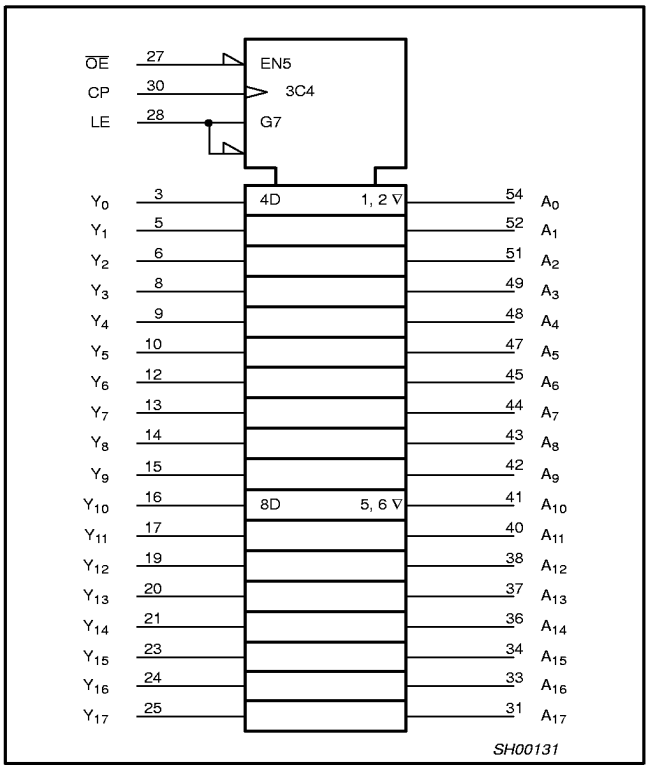
## PIN DESCRIPTION

| PIN NUMBER | SYMBOL | NAME AND FUNCTION |
|---|---|---|
| 1, 2, 55 | NC | No connection |
| 3, 5, 6, 8, 9, 10, 12, 13, 14, 15, 16, 17, 19, 20, 21, 23, 24, 26 | $Y_0$ to $Y_{17}$ | Data outputs |
| 4, 11, 18, 25, 32, 39, 46, 53, 56 | GND | Ground (0V) |
| 7, 22, 35, 50 | $V_{CC}$ | Positive supply voltage |
| 27 | $\overline{OE}$ | Output enable input (active LOW) |
| 28 | LE | Latch enable input (active HIGH) |
| 30 | CP | Clock input |
| 54, 52, 51, 49, 48, 47, 45, 44, 43, 42, 41, 40, 38, 37, 36, 34, 33, 31 | $A_0$ to $A_{17}$ | Data inputs |

## LOGIC SYMBOL




## LOGIC SYMBOL (IEEE/IEC)




## FUNCTION TABLE

| INPUTS | | | | OUTPUTS |
|---|---|---|---|---|
| $\overline{OE}$ | LE | CP | A | Y |
| H | X | X | X | Z |
| L | H | X | L | L |
| L | H | X | H | H |
| L | L | ↑ | L | L |
| L | L | ↑ | H | H |
| L | L | H | X | $Y_0$[1] |
| L | L | L | X | $Y_0$[2] |

H = HIGH voltage level
L = LOW voltage level
X = Don't care
Z = High impedance "off" state
↑ = LOW-to-HIGH level transition

**NOTES:**
1. Output level before the indicated steady-state input conditions were established, provided that CP is high before LE goes low.
2. Output level before the indicated steady-state input conditions were established.

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage 2.5V range (for max. speed performance @ 30 pF output load) | | 2.3 | 2.7 | V |
| | DC supply voltage 3.3V range (for max. speed performance @ 50 pF output load) | | 3.0 | 3.6 | |
| | DC supply voltage (for low-voltage applications) | | 1.2 | 3.6 | |
| $V_I$ | DC Input voltage range | | 0 | $V_{CC}$ | V |
| $V_O$ | DC output voltage range | | 0 | $V_{CC}$ | V |
| $T_{amb}$ | Operating free-air temperature range | | –40 | +85 | °C |
| $t_r$, $t_f$ | Input rise and fall times | $V_{CC}$ = 2.3 to 3.0V<br>$V_{CC}$ = 3.0 to 3.6V | 0<br>0 | 20<br>10 | ns/V |

## ABSOLUTE MAXIMUM RATINGS

In accordance with the Absolute Maximum Rating System (IEC 134)
Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|---|---|---|---|---|
| $V_{CC}$ | DC supply voltage | | –0.5 to +4.6 | V |
| $I_{IK}$ | DC input diode current | $V_I < 0$ | –50 | mA |
| $V_I$ | DC input voltage | Note 1 | –0.5 to +4.6 | V |
| $I_{OK}$ | DC output diode current | $V_O > V_{CC}$ or $V_O < 0$ | ±50 | mA |
| $V_O$ | DC output voltage | Note 1 | –0.5 to $V_{CC}$ +0.5 | V |
| $I_O$ | DC output source or sink current | $V_O$ = 0 to $V_{CC}$ | ±50 | mA |
| $I_{GND}$, $I_{CC}$ | DC $V_{CC}$ or GND current | | ±100 | mA |
| $T_{stg}$ | Storage temperature range | | –65 to +150 | °C |
| $P_{TOT}$ | Power dissipation per package<br>–plastic medium-shrink (SSOP)<br>–plastic thin-medium-shrink (TSSOP) | For temperature range: –40 to +125 °C<br>above +55°C derate linearly with 11.3 mW/K<br>above +55°C derate linearly with 8 mW/K | <br>850<br>600 | mW |

**NOTE:**
1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltage are referenced to GND (ground = 0 V).

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP[1] | MAX | |
| $V_{IH}$ | HIGH level Input voltage | $V_{CC}$ = 2.3 to 2.7V | 1.7 | 1.2 | | V |
| | | $V_{CC}$ = 2.7 to 3.6V | 2.0 | 1.5 | | |
| $V_{IL}$ | LOW level Input voltage | $V_{CC}$ = 2.3 to 2.7V | | 1.2 | 0.7 | V |
| | | $V_{CC}$ = 2.7 to 3.6V | | 1.5 | 0.8 | |
| $V_{OH}$ | HIGH level output voltage | $V_{CC}$ = 2.3 to 3.6V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –100µA | $V_{CC}$ – 0.2 | $V_{CC}$ | | V |
| | | $V_{CC}$ = 2.3V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –4mA | $V_{CC}$ – 0.4 | $V_{CC}$ – 0.11 | | |
| | | $V_{CC}$ = 2.3V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –6mA | $V_{CC}$ – 0.6 | $V_{CC}$ – 0.17 | | |
| | | $V_{CC}$ = 2.7V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –4mA | $V_{CC}$ – 0.5 | $V_{CC}$ – 0.09 | | |
| | | $V_{CC}$ = 2.7V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –8mA | $V_{CC}$ – 0.7 | $V_{CC}$ – 0.19 | | |
| | | $V_{CC}$ = 3.0V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –6mA | $V_{CC}$ – 0.6 | $V_{CC}$ – 0.13 | | |
| | | $V_{CC}$ = 3.0V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = –12mA | $V_{CC}$ – 1.0 | $V_{CC}$ – 0.27 | | |
| $V_{OL}$ | LOW level output voltage | $V_{CC}$ = 2.3 to 3.6V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 100µA | | GND | 0.20 | V |
| | | $V_{CC}$ = 2.3V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 4mA | | 0.07 | 0.40 | |
| | | $V_{CC}$ = 2.3V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 6mA | | 0.11 | 0.55 | |
| | | $V_{CC}$ = 2.7V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 4mA | | 0.06 | 0.40 | |
| | | $V_{CC}$ = 2.7V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 8mA | | 0.13 | 0.60 | |
| | | $V_{CC}$ = 3.0V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 6mA | | 0.09 | 0.55 | |
| | | $V_{CC}$ = 3.0V; $V_I$ = $V_{IH}$ or $V_{IL}$; $I_O$ = 12mA | | 0.19 | 0.80 | |
| $I_I$ | Input leakage current | $V_{CC}$ = 2.3 to 3.6V; $V_I$ = $V_{CC}$ or GND | | 0.1 | 5 | µA |
| $I_{OZ}$ | 3-State output OFF-state current | $V_{CC}$ = 2.3 to 3.6V; $V_I$ = $V_{IH}$ or $V_{IL}$; $V_O$ = $V_{CC}$ or GND | | 0.1 | 10 | µA |
| $I_{CC}$ | Quiescent supply current | $V_{CC}$ = 2.3 to 3.6V; $V_I$ = $V_{CC}$ or GND; $I_O$ = 0 | | 0.2 | 40 | µA |
| $\Delta I_{CC}$ | Additional quiescent supply current | $V_{CC}$ = 2.3V to 3.6V; $V_I$ = $V_{CC}$ – 0.6V; $I_O$ = 0 | | 150 | 750 | µA |

**NOTES:**

1. All typical values are at $T_{amb}$ = 25°C.

## AC CHARACTERISTICS FOR $V_{CC}$ = 2.3V TO 2.7V RANGE

GND = 0V; $t_r = t_f \leq 2.0$ns; $C_L$ = 30pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 2.3 to 2.7V | | | |
| | | | MIN | TYP[1] | MAX | |
| $t_{PHL}/t_{PLH}$ | Propagation delay An to Yn | 1, 7 | 1.0 | 3.5 | 5.0 | ns |
| | Propagation delay LE to Yn | 2, 7 | 1.3 | 4.1 | 5.9 | |
| | Propagation delay CP to Yn | 4, 7 | 1.4 | 4.0 | 6.3 | |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time $\overline{OE}$ to Yn | 6, 7 | 1.4 | 3.8 | 6.3 | ns |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disable time $\overline{OE}$ to Yn | 6, 7 | 1.0 | 2.6 | 4.7 | ns |
| $t_W$ | CP pulse width HIGH or LOW | 4, 7 | 3.3 | 1.0 | – | ns |
| | LE pulse width HIGH | 2, 7 | 3.3 | 0.7 | – | |
| $t_{SU}$ | Set-up time An to CP | 5, 7 | 2.2 | 0.2 | – | ns |
| | Set-up time An to LE | 5, 7 | 0.6 | –0.1 | – | |
| $t_h$ | Hold time An to CP | 3, 7 | 1.3 | 0.2 | – | ns |
| | Hold time An to LE | 3, 7 | 1.4 | 0.4 | – | |
| $F_{max}$ | Maximum clock pulse frequency | 4, 7 | 150 | 190 | – | MHz |

**NOTE:**
1. All typical values are at $V_{CC}$ = 2.5V and $T_{amb}$ = 25°C.

## AC CHARACTERISTICS FOR $V_{CC}$ = 3.0V TO 3.6V RANGE AND $V_{CC}$ = 2.7V

GND = 0V; $t_r = t_f \leq 2.5$ns; $C_L$ = 50pF

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC} = 3.3 \pm 0.3$V | | | $V_{CC}$ = 2.7V | | | |
| | | | MIN | TYP[1, 2] | MAX | MIN | TYP[1] | MAX | |
| $t_{PHL}/t_{PLH}$ | Propagation delay An to Yn | 1, 7 | 1.0 | 2.9 | 4.2 | 1.0 | 3.3 | 5.0 | ns |
| | Propagation delay LE to Yn | 2, 7 | 1.3 | 3.4 | 5.1 | 1.3 | 3.8 | 5.8 | |
| | Propagation delay CP to Yn | 4, 7 | 1.4 | 3.3 | 5.9 | 1.4 | 3.7 | 6.1 | |
| $t_{PZH}/t_{PZL}$ | 3-State output enable time $\overline{OE}$ to Yn | 6, 7 | 1.1 | 3.4 | 5.5 | 1.1 | 4.0 | 6.5 | ns |
| $t_{PHZ}/t_{PLZ}$ | 3-State output disable time $\overline{OE}$ to Yn | 6, 7 | 1.3 | 3.0 | 4.5 | 1.3 | 3.2 | 4.9 | ns |
| $t_W$ | CP pulse width HIGH or LOW | 4, 7 | 3.3 | 0.7 | – | 3.3 | 1.2 | – | ns |
| | LE pulse width HIGH | 2, 7 | 3.3 | 0.6 | – | 3.3 | 0.6 | – | |
| $t_{SU}$ | Set-up time An to CP | 5, 7 | 1.4 | 0.1 | – | 1.4 | 0.2 | – | ns |
| | Set-up time An to LE | 5, 7 | 1.5 | 0.2 | – | 1.5 | 0.2 | – | |
| $t_h$ | Hold time An to CP | 3, 7 | 0.6 | 0.3 | – | 0.6 | 0.0 | – | ns |
| | Hold time An to LE | 3, 7 | 1.0 | 0.3 | – | 1.0 | 0.4 | – | |
| $F_{max}$ | Maximum clock pulse frequency | 4, 7 | 150 | 240 | – | 150 | 190 | – | MHz |

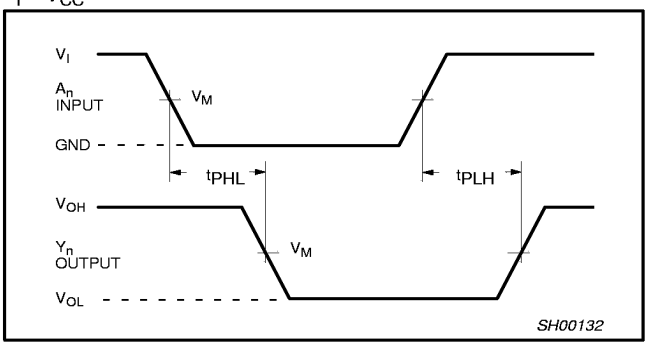
**NOTES:**
1. All typical values are measured $T_{amb}$ = 25°C.
2. Typical value is measured at $V_{CC}$ = 3.3V

## AC WAVEFORMS FOR $V_{CC}$ = 3.0V TO 3.6V AND $V_{CC}$ = 2.7V RANGE

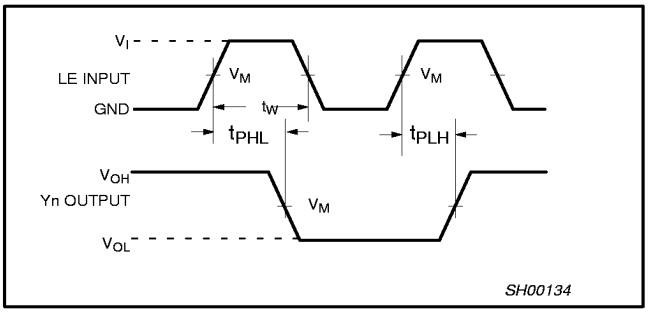
$V_M$ = 1.5 $V_{CC}$
$V_X$ = $V_{OL}$ + 0.3V
$V_Y$ = $V_{OH}$ –0.3V
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.
$V_I$ = 2.7V

## AC WAVEFORMS FOR $V_{CC}$ = 2.3V TO 2.7V AND $V_{CC}$ < 2.3V RANGE

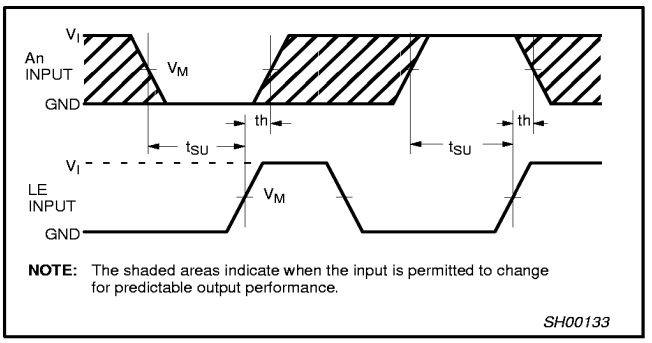
$V_M$ = 0.5 V
$V_X$ = $V_{OL}$ + 0.15V
$V_Y$ = $V_{OH}$ –0.15V
$V_{OL}$ and $V_{OH}$ are the typical output voltage drop that occur with the output load.
$V_I$ = $V_{CC}$



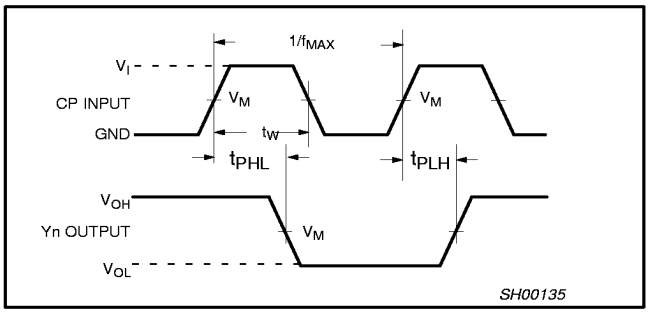

**Waveform 1. Input (Dn) to output (Yn) propagation delay**



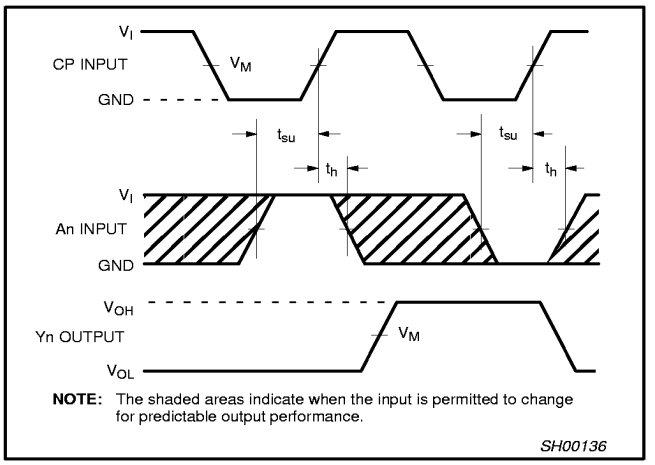

**Waveform 2. Latch enable input (LE) pulse width, the latch enable input to output (Yn) propagation delays.**



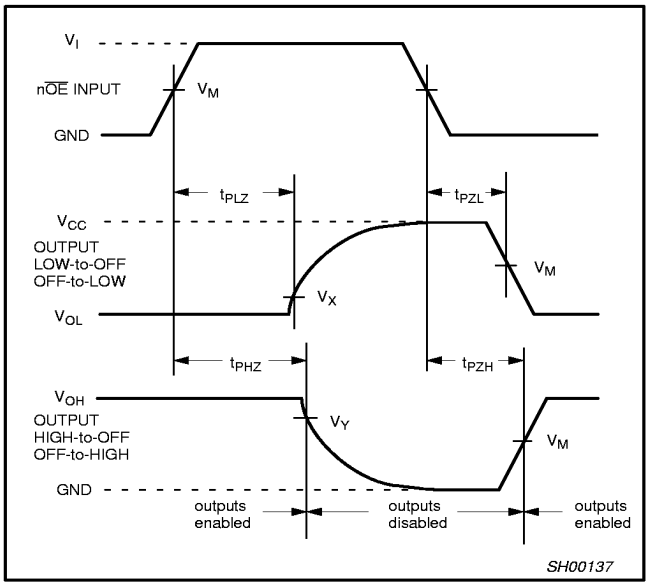

**Waveform 3. Data set-up and hold times for the An input to the LE input**




**Waveform 4. The clock (CP) to Yn propagation delays, the clock pulse width and the maximum clock frequency.**

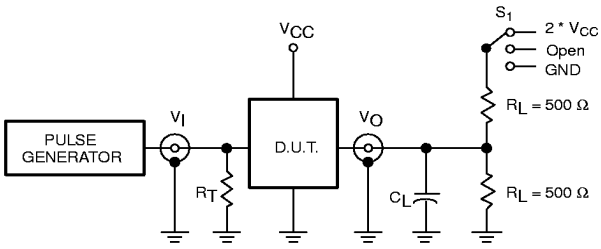



**Waveform 5. Data set-up and hold times for the An input to the clock CP input**




**Waveform 6. 3-State enable and disable times**

## TEST CIRCUIT




**Test Circuit for switching times**

**DEFINITIONS**

$R_L$ = Load resistor

$C_L$ = Load capacitance includes jig and probe capacitance

$R_T$ = Termination resistance should be equal to $Z_{OUT}$ of pulse generators.

**SWITCH POSITION**

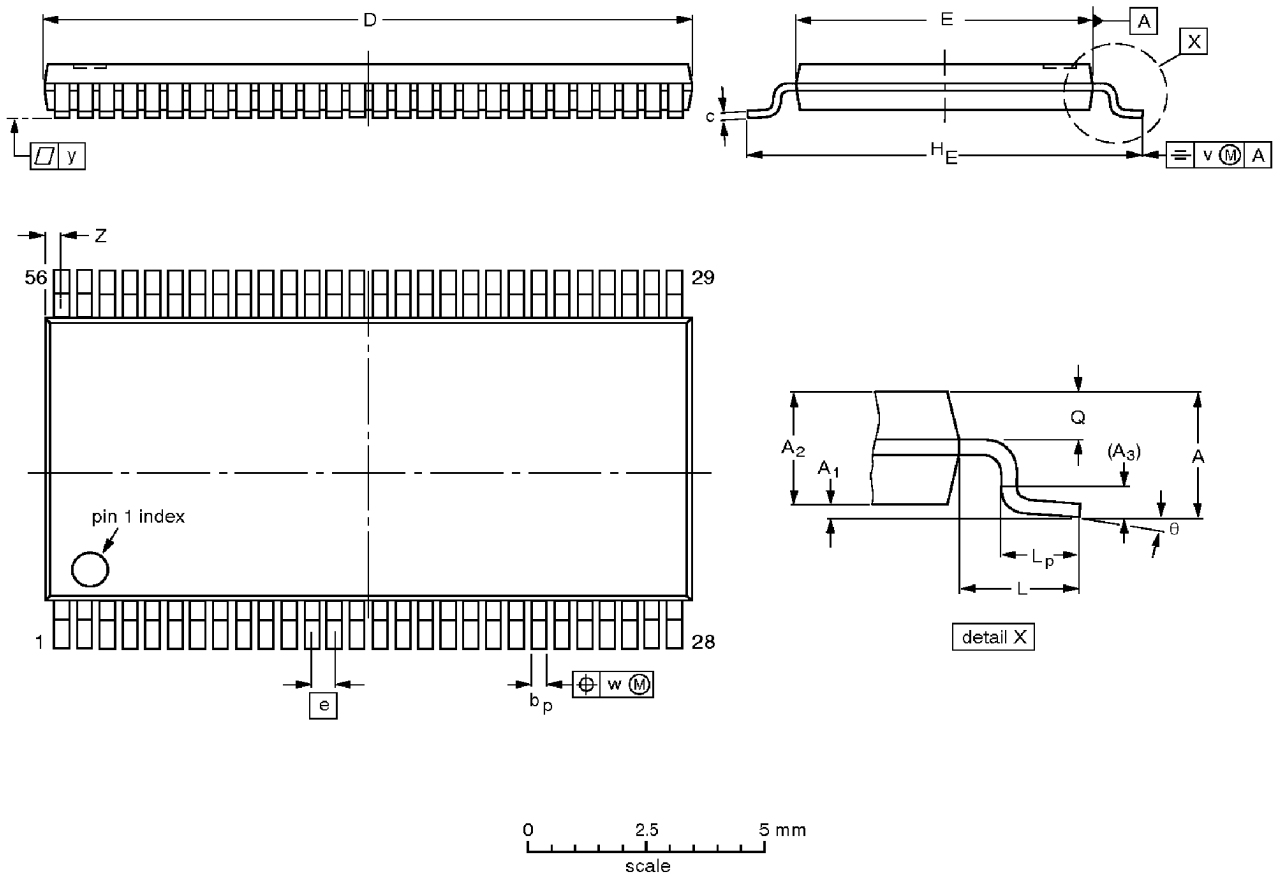
| TEST | $S_1$ |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 * $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

| $V_{CC}$ | $V_I$ |
|---|---|
| < 2.7V | $V_{CC}$ |
| 2.7–3.6V | 2.7V |

*SV00906*

**Waveform 7. Load circuitry for switching times**

**TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm SOT364-1**




**DIMENSIONS (mm are the original dimensions).**

| UNIT | A max. | $A_1$ | $A_2$ | $A_3$ | $b_p$ | c | $D^{(1)}$ | $E^{(2)}$ | e | $H_E$ | L | $L_p$ | Q | v | w | y | Z | θ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.2 | 0.15<br>0.05 | 1.05<br>0.85 | 0.25 | 0.28<br>0.17 | 0.2<br>0.1 | 14.1<br>13.9 | 6.2<br>6.0 | 0.5 | 8.3<br>7.9 | 1.0 | 0.8<br>0.4 | 0.50<br>0.35 | 0.25 | 0.08 | 0.1 | 0.5<br>0.1 | 8°<br>0° |

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|---|
| | IEC | JEDEC | EIAJ | | | | |
| SOT364-1 | | MO-153EE | | | | | ~~93-02-03~~<br>95-02-10 |