

74CBTLVD3384

10-bit level-shifting bus switch with 5-bit output enables

Rev. 4 — 24 June 2024

Product data sheet

1. General description

The 74CBTLVD3384 is a dual 5-pole, single-throw bus switch. The device features two output enable inputs (nOE) that each control five switch channels. The switches are disabled when the associated nOE input is HIGH. CBTLVD is specifically designed for 3.3 V to 1.8 V level shifting applications. Schmitt-trigger action at control inputs makes the circuit tolerant of slower input rise and fall times. This device is fully specified for partial power down applications using I_{OFF}.

2. Features and benefits

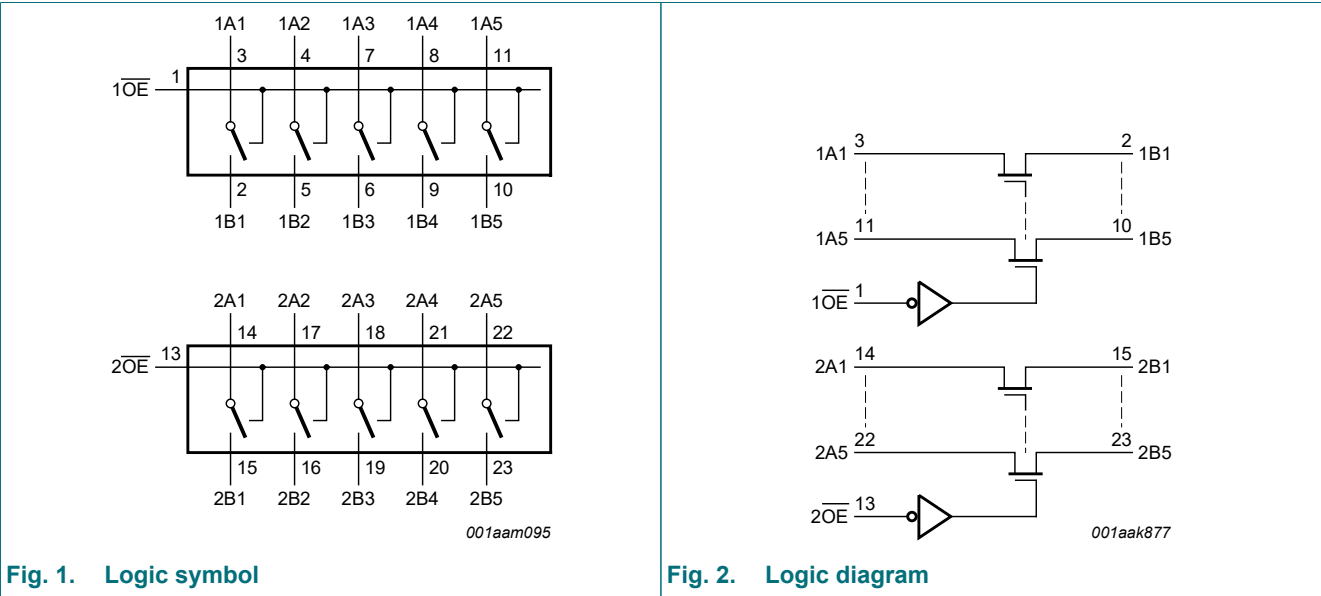
- Supply voltage range from 3.0 V to 3.6 V
- 3.3 V to 1.8 V level shifting
- High noise immunity
- 5 Ω switch connection between two ports
- 600 MHz typical bandwidth
- Overvoltage tolerant control inputs to 3.6 V
- I_{OFF} circuitry provides partial Power-down mode operation
- Rail to rail switching on data I/O ports
- CMOS low power consumption
- Latch-up performance exceeds 250 mA per JESD78B Class I level A
- Complies with JEDEC standard:
 - JESD8-B/JESD36 (3.0 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

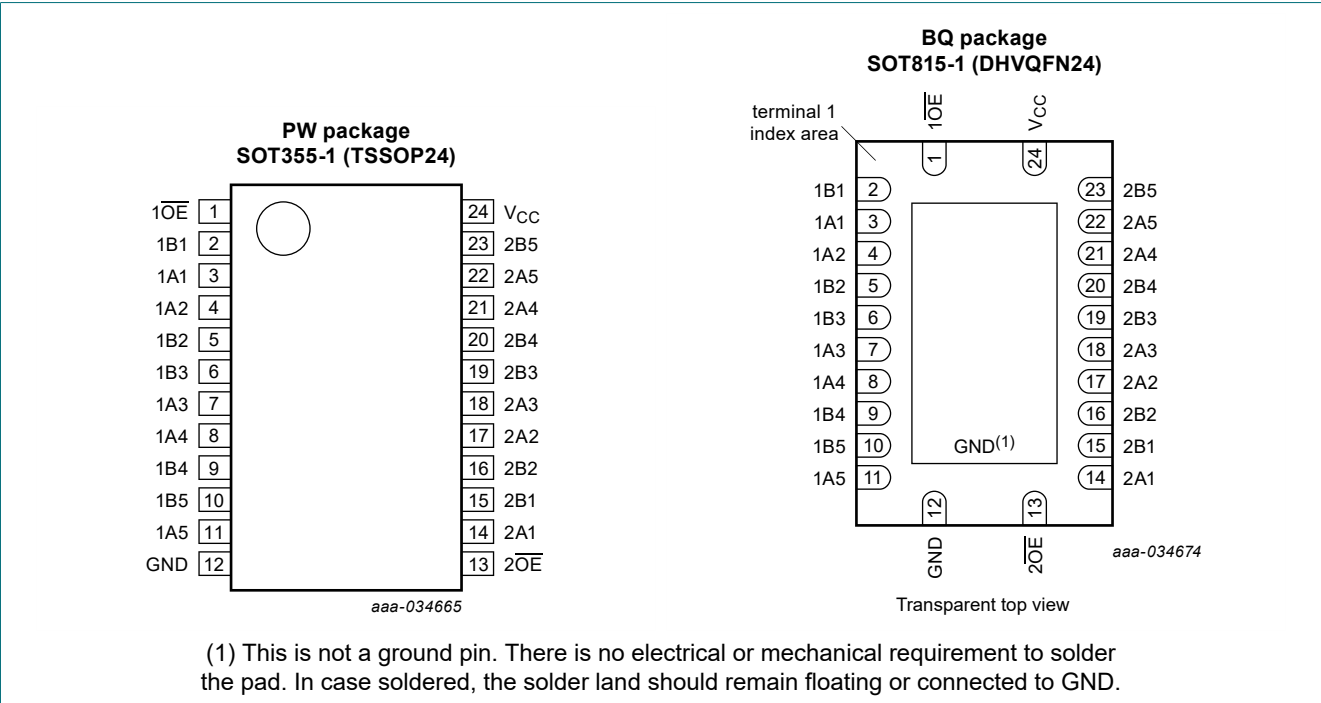
Type number	Package			
	Temperature range	Name	Description	Version
74CBTLVD3384PW	-40 °C to +125 °C	TSSOP24	plastic thin shrink small outline package; 24 leads; body width 4.4 mm	SOT355-1
74CBTLVD3384BQ	-40 °C to +125 °C	DHVQFN24	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 24 terminals; body 3.5 × 5.5 × 0.85 mm	SOT815-1

4. Functional diagram



5. Pinning information

5.1. Pinning



5.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
1OE, 2OE	1, 13	output enable input (active LOW)
1A1, 1A2, 1A3, 1A4, 1A5	3, 4, 7, 8, 11	data input/output (A port)
2A1, 2A2, 2A3, 2A4, 2A5	14, 17, 18, 21, 22	data input/output (A port)
1B1, 1B2, 1B3, 1B4, 1B5	2, 5, 6, 9, 10	data input/output (B port)
2B1, 2B2, 2B3, 2B4, 2B5	15, 16, 19, 20, 23	data input/output (B port)
GND	12	ground (0 V)
V _{CC}	24	positive supply voltage

6. Functional description

Table 3. Function selection

H = HIGH voltage level; L = LOW voltage level; Z = high-impedance OFF-state.

Input		Input/output	
1OE	2OE	1An, 1Bn	2An, 2Bn
L	L	1An = 1Bn	2An = 2Bn
L	H	1An = 1Bn	Z
H	L	Z	2An = 2Bn
H	H	Z	Z

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+4.6	V
V _I	input voltage	[1]	-0.5	+4.6	V
V _{SW}	switch voltage	enable and disable mode [1]	-0.5	V _{CC} + 0.5	V
I _{IK}	input clamping current	V _{I/O} < -0.5 V	-50	-	mA
I _{SK}	switch clamping current	V _I < -0.5 V	-50	-	mA
I _{SW}	switch current	V _{SW} = 0 V to V _{CC}	-	±128	mA
I _{CC}	supply current		-	+100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C [2]	-	500	mW

[1] The minimum input and output voltage ratings may be exceeded if the input and output current ratings are observed.
[2] For SOT355-1 (TSSOP24) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
For SOT815-1 (DHVQFN24) package: P_{tot} derates linearly with 15.0 mW/K above 117 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		3.0	3.6	V
V _I	input voltage		0	3.6	V
V _{SW}	switch voltage	enable and disable mode	0	V _{CC}	V
T _{amb}	ambient temperature		-40	+125	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 3.0 V to 3.6 V [1]	0	200	ns/V

[1] Applies to control signal levels.

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 3.0 V to 3.6 V	2.0	-	-	2.0	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 3.0 V to 3.6 V	-	-	0.9	-	0.9	V
I _I	input leakage current	pin n $\overline{\text{OE}}$; V _I = GND to V _{CC} ; V _{CC} = 3.6 V	-	-	±1	-	±20	μA
V _{pass}	pass voltage	V _I = V _{CC} ; see Fig. 5 to Fig. 9	-	-	-	-	-	V
I _{S(OFF)}	OFF-state leakage current	V _{CC} = 3.6 V; see Fig. 3	-	-	±1	-	±20	μA
I _{S(ON)}	ON-state leakage current	V _{CC} = 3.6 V; see Fig. 4	-	-	±1	-	±20	μA
I _{OFF}	power-off leakage current	V _I or V _O = 0 V to 3.6 V; V _{CC} = 0 V	-	-	±10	-	±50	μA
I _{CC}	supply current	V _I = V _{CC} ; I _O = 0 A; V _{CC} = 3.6 V; V _{SW} = GND or V _{CC}	-	-	20	-	50	μA
		V _I = GND; I _O = 0 A; V _{CC} = 3.6 V; V _{SW} = GND or V _{CC}	-	-	100	-	150	μA
ΔI _{CC}	additional supply current	pin n $\overline{\text{OE}}$; V _I = V _{CC} - 0.6 V; V _{SW} = GND or V _{CC} ; V _{CC} = 3.6 V [2]	-	-	300	-	2000	μA
C _I	input capacitance	pin n $\overline{\text{OE}}$; V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	0.9	-	-	-	pF
C _{S(OFF)}	OFF-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	2.5	-	-	-	pF
C _{S(ON)}	ON-state capacitance	V _{CC} = 3.3 V; V _I = 0 V to 3.3 V	-	9.0	-	-	-	pF

[1] All typical values are measured at T_{amb} = 25 °C.

[2] One input at 3 V, other inputs at V_{CC} or GND.

9.1. Test circuits

001aam032

$V_I = V_{CC}$ or GND and $V_O =$ GND or V_{CC} .

Fig. 3. Test circuit for measuring OFF-state leakage current (one switch)

001aam033

$V_I = V_{CC}$ or GND and $V_O =$ open circuit.

Fig. 4. Test circuit for measuring ON-state leakage current (one switch)

9.2. Typical pass voltage graphs

001aam102

**Fig. 5. Pass voltage versus supply voltage;
 $T_{amb} = 125\text{ °C}$ (typical)**

001aam103

**Fig. 6. Pass voltage versus supply voltage;
 $T_{amb} = 85\text{ °C}$ (typical)**

001aam104

**Fig. 7. Pass voltage versus supply voltage;
 $T_{amb} = 25\text{ °C}$ (typical)**

001aam105

**Fig. 8. Pass voltage versus supply voltage;
 $T_{amb} = 0\text{ °C}$ (typical)**

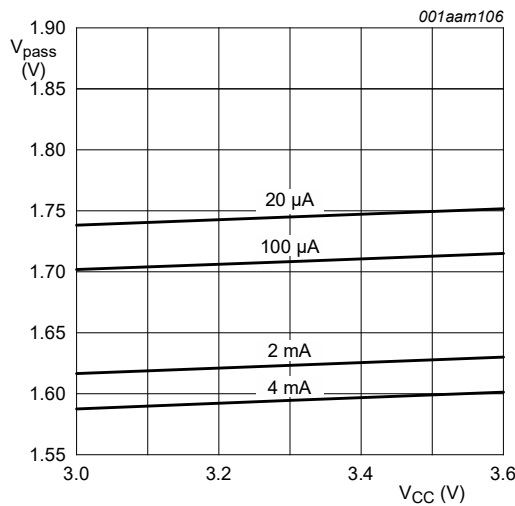


Fig. 9. Pass voltage versus supply voltage; $T_{\text{amb}} = -40\text{ }^{\circ}\text{C}$ (typical)

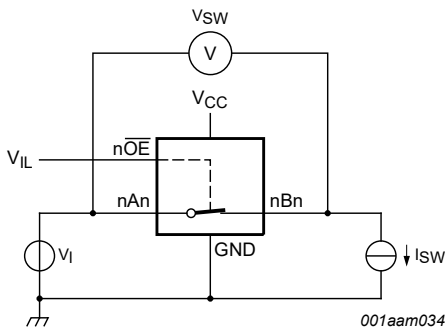
9.3. ON resistance

Table 7. Resistance R_{ON}

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for test circuit see Fig. 10.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
R_{ON}	ON resistance	$V_{\text{CC}} = 3.0\text{ V to }3.6\text{ V}$ [2]						
		$I_{\text{SW}} = 64\text{ mA}; V_{\text{I}} = 0\text{ V}$	-	3.7	7.0	-	10.0	Ω
		$I_{\text{SW}} = 24\text{ mA}; V_{\text{I}} = 0\text{ V}$	-	3.7	7.0	-	10.0	Ω
		$I_{\text{SW}} = 15\text{ mA}; V_{\text{I}} = 1.2\text{ V}$	-	4.7	10.0	-	12.0	Ω

- [1] Typical values are measured at $T_{\text{amb}} = 25\text{ }^{\circ}\text{C}$ and nominal V_{CC} .
- [2] Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.



$R_{\text{ON}} = V_{\text{SW}} / I_{\text{SW}}$.

Fig. 10. Test circuit for measuring ON resistance (one switch)

10. Dynamic characteristics

Table 8. Dynamic characteristics

GND = 0 V; for test circuit see Fig. 13

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ [1]	Max	Min	Max	
t _{pd}	propagation delay	nAn to nBn or nBn to nAn; V _{CC} = 3.0 V to 3.6 V; see Fig. 11 [2] [3]	-	-	0.11	-	0.22	ns
t _{en}	enable time	nOE to nAn or nBn; V _{CC} = 3.0 V to 3.6 V; see Fig. 12 [4]	1.5	2.8	5.0	1.5	6.0	ns
t _{dis}	disable time	nOE to nAn or nBn; V _{CC} = 3.0 V to 3.6 V; see Fig. 12 [5]	0.8	3.2	7.0	0.8	8.0	ns

- [1] All typical values are measured at T_{amb} = 25 °C and at nominal V_{CC}.
- [2] The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the load capacitance, when driven by an ideal voltage source (zero output impedance).
- [3] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [4] t_{en} is the same as t_{PZH} and t_{PZL}.
- [5] t_{dis} is the same as t_{PHZ} and t_{PLZ}.

10.1. Waveforms and test circuit

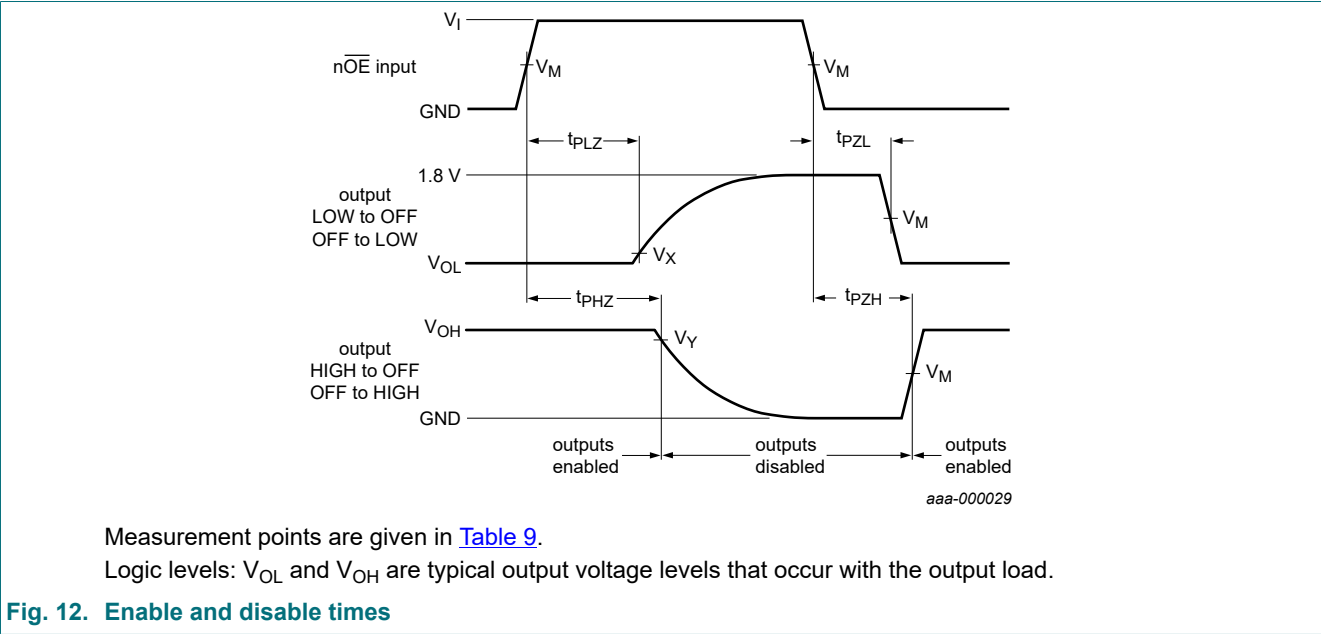
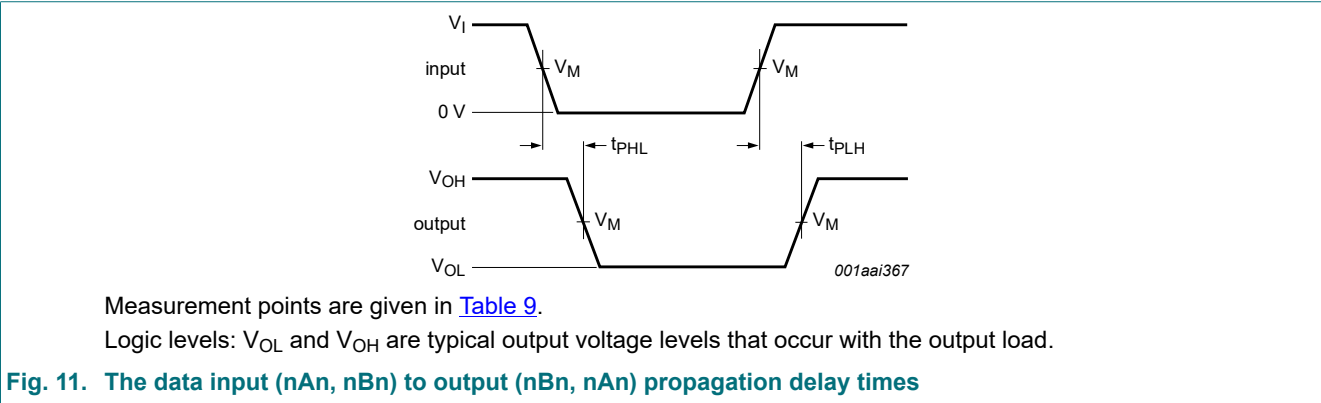
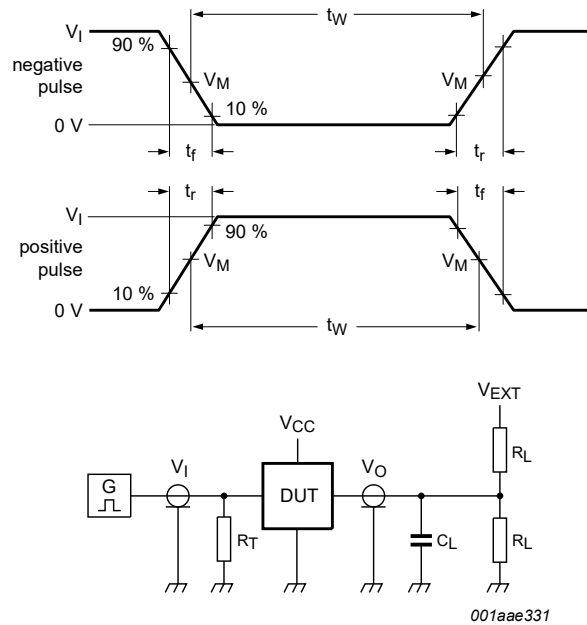


Table 9. Measurement points

Supply voltage	Input			Output		
V _{CC}	V _M	V _I	t _r = t _f	V _M	V _X	V _Y
3.0 V to 3.6 V	0.5 × V _{CC}	V _{CC}	≤ 2.0 ns	0.9 V	V _{OL} + 0.15 V	V _{OH} - 0.15 V



Test data is given in [Table 10](#).
Definitions for test circuit:
R_L = Load resistance;
C_L = Load capacitance including jig and probe capacitance;
R_T = Termination resistance should be equal to the output impedance Z_o of the pulse generator;
V_{EXT} = External voltage for measuring switching times.

Fig. 13. Test circuit for measuring switching times

Table 10. Test data

Supply voltage	Load		V _{EXT}		
V _{CC}	C _L	R _L	t _{PLH} , t _{PHL}	t _{PZH} , t _{PHZ}	t _{PZL} , t _{PLZ}
3.0 V to 3.6 V	30 pF	1 kΩ	open	GND	3.6 V

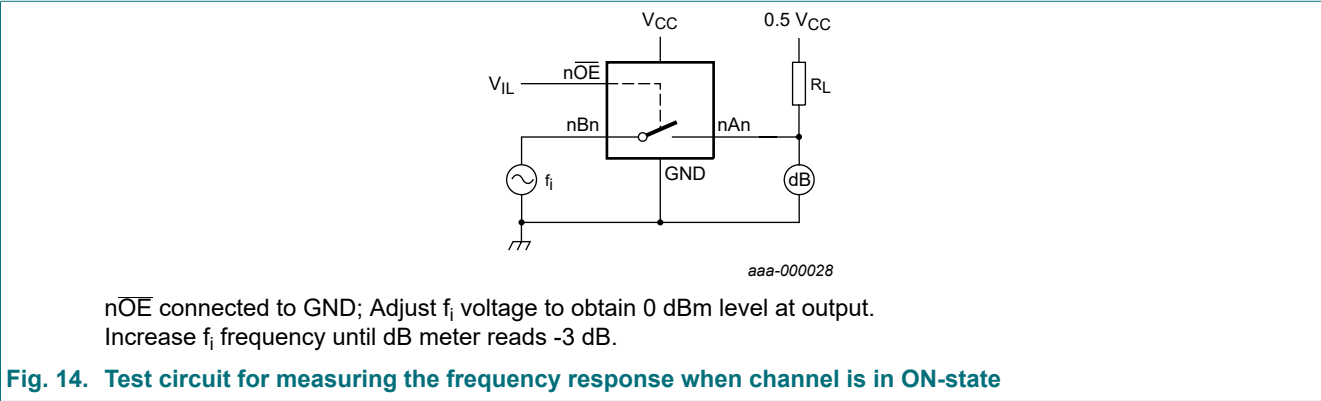
10.2. Additional dynamic characteristics

Table 11. Additional dynamic characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $V_I = \text{GND or } V_{CC}$ (unless otherwise specified); $t_r = t_f \leq 2.5 \text{ ns}$.

Symbol	Parameter	Conditions	T _{amb} = 25 °C			Unit
			Min	Typ [1]	Max	
f _(-3dB)	-3 dB frequency response	V _{CC} = 3.3 V; R _L = 50 Ω; see Fig. 14 [2]	-	575	-	MHz

[1] Typical values are measured at T_{amb} = 25 °C and V_{CC} = 3.3 V.
[2] f_i is biased at 0.5V_{CC}.



11. Package outline

TSSOP24: plastic thin shrink small outline package; 24 leads; body width 4.4 mm

SOT355-1

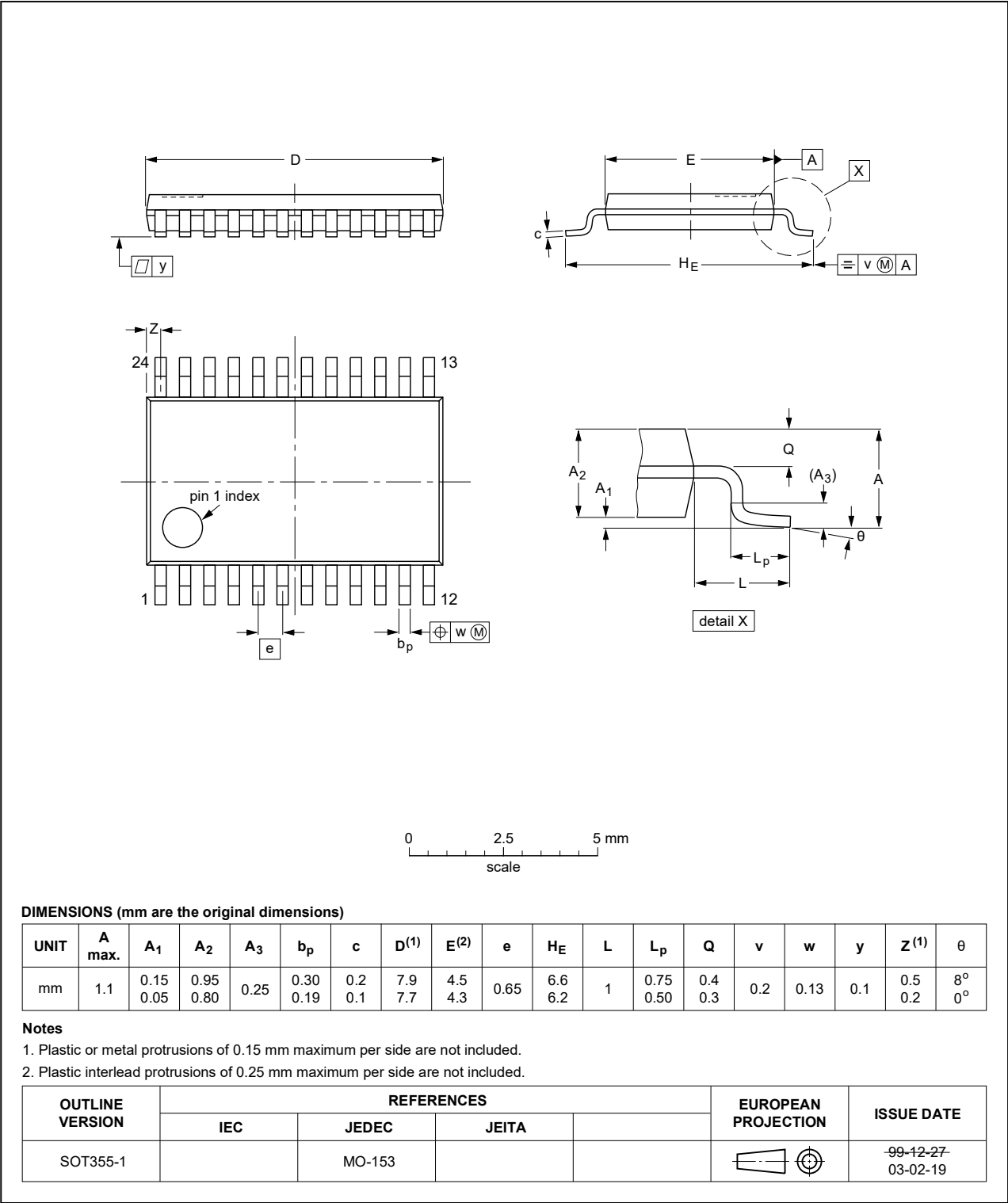


Fig. 15. Package outline SOT355-1 (TSSOP24)

DHVQFN24: plastic dual in-line compatible thermal enhanced very thin quad flat package;
no leads; 24 terminals; body 3.5 x 5.5 x 0.85 mm

SOT815-1

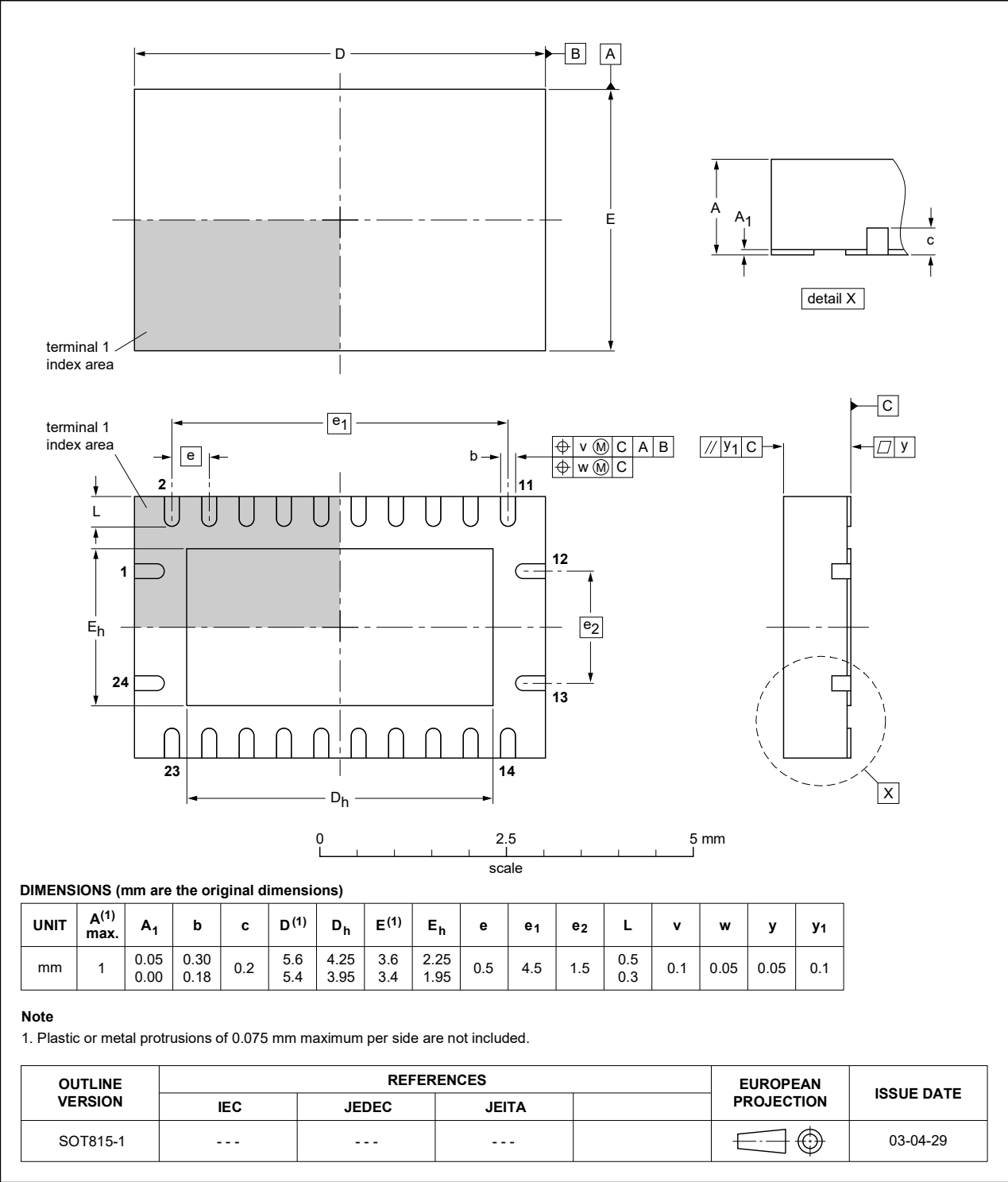


Fig. 16. Package outline SOT815-1 (DHVQFN24)

12. Abbreviations

Table 12. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council

13. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74CBTLVD3384 v.4	20240624	Product data sheet	-	74CBTLVD3384 v.3
Modifications:	Section 2: ESD specification updated according to the latest JEDEC standard.			
74CBTLVD3384 v.3	20190417	Product data sheet	-	74CBTLVD3384 v.2
Modifications:	- The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. - Legal texts have been adapted to the new company name where appropriate. - Type number 74CBTLVD3384DK (SOT556-1) removed.			
74CBTLVD3384 v.2	20111216	Product data sheet	-	74CBTLVD3384 v.1
Modifications:	Legal pages updated.			
74CBTLVD3384 v.1	20110719	Product data sheet	-	-

14. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Date of release: 24 June 2024