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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

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H7N1002LD, H7N1002LS, H7N1002LM

Silicon N Channel MOS FET
High Speed Power Switching

RENESAS

ADE-208-1573E (Z)

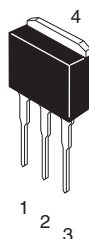
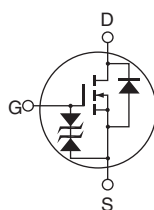
6th. Edition
Aug. 2002

Features

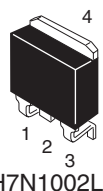
- Low on-resistance
- $R_{DS(on)} = 8\text{ m}\Omega$ typ.
- Low drive current
- Available for 4.5 V gate drive

Outline

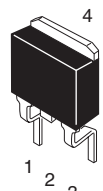
LDPAK



H7N1002LD



H7N1002LS



H7N1002LM

1. Gate
2. Drain
3. Source
4. Drain

Absolute Maximum Ratings

(Ta = 25°C)

Item	Symbol	Ratings	Unit
Drain to source voltage	V_{DSS}	100	V
Gate to source voltage	V_{GSS}	±20	V
Drain current	I_D	75	A
Drain peak current	$I_{D(pulse)}$ ^{Note1}	300	A
Body-drain diode reverse drain current	I_{DR}	75	A
Avalanche current	I_{AP} ^{Note3}	50	A
Avalanche energy	E_{AR} ^{Note3}	166	mJ
Channel dissipation	P_{ch} ^{Note2}	100	W
Channel temperature	Tch	150	°C
Storage temperature	Tstg	−55 to +150	°C

Notes: 1. $PW \leq 10 \mu s$, duty cycle $\leq 1 \%$
2. Value at Tc = 25°C
3. Value at Tch = 25°C, Rg $\geq 50 \Omega$

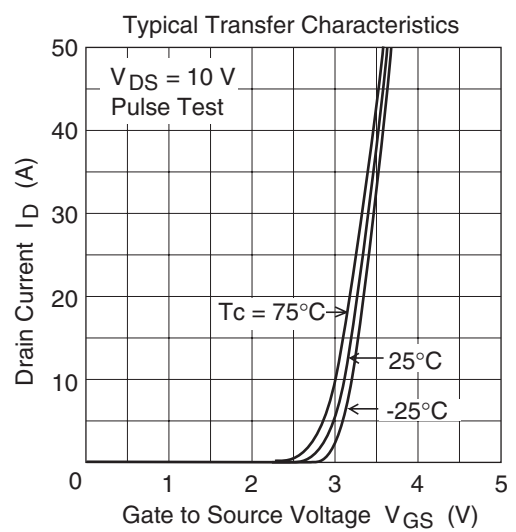
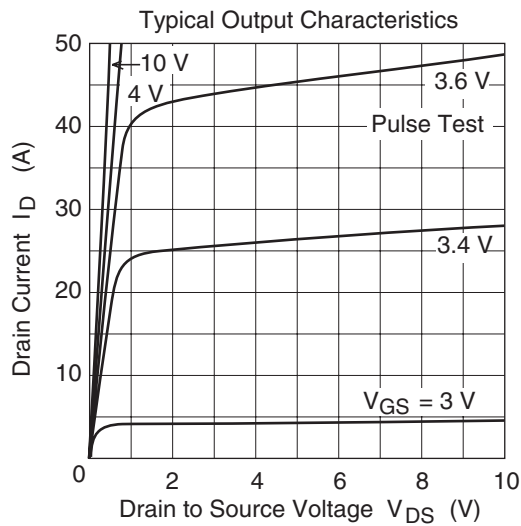
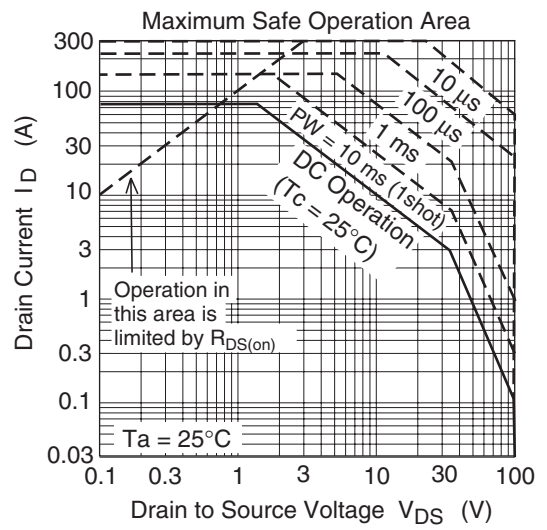
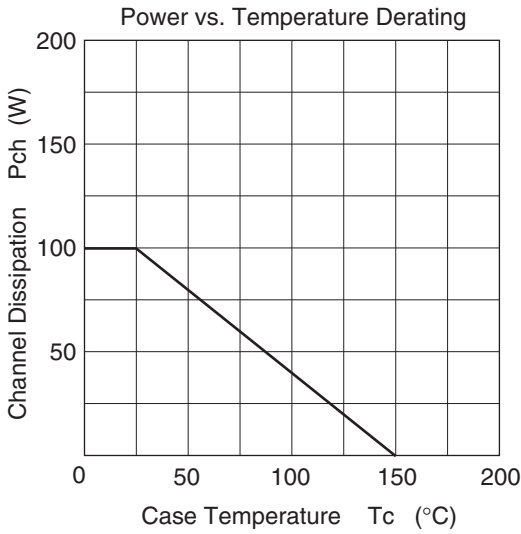
Electrical Characteristics

(Ta = 25°C)

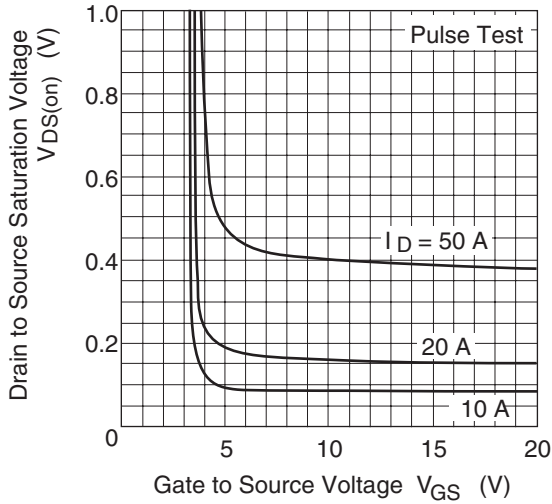
Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Drain to source breakdown voltage	$V_{(BR)DSS}$	100	—	—	V	$I_D = 10 \text{ mA}$, $V_{GS} = 0$
Gate to source breakdown Voltage	$V_{(BR)GSS}$	±20	—	—	V	$I_G = \pm 100 \text{ } \mu\text{A}$, $V_{DS} = 0$
Gate to source leak current	I_{GSS}	—	—	±10	μA	$V_{GS} = \pm 16 \text{ V}$, $V_{DS} = 0$
Zero gate voltage drain current	I_{DSS}	—	—	10	μA	$V_{DS} = 100 \text{ V}$, $V_{GS} = 0$
Gate to source cutoff voltage	$V_{GS(off)}$	1.0	—	2.5	V	$I_D = 1 \text{ mA}$, $V_{DS} = 10 \text{ V}^{*1}$
Static drain to source on state resistance	$R_{DS(on)}$	—	8	10	mΩ	$I_D = 37.5 \text{ A}$, $V_{GS} = 10 \text{ V}^{*1}$
		—	10	15	mΩ	$I_D = 37.5 \text{ A}$, $V_{GS} = 4.5 \text{ V}^{*1}$
Forward transfer admittance	$ y_{fs} $	57	95	—	S	$I_D = 37.5 \text{ A}$, $V_{DS} = 10 \text{ V}^{*1}$
Input capacitance	Ciss	—	9700	—	pF	$V_{DS} = 10 \text{ V}$
Output capacitance	Coss	—	740	—	pF	$V_{GS} = 0$
Reverse transfer capacitance	Crss	—	330	—	pF	$f = 1 \text{ MHz}$
Total gate charge	Qg	—	155	—	nc	$V_{DD} = 50 \text{ V}$
Gate to source charge	Qgs	—	35	—	nc	$V_{GS} = 10 \text{ V}$
Gate to drain charge	Qgd	—	33	—	nc	$I_D = 75 \text{ A}$
Turn-on delay time	$t_{d(on)}$	—	43	—	ns	$V_{GS} = 10 \text{ V}$, $I_D = 37.5 \text{ A}$
Rise time	t_r	—	245	—	ns	$R_L = 0.8 \text{ } \Omega$
Turn-off delay time	$t_{d(off)}$	—	130	—	ns	$R_g = 4.7 \text{ } \Omega$
Fall time	t_f	—	25	—	ns	
Body-drain diode forward voltage	V_{DF}	—	0.93	—	V	$I_F = 75 \text{ A}$, $V_{GS} = 0$
Body-drain diode reverse recovery time	t_{rr}	—	70	—	ns	$I_F = 75 \text{ A}$, $V_{GS} = 0$ $diF/dt = 100 \text{ A}/\mu\text{s}$

Notes: 1. Pulse test

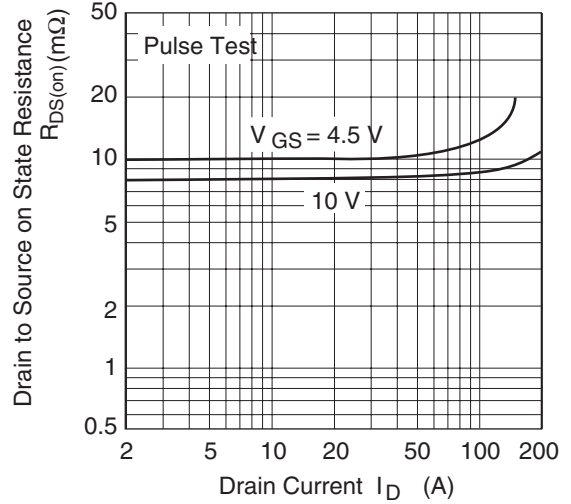
Main Characteristics



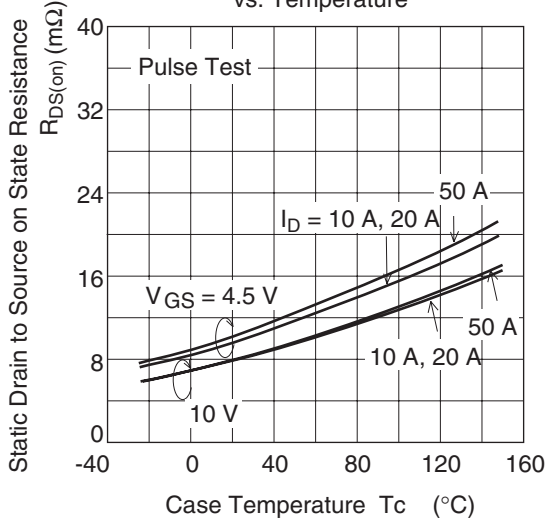
Drain to Source Saturation Voltage VS.
Gate to Source Voltage



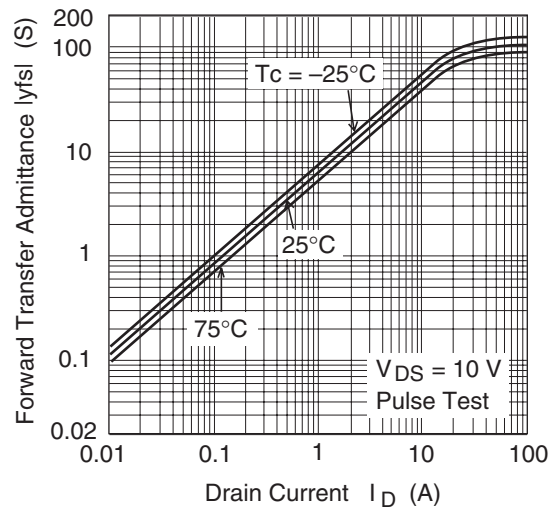
Static Drain to Source on State Resistance
vs. Drain Current

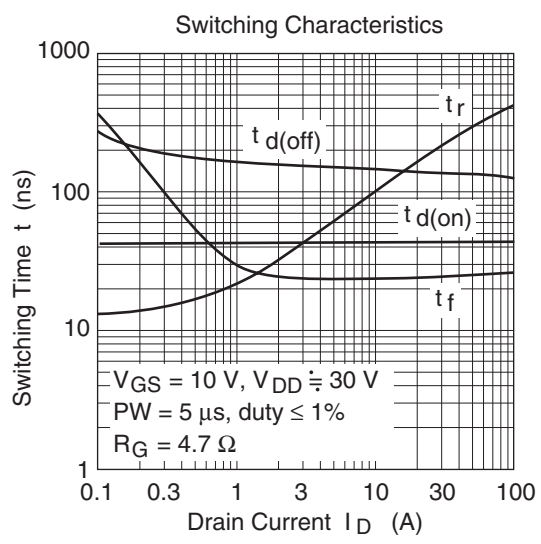
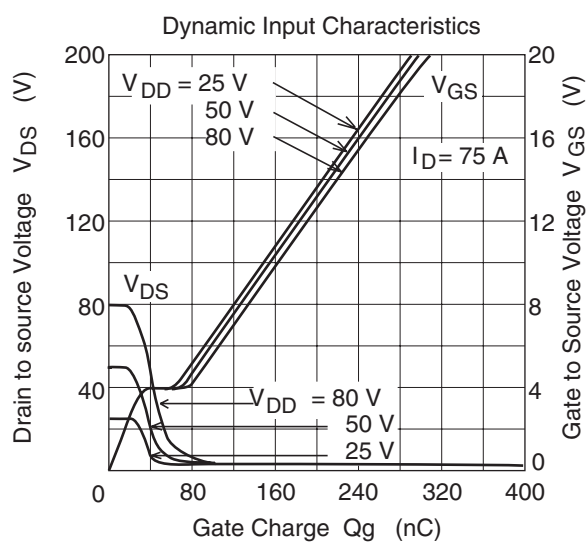
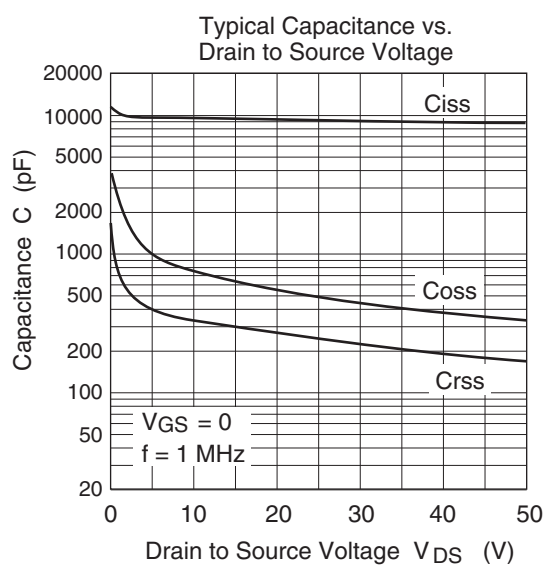
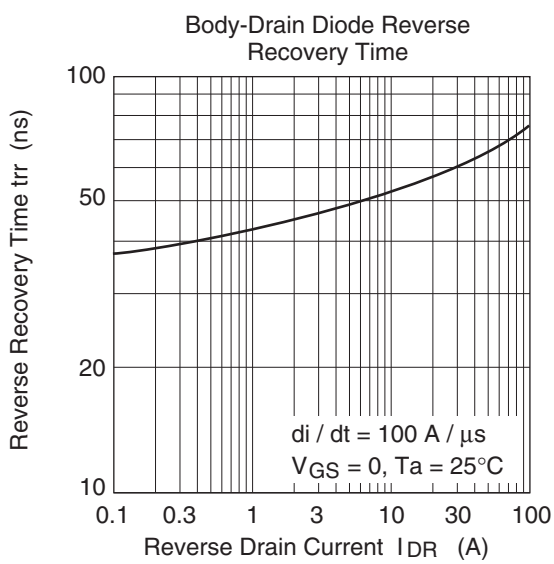


Static Drain to Source on State Resistance
vs. Temperature

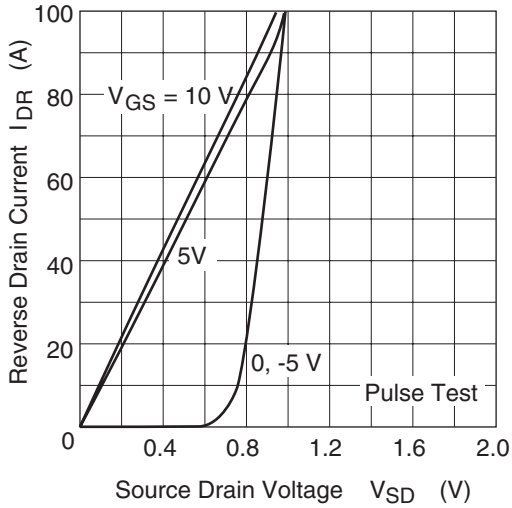


Forward Transfer Admittance vs.
Drain Current

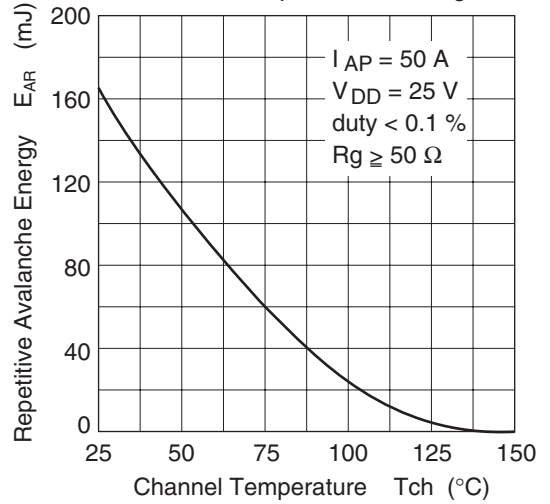




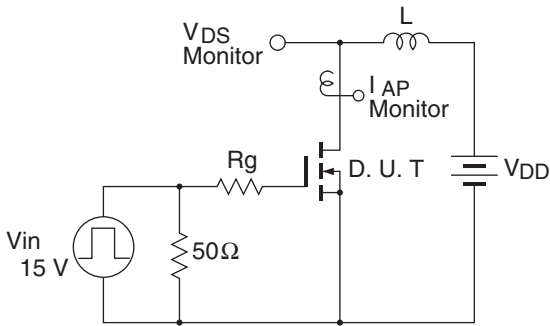
Reverses Drain Current vs.
Source to Drain Voltage



Maximum Avalanche Energy vs.
Channel Temperature Derating

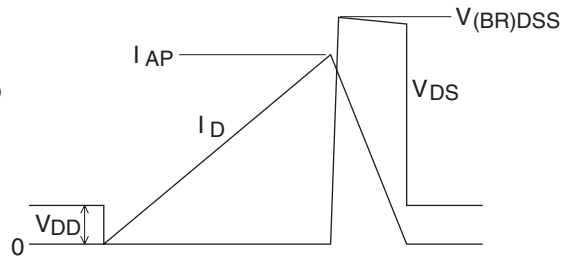


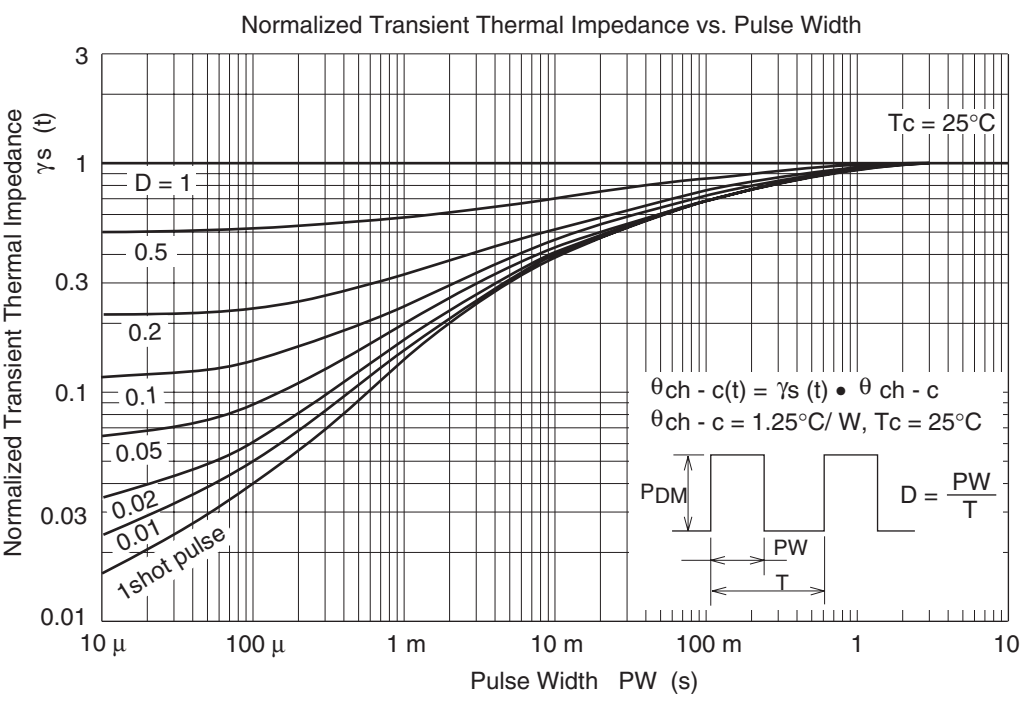
Avalanche Test Circuit



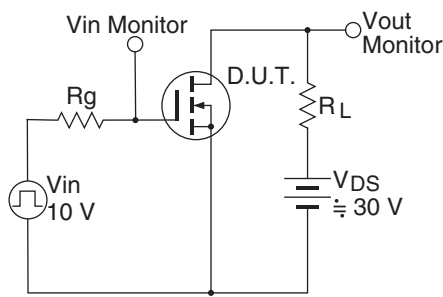
Avalanche Waveform

$$E_{AR} = \frac{1}{2} \cdot L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}$$

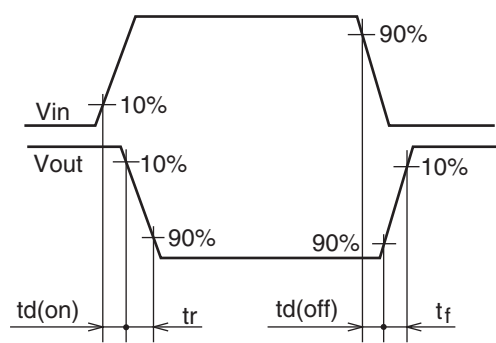




Switching Time Test Circuit



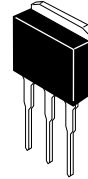
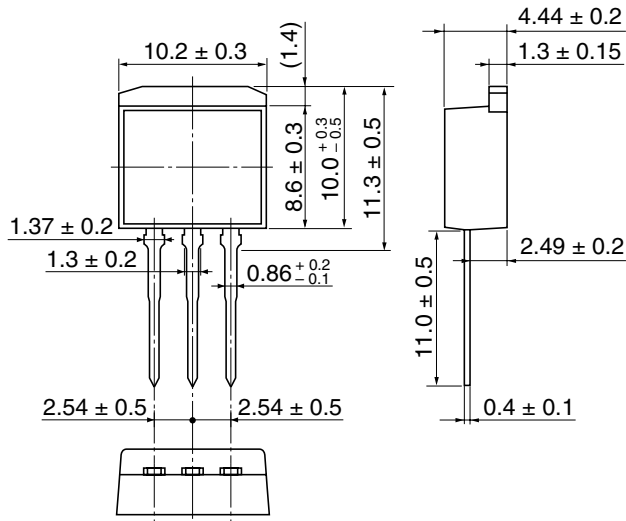
Switching Time Waveform



Package Dimensions

• H7N1002LD

Unit: mm

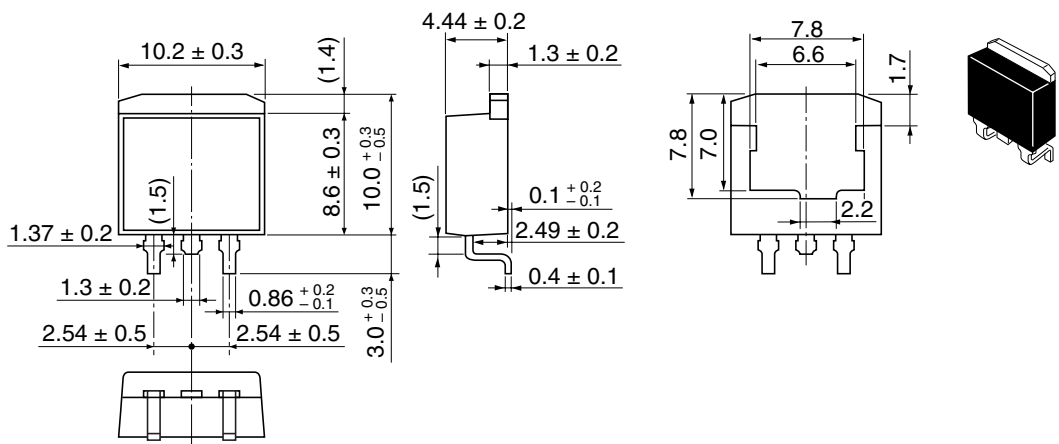


Hitachi Code	LDPAK (L)
JEDEC	—
JEITA	—
Mass (reference value)	1.4 g

H7N1002LD, H7N1002LS, H7N1002LM

• H7N1002LS

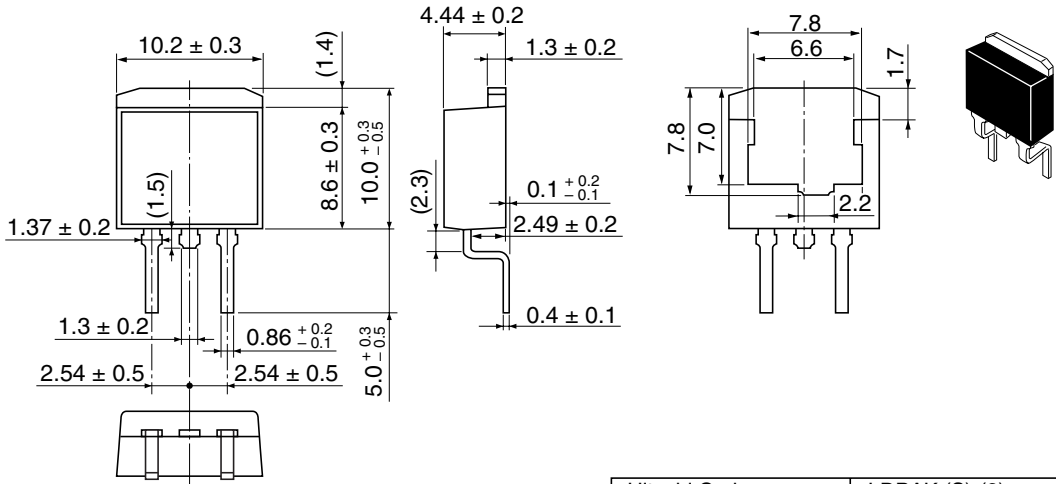
Unit: mm



Hitachi Code	LDPAK (S)-(1)
JEDEC	—
JEITA	—
Mass (reference value)	1.3 g

• H7N1002LM

Unit: mm



Hitachi Code	LDBAK (S)-(2)
JEDEC	—
JEITA	—
Mass (reference value)	1.35 g

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