

200MHz, CMOS OPERATIONAL AMPLIFIER WITH SHUTDOWN

FEATURES

- **UNITY-GAIN BANDWIDTH: 450MHz**
- **WIDE BANDWIDTH: 200MHz GBW**
- **HIGH SLEW RATE: 360V/ μ s**
- **LOW NOISE: 5.8nV/ $\sqrt{\text{Hz}}$**
- **EXCELLENT VIDEO PERFORMANCE:**
DIFF GAIN: 0.02%, DIFF PHASE: 0.05°
0.1dB GAIN FLATNESS: 75MHz
- **INPUT RANGE INCLUDES GROUND**
- **RAIL-TO-RAIL OUTPUT (within 100mV)**
- **LOW INPUT BIAS CURRENT: 3pA**
- **LOW SHUTDOWN CURRENT: 3.4 μ A**
- **ENABLE/DISABLE TIME: 100ns/30ns**
- **THERMAL SHUTDOWN**
- **SINGLE-SUPPLY OPERATING RANGE: 2.5V to 5.5V**
- **MicroSIZE PACKAGES**

APPLICATIONS

- **VIDEO PROCESSING**
- **ULTRASOUND**
- **OPTICAL NETWORKING, TUNABLE LASERS**
- **PHOTODIODE TRANSIMPEDANCE AMPS**
- **ACTIVE FILTERS**
- **HIGH-SPEED INTEGRATORS**
- **ANALOG-TO-DIGITAL (A/D) CONVERTER INPUT BUFFERS**
- **DIGITAL-TO-ANALOG (D/A) CONVERTER OUTPUT AMPLIFIERS**
- **BARCODE SCANNERS**
- **COMMUNICATIONS**

DESCRIPTION

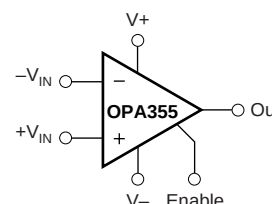
The OPA355 series high-speed, voltage-feedback CMOS operational amplifiers are designed for video and other applications requiring wide bandwidth. The OPA355 is unity-gain stable and can drive large output currents. In addition, the OPA355 has a digital shutdown (Enable) function. This feature provides power savings during idle periods and places the output in a high-impedance state to support output multiplexing. Differential gain is 0.02% and differential phase is 0.05°. Quiescent current is only 8.3mA per channel.

The OPA355 is optimized for operation on single or dual supplies as low as 2.5V ($\pm 1.25\text{V}$) and up to 5.5V ($\pm 2.75\text{V}$). Common-mode input range for the OPA355 extends 100mV below ground and up to 1.5V from V+. The output swing is within 100mV of the rails, supporting wide dynamic range.

The OPA355 series is available in single (SOT23-6 and SO-8), dual (MSOP-10), and triple (TSSOP-14 and SO-14) versions. Multichannel versions feature completely independent circuitry for lowest crosstalk and freedom from interaction. All are specified over the extended -40°C to $+125^{\circ}\text{C}$ range.

OPA355 RELATED PRODUCTS

FEATURES	PRODUCT
200MHz, Rail-to-Rail Output, CMOS, No Shutdown	OPA356
38MHz, Rail-to-Rail Input/Output, CMOS	OPAx350
75MHz, Rail-to-Rail Output	OPAx631
150MHz, Rail-to-Rail Output	OPAx634
Differential Input/Output, 3.3V Supply	THS412x



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ABSOLUTE MAXIMUM RATINGS⁽¹⁾

Supply Voltage, V+ to V-	7.5V
Signal Input Terminals, Voltage ⁽²⁾	(V-) – 0.5V to (V+) + 0.5V
Current ⁽²⁾	10mA
Enable Input	(V-) – 0.5V to (V+) + 0.5V
Output Short-Circuit ⁽³⁾	Continuous
Operating Temperature	–55°C to +150°C
Storage Temperature	–65°C to +150°C
Junction Temperature	+160°C
Lead Temperature (soldering, 10s)	+300°C

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied. (2) Input terminals are diode-clamped to the power-supply rails. Input signals that can swing more than 0.5V beyond the supply rails should be current limited to 10mA or less. (3) Short-circuit to ground, one amplifier per package.

PACKAGE/ORDERING INFORMATION⁽¹⁾

PRODUCT	PACKAGE-LEAD	PACKAGE MARKING
OPA355	SOT23-6	C55
OPA355	SO-8	OPA355UA
OPA2355	MSOP-10	D55
OPA3355	TSSOP-14	OPA3355EA
OPA3355	SO-14	OPA3355UA

NOTE: (1) For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.



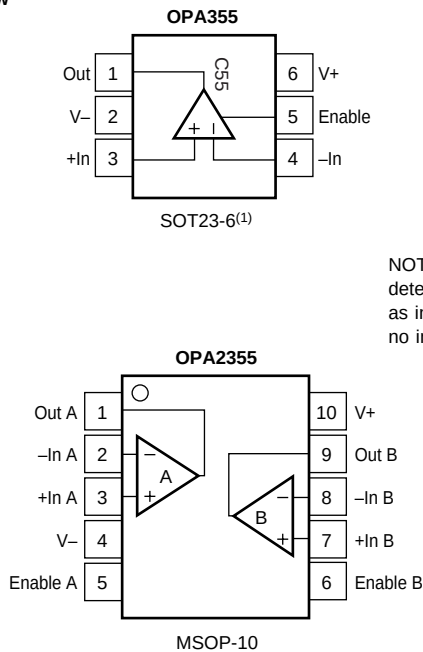
ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

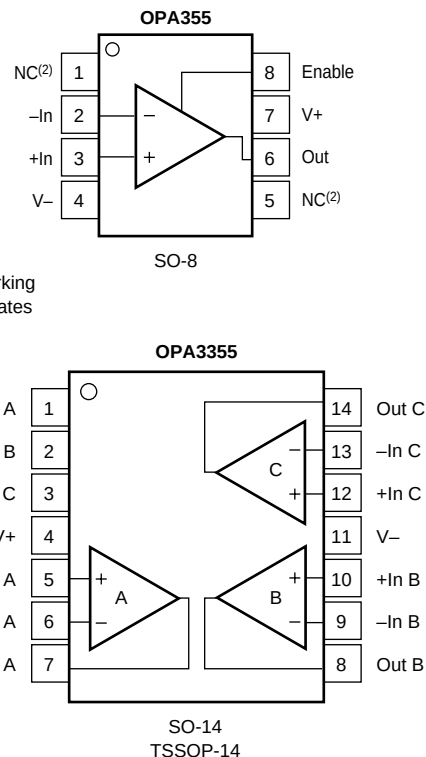
ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PIN CONFIGURATIONS

Top View



NOTES: (1) Pin 1 of the SOT23-6 is determined by orienting the package marking as indicated in the diagram. (2) NC indicates no internal connection.



ELECTRICAL CHARACTERISTICS: $V_S = +2.7V$ to $+5.5V$ Single-Supply

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+125^{\circ}C$.

At $T_A = +25^{\circ}C$, $R_F = 604\Omega$, $R_L = 150\Omega$, and connected to $V_S/2$, unless otherwise noted.

PARAMETER	CONDITION	OPA355 OPA2355 OPA3355			UNITS
		MIN	TYP	MAX	
OFFSET VOLTAGE					
Input Offset Voltage V_{OS}	$V_S = +5V$		± 2	± 9	mV
vs Temperature dV_{OS}/dT	Specified Temperature Range		± 7	± 15	mV/ $^{\circ}C$
vs Power Supply PSRR	$V_S = +2.7V$ to $+5.5V$, $V_{CM} = V_S/2 - 0.15V$		± 80	± 350	$\mu V/V$
INPUT BIAS CURRENT					
Input Bias Current I_B			3	± 50	pA
Input Offset Current I_{OS}			± 1	± 50	pA
NOISE					
Input Noise Voltage Density e_n	$f = 1MHz$		5.8		$nV/\sqrt{Hz}$
Current Noise Density i_n	$f = 1MHz$		50		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE					
Common-Mode Voltage Range V_{CM}	$V_S = +5.5V$, $-0.1V < V_{CM} < +4.0V$	$(V-) - 0.1$		$(V+) - 1.5$	V
Common-Mode Rejection Ratio CMRR	Specified Temperature Range	66	80		dB
		66			dB
INPUT IMPEDANCE					
Differential			$10^{13} \parallel 1.5$		$\Omega \parallel pF$
Common-Mode			$10^{13} \parallel 1.5$		$\Omega \parallel pF$
OPEN-LOOP GAIN					
	$V_S = +5V$, $0.3V < V_O < 4.7V$	84	92		dB
OPA355	$V_S = +5V$, $0.3V < V_O < 4.7V$	80			dB
OPA2355, OPA3355	$V_S = +5V$, $0.4V < V_O < 4.6V$	80			dB
FREQUENCY RESPONSE					
Small-Signal Bandwidth f_{-3dB}	$G = +1$, $V_O = 100mVp-p$, $R_F = 0\Omega$		450		MHz
f_{-3dB}	$G = +2$, $V_O = 100mVp-p$, $R_L = 50\Omega$		100		MHz
f_{-3dB}	$G = +2$, $V_O = 100mVp-p$, $R_L = 150\Omega$		170		MHz
f_{-3dB}	$G = +2$, $V_O = 100mVp-p$, $R_L = 1k\Omega$		200		MHz
Gain-Bandwidth Product GBW	$G = +10$, $R_L = 1k\Omega$		200		MHz
Bandwidth for 0.1dB Gain Flatness $f_{0.1dB}$	$G = +2$, $V_O = 100mVp-p$, $R_F = 560\Omega$		75		MHz
Slew Rate SR	$V_S = +5V$, $G = +2$, 4V Output Step		300/–360		V/ μs
Rise-and-Fall Time	$G = +2$, $V_O = 200mVp-p$, 10% to 90%		2.4		ns
	$G = +2$, $V_O = 2Vp-p$, 10% to 90%		8		ns
Settling Time, 0.1%	$V_S = +5V$, $G = +2$, 2V Output Step		30		ns
0.01%	$V_S = +5V$, $G = +2$, 2V Output Step		120		ns
Overload Recovery Time	$V_{IN} \cdot \text{Gain} = V_S$		8		ns
Harmonic Distortion					
2nd-Harmonic	$G = +2$, $f = 1MHz$, $V_O = 2Vp-p$, $R_L = 200\Omega$		–81		dBc
3rd-Harmonic	$G = +2$, $f = 1MHz$, $V_O = 2Vp-p$, $R_L = 200\Omega$		–93		dBc
Differential Gain Error	NTSC, $R_L = 150\Omega$		0.02		%
Differential Phase Error	NTSC, $R_L = 150\Omega$		0.05		degrees
Channel-to-Channel Crosstalk OPA2355	$f = 5MHz$		–90		dB
OPA3355	$f = 5MHz$		–70		dB
OUTPUT					
Voltage Output Swing from Rail	$V_S = +5V$, $R_L = 150\Omega$, $A_{OL} > 84dB$		0.2	0.3	V
Voltage Output Swing from Rail	$V_S = +5V$, $R_L = 1k\Omega$		0.1		V
Output Current, Continuous ⁽¹⁾ I_O			± 60		mA
Output Current, Peak ⁽¹⁾ I_O	$V_S = +5V$		± 100		mA
Output Current, Peak ⁽¹⁾ I_O	$V_S = +3V$		± 80		mA
Closed-Loop Output Impedance	$f < 100kHz$		0.02		Ω
POWER SUPPLY					
Specified Voltage Range V_S		2.7		5.5	V
Operating Voltage Range			2.5 to 5.5		V
Quiescent Current (per amplifier) I_Q	$V_S = +5V$, Enabled, $I_O = 0$		8.3	11	mA
	Specified Temperature Range			14	mA

NOTES: (1) See typical characteristic *Output Voltage Swing vs Output Current*. (2) Logic LOW and HIGH levels are CMOS logic compatible. They are referenced to V_- .

ELECTRICAL CHARACTERISTICS: $V_S = +2.7V$ to $+5.5V$ Single-Supply (Cont.)

Boldface limits apply over the specified temperature range, $T_A = -40^{\circ}C$ to $+125^{\circ}C$.

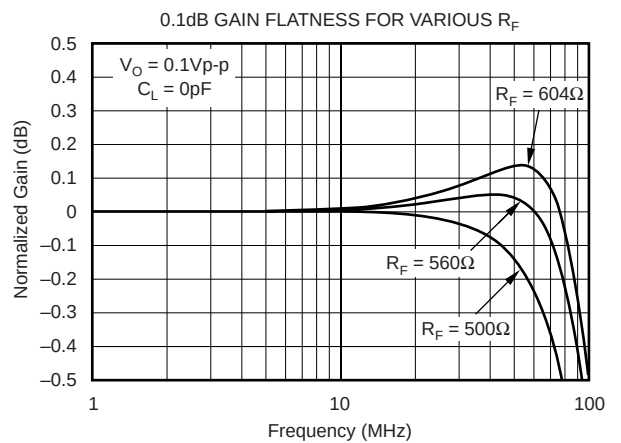
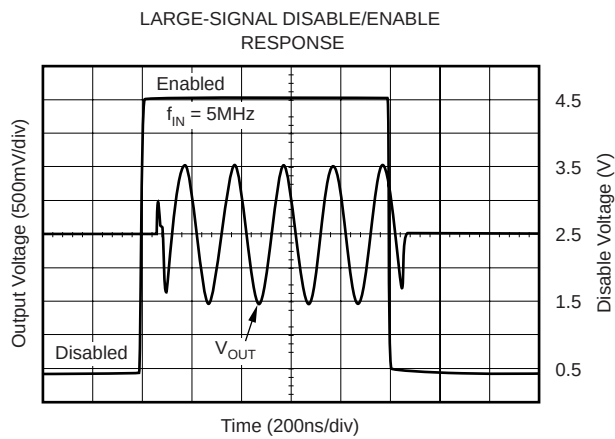
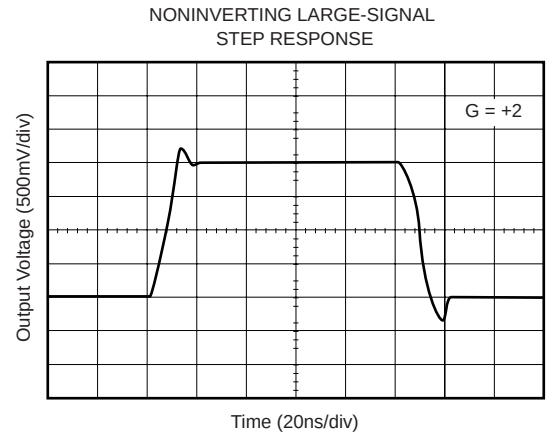
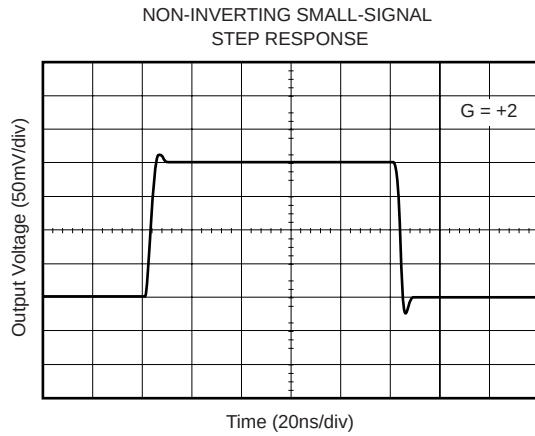
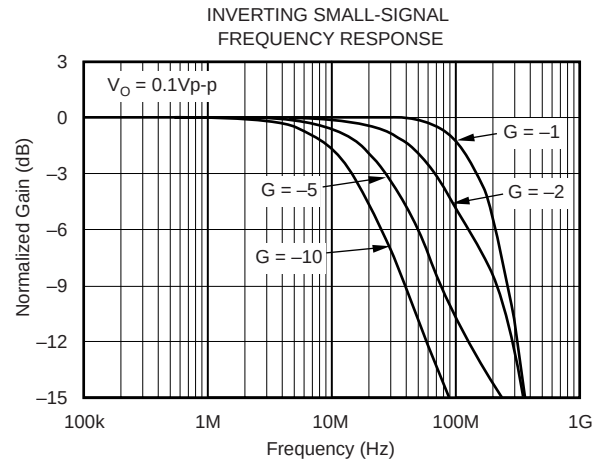
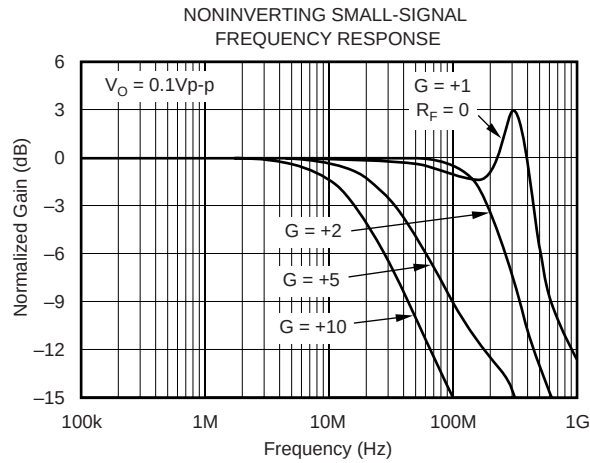
At $T_A = +25^{\circ}C$, $R_F = 604\Omega$, $R_L = 150\Omega$, and connected to $V_S/2$, unless otherwise noted.

PARAMETER	CONDITION	OPA355 OPA2355 OPA3355			UNITS
		MIN	TYP	MAX	
SHUTDOWN					
Disabled (Logic-LOW Threshold) ⁽²⁾				0.8	V
Enabled (Logic-HIGH Threshold) ⁽²⁾		2			V
Enable Time			100		ns
Disable Time			30		ns
Shutdown Current (per amplifier)	$V_S = +5V$, Disabled		3.4	6	μA
THERMAL SHUTDOWN					
Junction Temperature					
Shutdown			160		$^{\circ}C$
Reset from Shutdown			140		$^{\circ}C$
TEMPERATURE RANGE					
Specified Range		-40		125	$^{\circ}C$
Operating Range		-55		150	$^{\circ}C$
Storage Range		-65		150	$^{\circ}C$
Thermal Resistance θ_{JA}					$^{\circ}C/W$
SOT-23-6, MSOP-10			150		$^{\circ}C/W$
SO-8			125		$^{\circ}C/W$
SO-14, TSSOP-14			100		$^{\circ}C/W$

NOTES: (1) See typical characteristic *Output Voltage Swing vs Output Current*. (2) Logic LOW and HIGH levels are CMOS logic compatible. They are referenced to V_- .

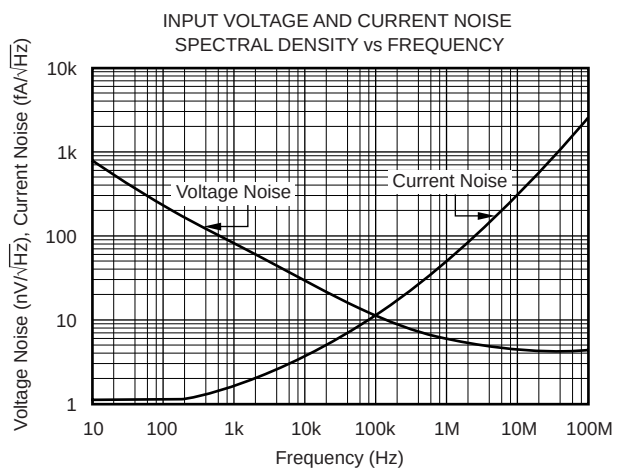
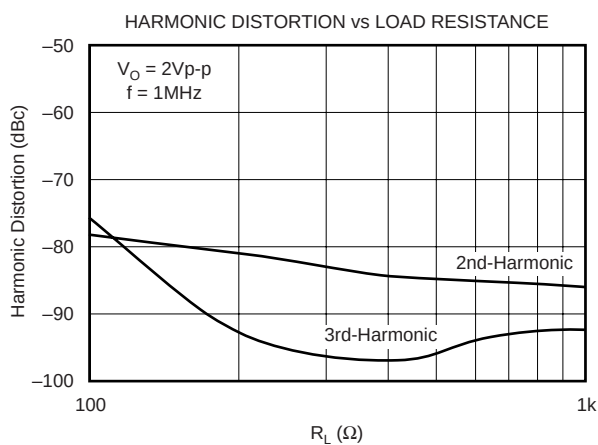
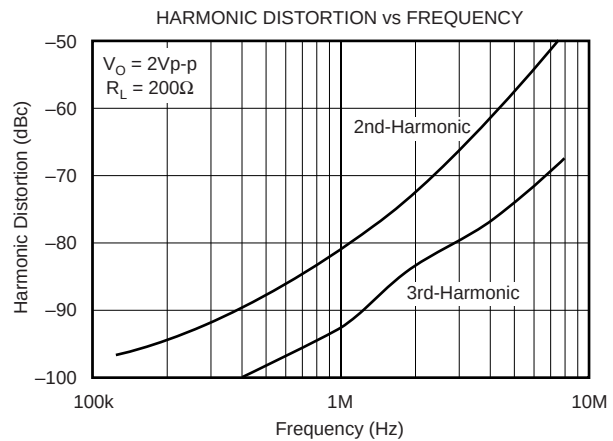
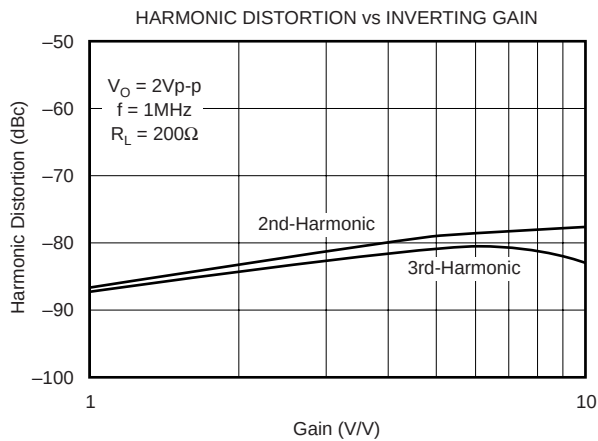
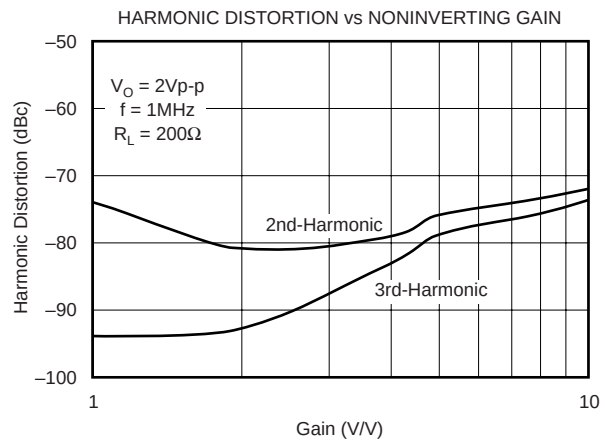
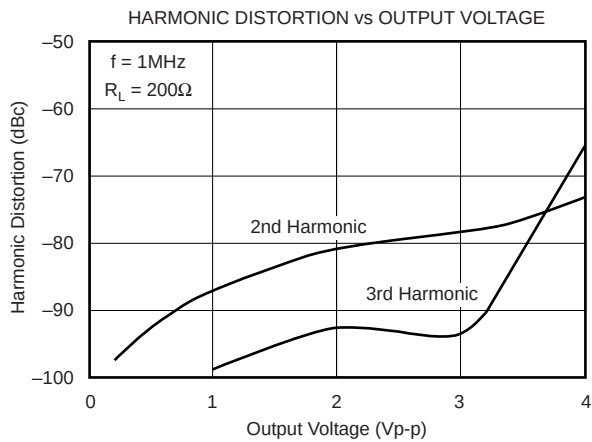
TYPICAL CHARACTERISTICS

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $G = +2$, $R_F = 604\Omega$, and $R_L = 150\Omega$ connected to $V_S/2$, unless otherwise noted.



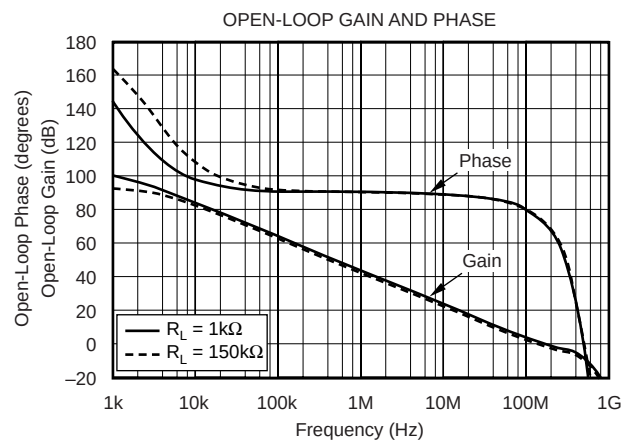
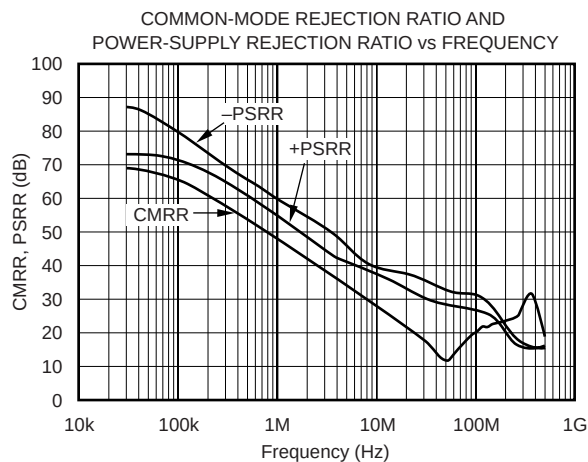
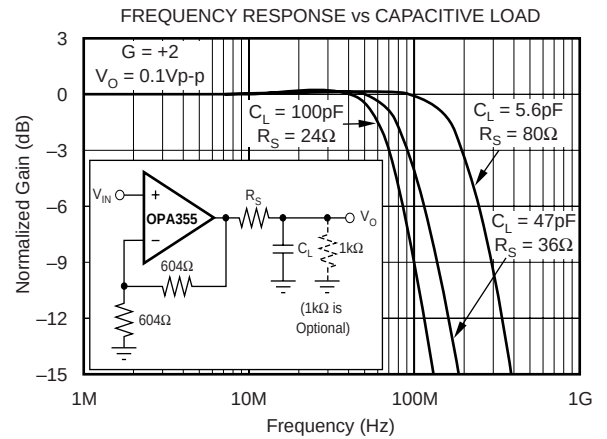
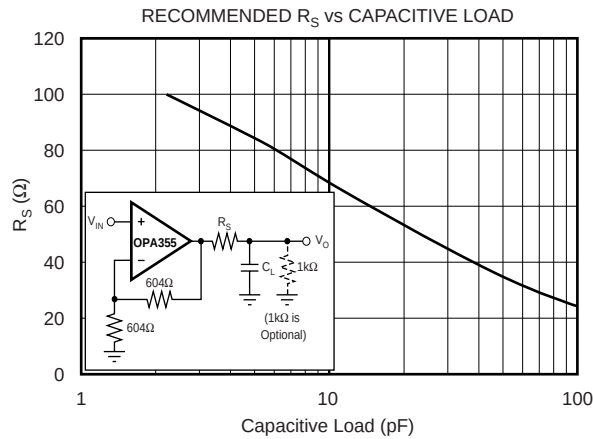
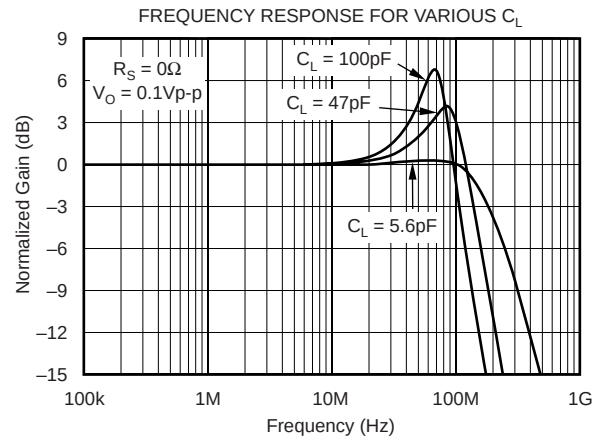
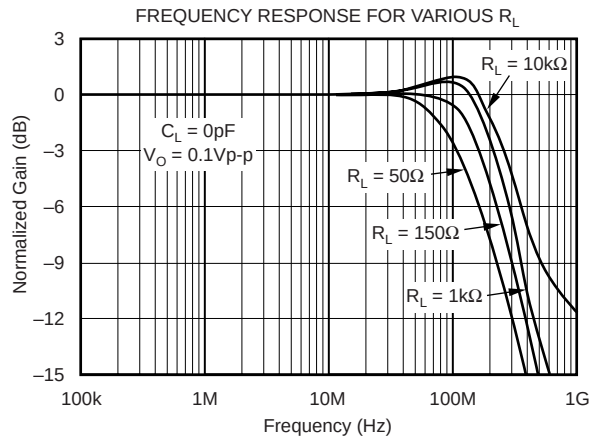
TYPICAL CHARACTERISTICS (Cont.)

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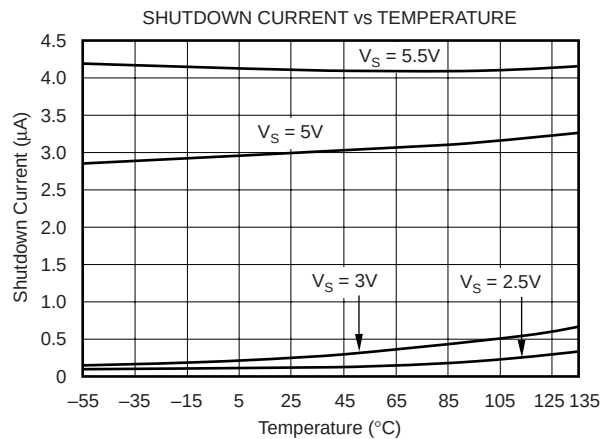
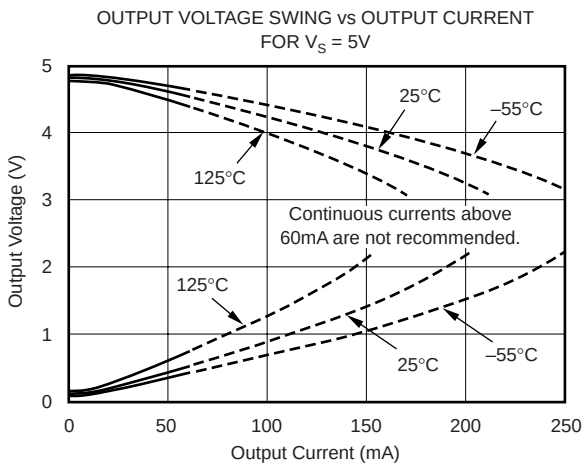
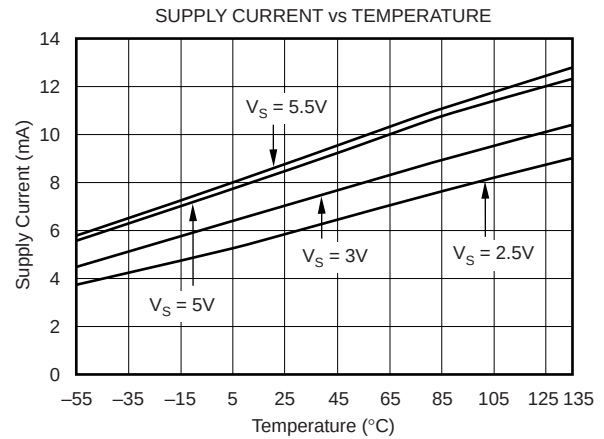
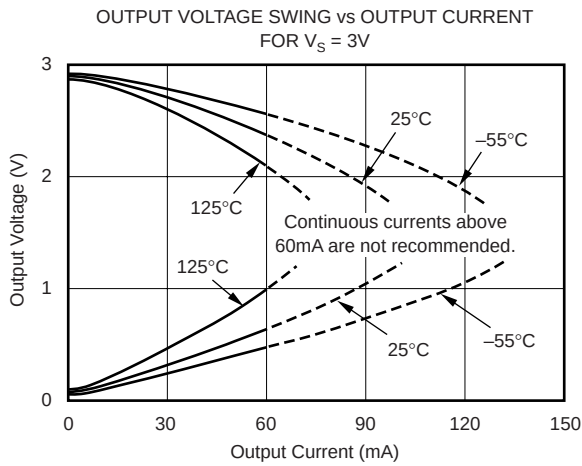
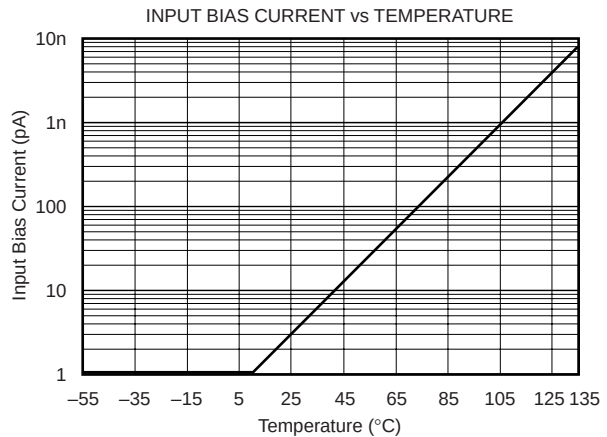
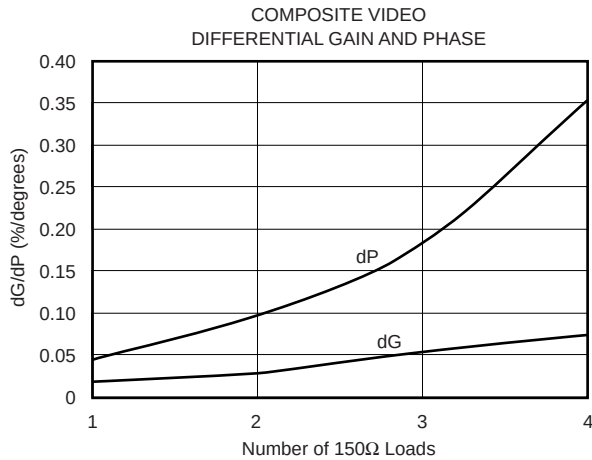
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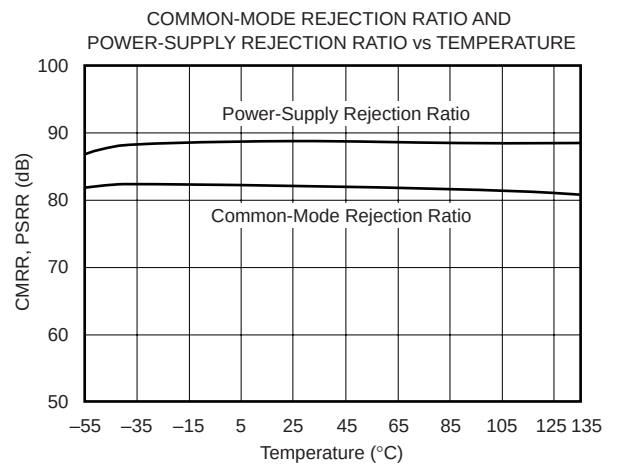
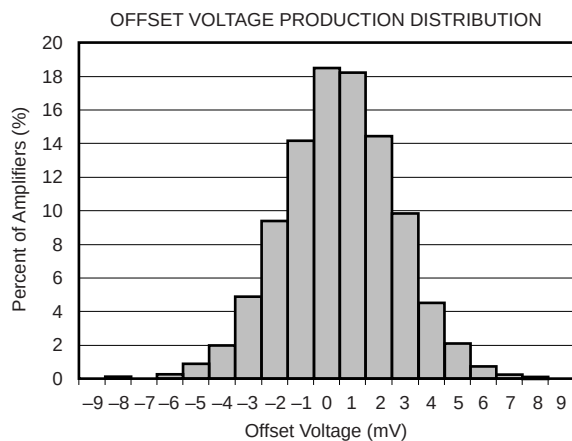
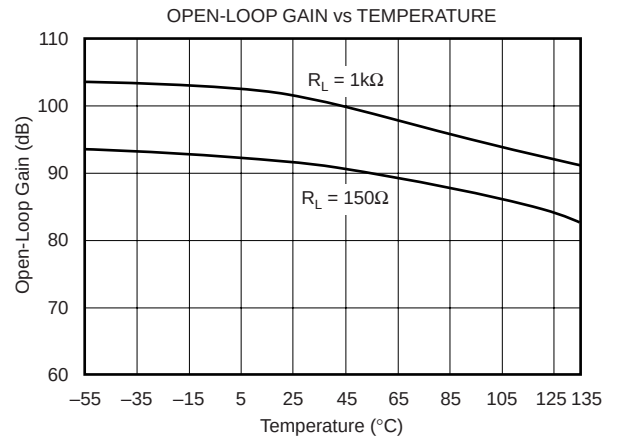
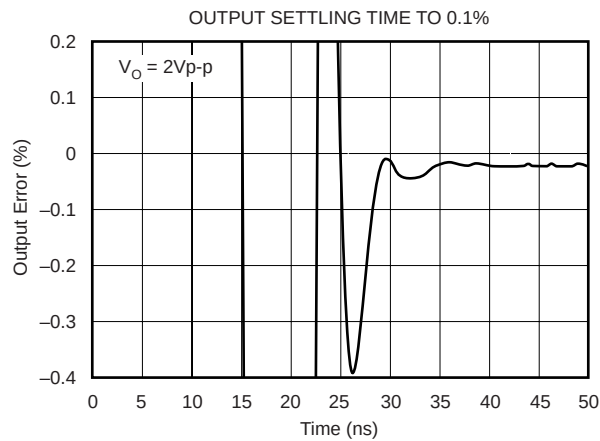
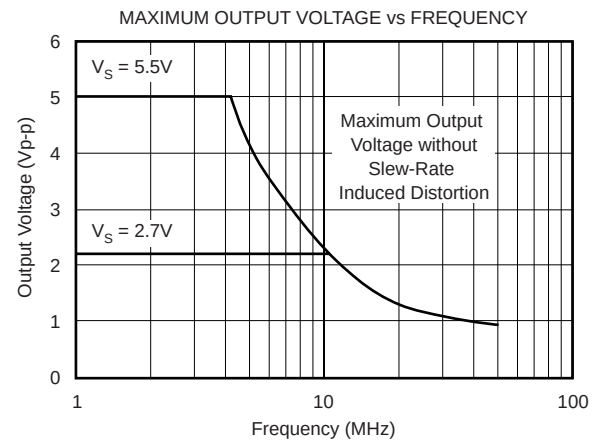
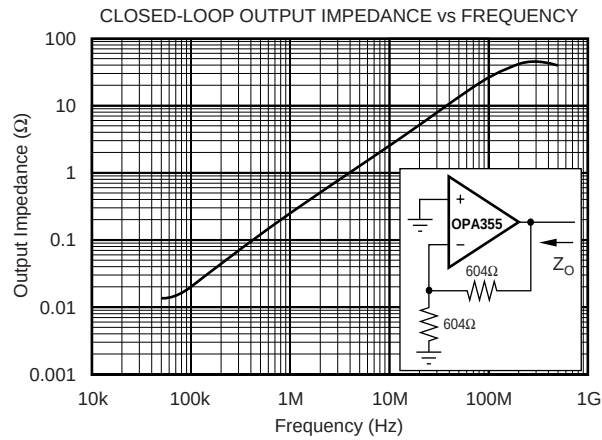
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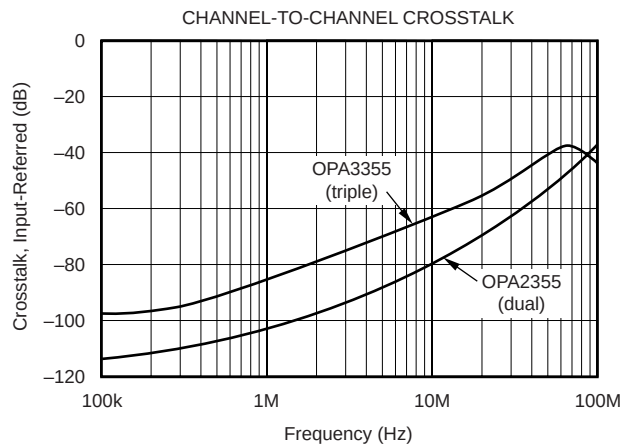
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TYPICAL CHARACTERISTICS (Cont.)

At $T_A = +25^\circ\text{C}$, $V_S = 5\text{V}$, $G = +2$, $R_F = 604\Omega$, and $R_L = 150\Omega$ connected to $V_S/2$, unless otherwise noted.



APPLICATIONS INFORMATION

The OPA355 series is a CMOS, high-speed, voltage-feed-back, operational amplifier designed for video and other general-purpose applications. It is available as a single, dual, or triple op amp.

The amplifier features a 200MHz gain bandwidth and 360V/ μs slew rate, but it is unity-gain stable and can be operated as a +1V/V voltage follower.

Its input common-mode voltage range includes ground, allowing the OPA355 to be used in virtually any single-supply application up to a supply voltage of +5.5V.

PCB LAYOUT

Good high-frequency PC board layout techniques should be employed for the OPA355. Generous use of ground planes, short direct signal traces, and a suitable bypass capacitor located at the V+ pin will assure clean, stable operation. Large areas of copper also provide a means of dissipating heat that is generated within the amplifier in normal operation.

Sockets are definitely not recommended for use with any high-speed amplifier.

A 10nF ceramic bypass capacitor is the minimum recommended value; adding a 1 μF or larger tantalum capacitor in

parallel can be beneficial when driving a low-resistance load. Providing adequate bypass capacitance is essential to achieving very low harmonic and intermodulation distortion.

OPERATING VOLTAGE

The OPA355 is specified over a power-supply range of +2.7V to +5.5V ($\pm 1.35\text{V}$ to $\pm 2.75\text{V}$). However, the supply voltage may range from +2.5V to +5.5V ($\pm 1.25\text{V}$ to $\pm 2.75\text{V}$). Supply voltages higher than 7.5V (absolute maximum) can permanently damage the amplifier.

Parameters that vary significantly over supply voltage or temperature are shown in the Typical Characteristics section of this data sheet.

ENABLE FUNCTION

The OPA355 can be enabled by applying a TTL HIGH voltage level to the Enable pin. Conversely, a TTL LOW voltage level will disable the amplifier, reducing its supply current from 8.3mA to only 3.4 μA per amplifier. This pin voltage is referenced to single-supply ground. When using a split-supply, such as $\pm 2.5\text{V}$, the enable/disable voltage levels will be referenced to V-. Independent Enable pins are available for each channel, providing maximum design flexibility. For portable battery-operated applications, this feature can be used to greatly reduce the average current and thereby extend battery life.

The Enable input can be modeled as a CMOS input gate with a 100k Ω pull-up resistor to V+. Left open, the Enable pin will assume a logic HIGH, and the amplifier will be on.

The Enable time is 100ns and the disable time is only 30ns. This allows the OPA355 to be operated as a “gated” amplifier, or to have its output multiplexed onto a common output bus. When disabled, the output assumes a high-impedance state.

OUTPUT DRIVE

The output stage can supply high short-circuit current (typically over 200mA). Therefore, an on-chip thermal shutdown circuit is provided to protect the OPA355 from dangerously high junction temperatures. At 160°C, the protection circuit will shut down the amplifier. Normal operation will resume when the junction temperature cools to below 140°C.

NOTE: it is not recommended to run a continuous DC current in excess of ± 60 mA. Refer to the Typical Characteristics, *Output Voltage Swing vs Output Current*.

VIDEO

The OPA355 output stage is capable of driving a standard back-terminated 75 Ω video cable. By back-terminating a transmission line, it does not exhibit a capacitive load to its

driver. A properly back-terminated 75 Ω cable does not appear as capacitance; it presents only a 150 Ω resistive load to the OPA355 output.

The OPA355 can be used as an amplifier for RGB graphic signals, which have a voltage of zero at the video black level, by offsetting and AC-coupling the signal, as shown in Figure 1.

WIDEBAND VIDEO MULTIPLEXING

One common application for video speed amplifiers which include an enable pin is to wire multiple amplifier outputs together, then select which one of several possible video inputs to source onto a single line. This simple *Wired-OR Video Multiplexer* can be easily implemented using the OPA355; see Figure 2.

INPUT AND ESD PROTECTION

All OPA355 pins are static protected with internal ESD protection diodes tied to the supplies; see Figure 3.

These diodes will provide overdrive protection if the current is externally limited to 10mA by the source or by a resistor.

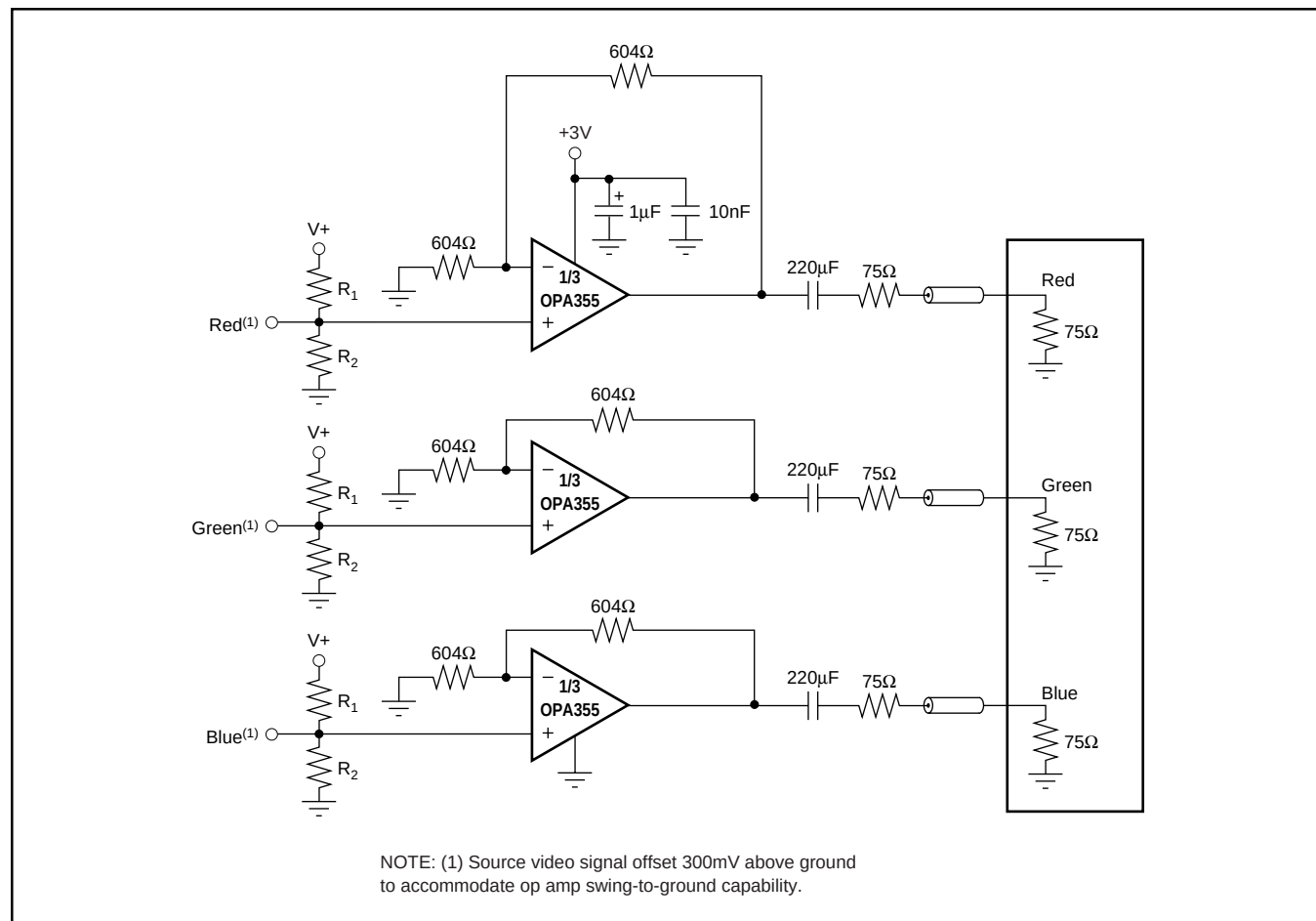


FIGURE 1. RGB Cable Driver.

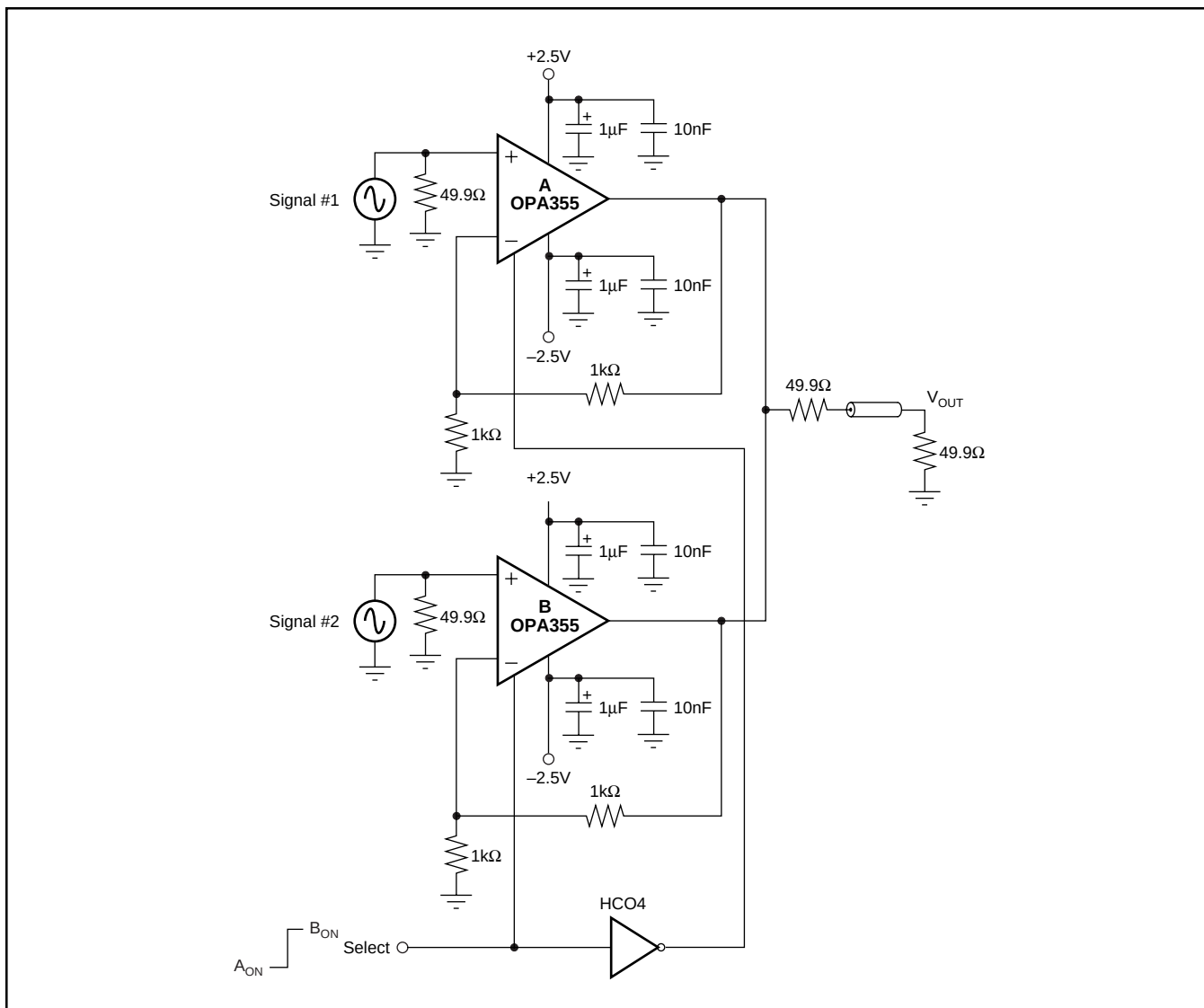


FIGURE 2. Multiplexed Output.

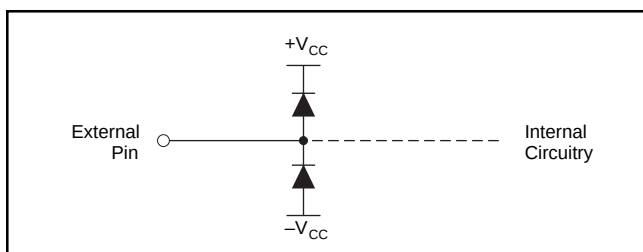


FIGURE 3. Internal ESD Protection.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
OPA2355DGSA/250	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D55	Samples
OPA2355DGSA/250G4	ACTIVE	VSSOP	DGS	10	250	Green (RoHS & no Sb/Br)	CU NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	D55	Samples
OPA3355EA/250	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 3355EA	Samples
OPA3355EA/250G4	ACTIVE	TSSOP	PW	14	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 3355EA	Samples
OPA3355EA/2K5	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 3355EA	Samples
OPA3355EA/2K5G4	ACTIVE	TSSOP	PW	14	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 3355EA	Samples
OPA3355UA	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA3355UA	Samples
OPA3355UAG4	ACTIVE	SOIC	D	14	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA3355UA	Samples
OPA355NA/250	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C55	Samples
OPA355NA/250G4	ACTIVE	SOT-23	DBV	6	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C55	Samples
OPA355NA/3K	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C55	Samples
OPA355NA/3KG4	ACTIVE	SOT-23	DBV	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	C55	Samples
OPA355UA	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 355UA	Samples
OPA355UA/2K5	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 355UA	Samples
OPA355UA/2K5G4	ACTIVE	SOIC	D	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 355UA	Samples
OPA355UAG4	ACTIVE	SOIC	D	8	75	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA 355UA	Samples

⁽¹⁾ The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

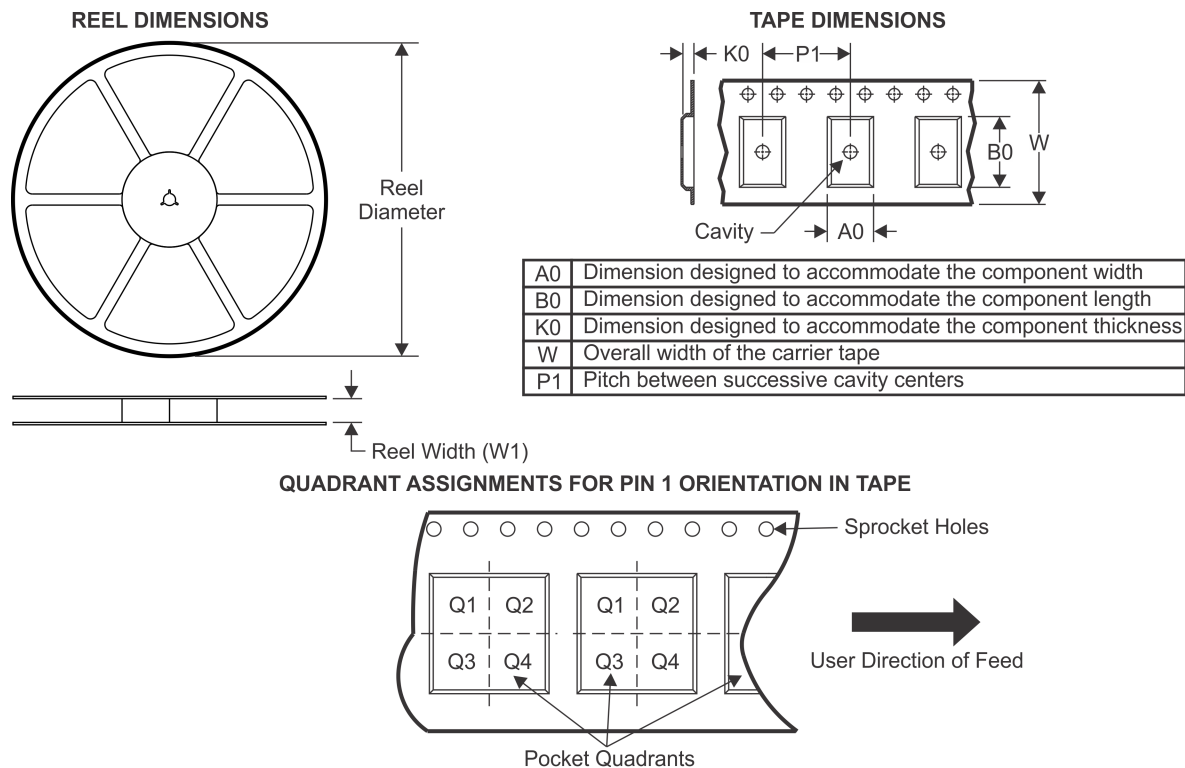
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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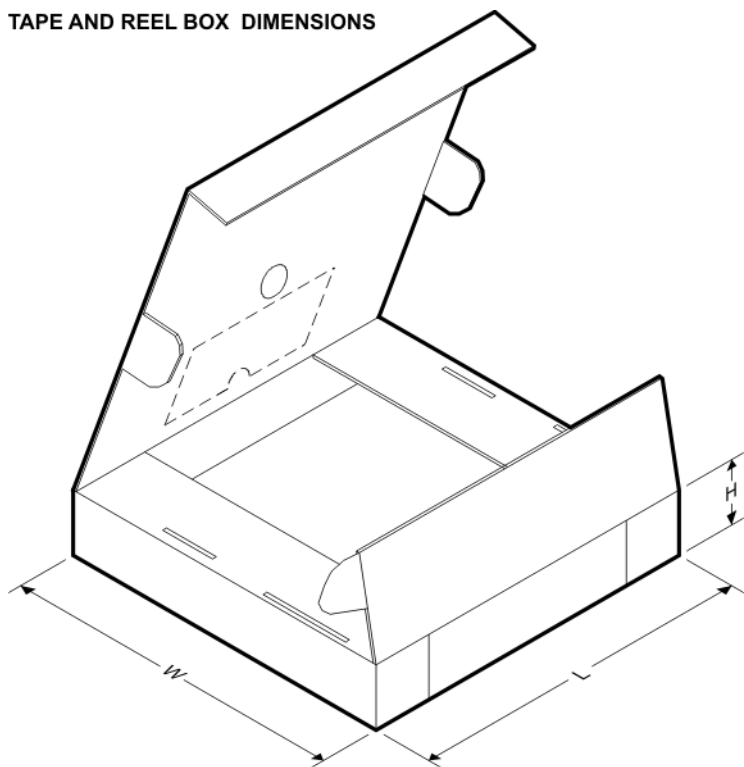
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TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2355DGSA/250	VSSOP	DGS	10	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA3355EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA3355EA/2K5	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA355UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

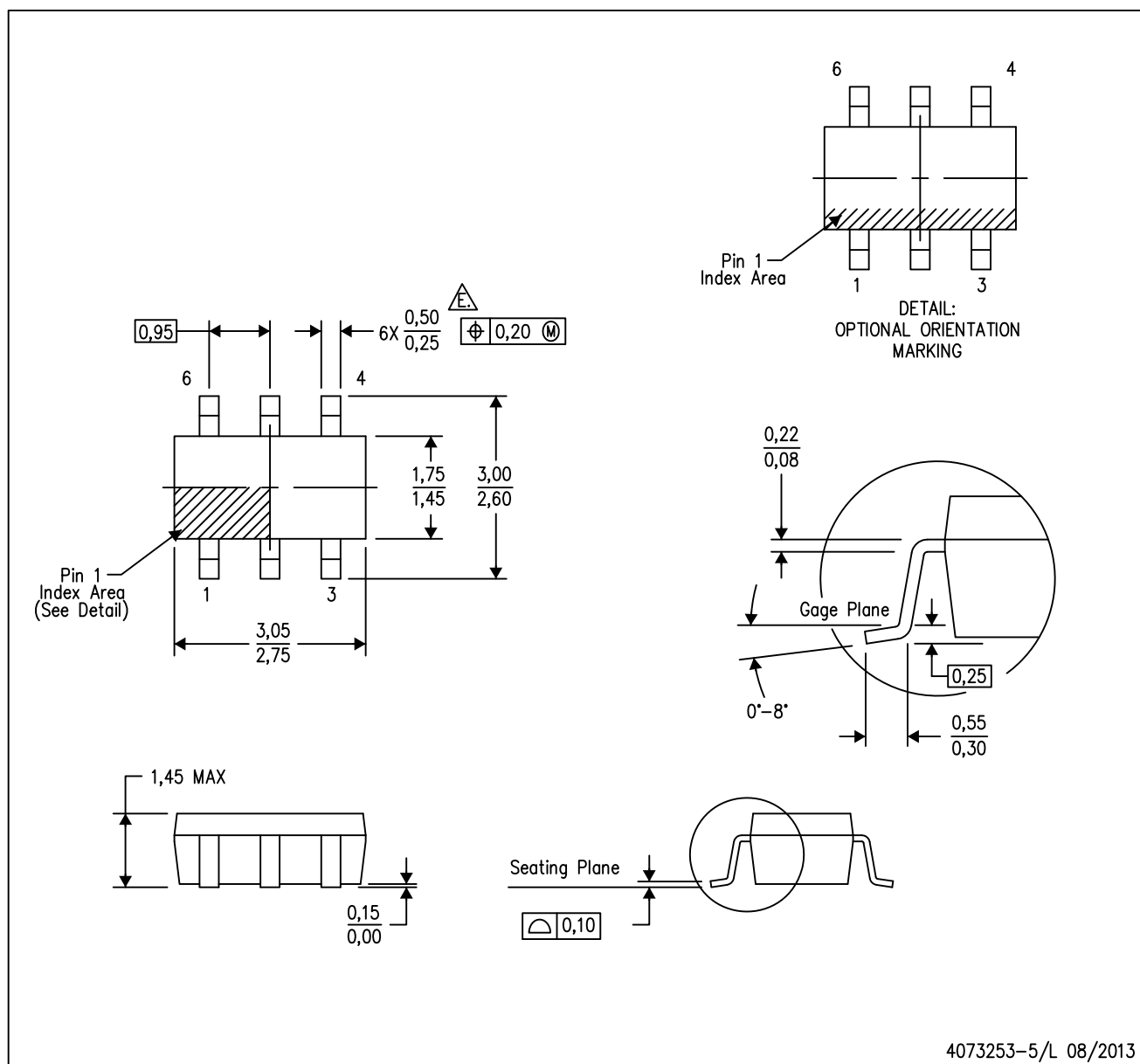


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2355DGSA/250	VSSOP	DGS	10	250	210.0	185.0	35.0
OPA3355EA/250	TSSOP	PW	14	250	210.0	185.0	35.0
OPA3355EA/2K5	TSSOP	PW	14	2500	367.0	367.0	35.0
OPA355UA/2K5	SOIC	D	8	2500	367.0	367.0	35.0

DBV (R-PDSO-G6)

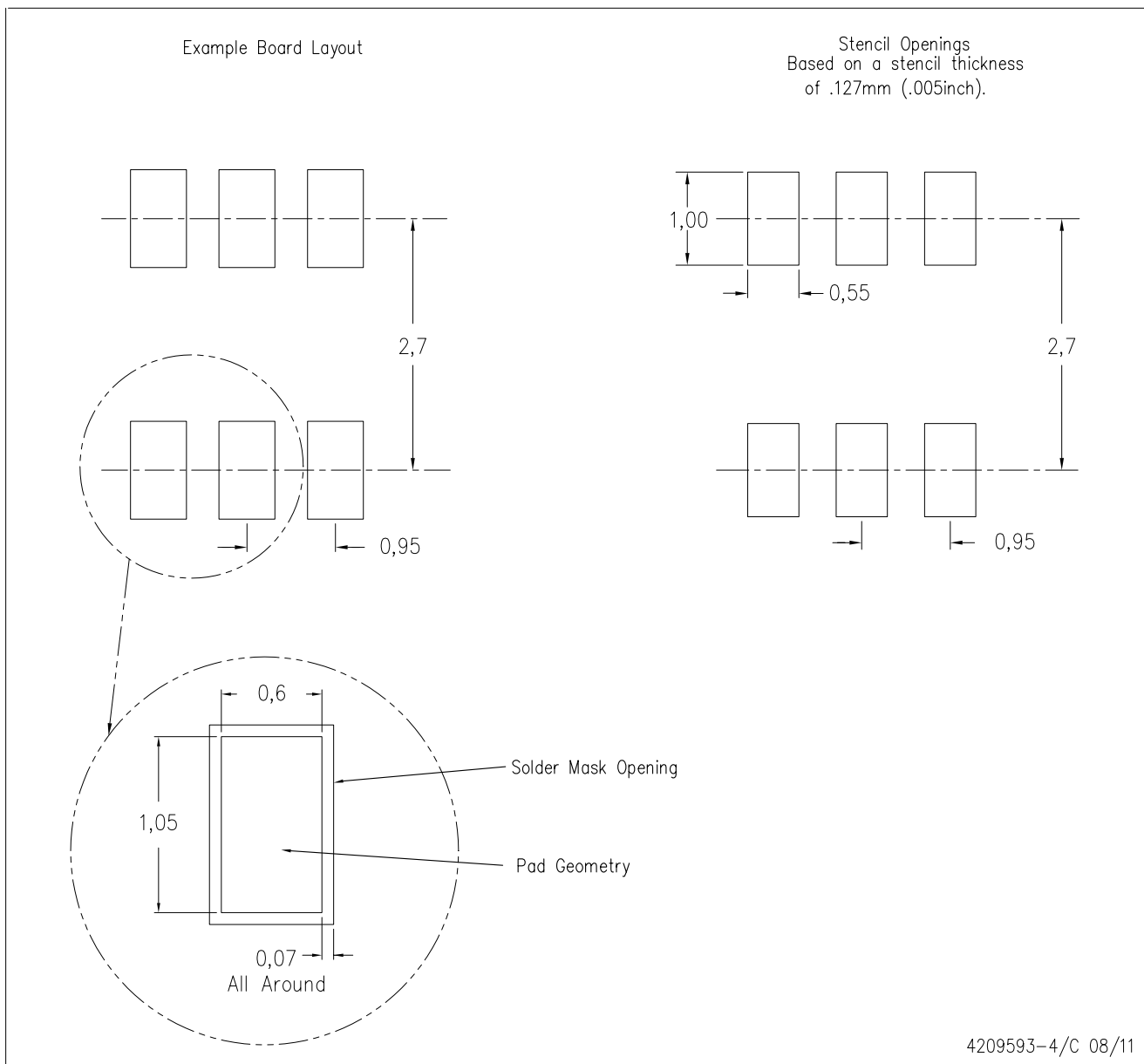
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
 - D. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
 - E. Falls within JEDEC MO-178 Variation AB, except minimum lead width.

DBV (R-PDSO-G6)

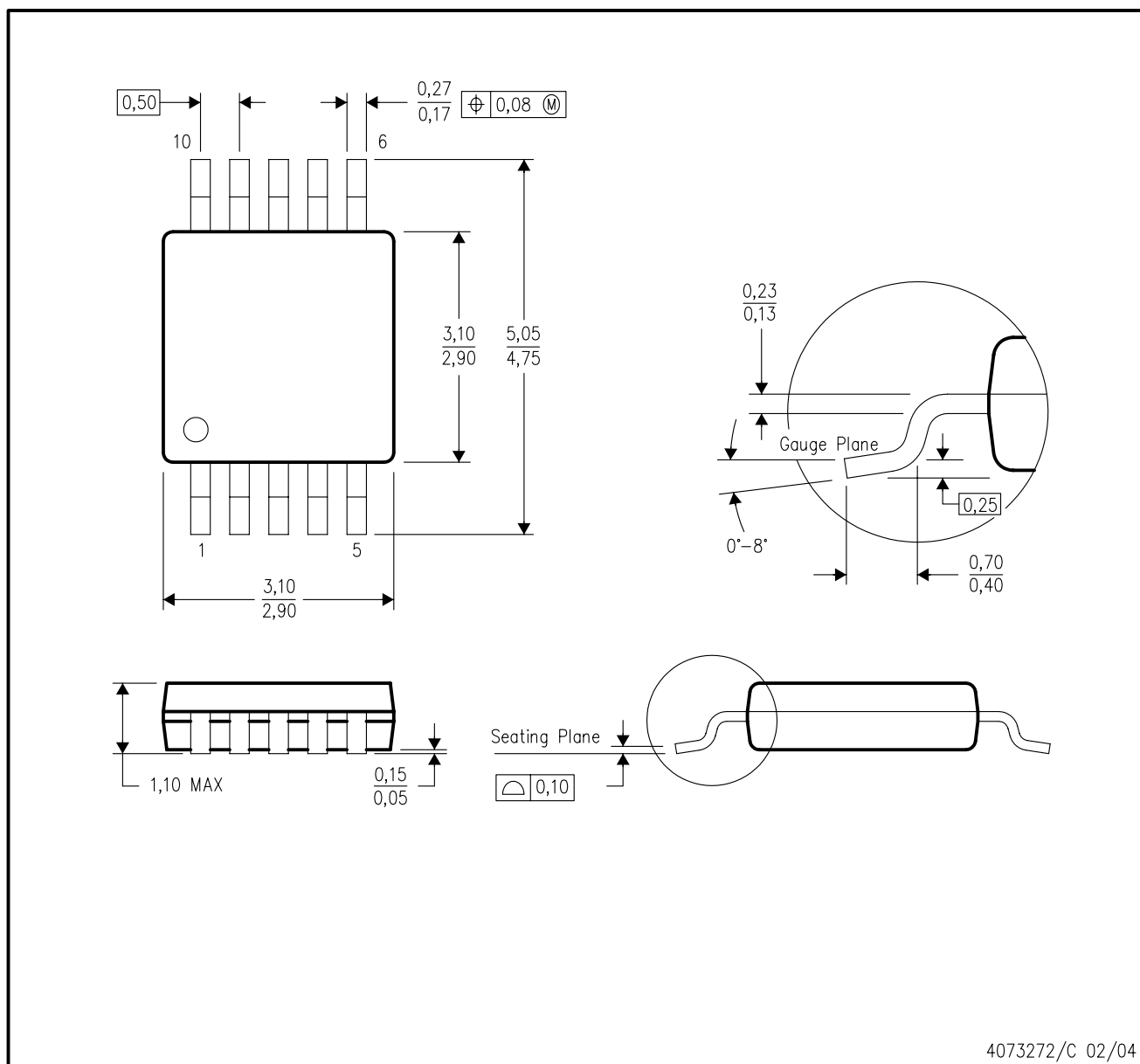
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
 - D. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

DGS (S-PDSO-G10)

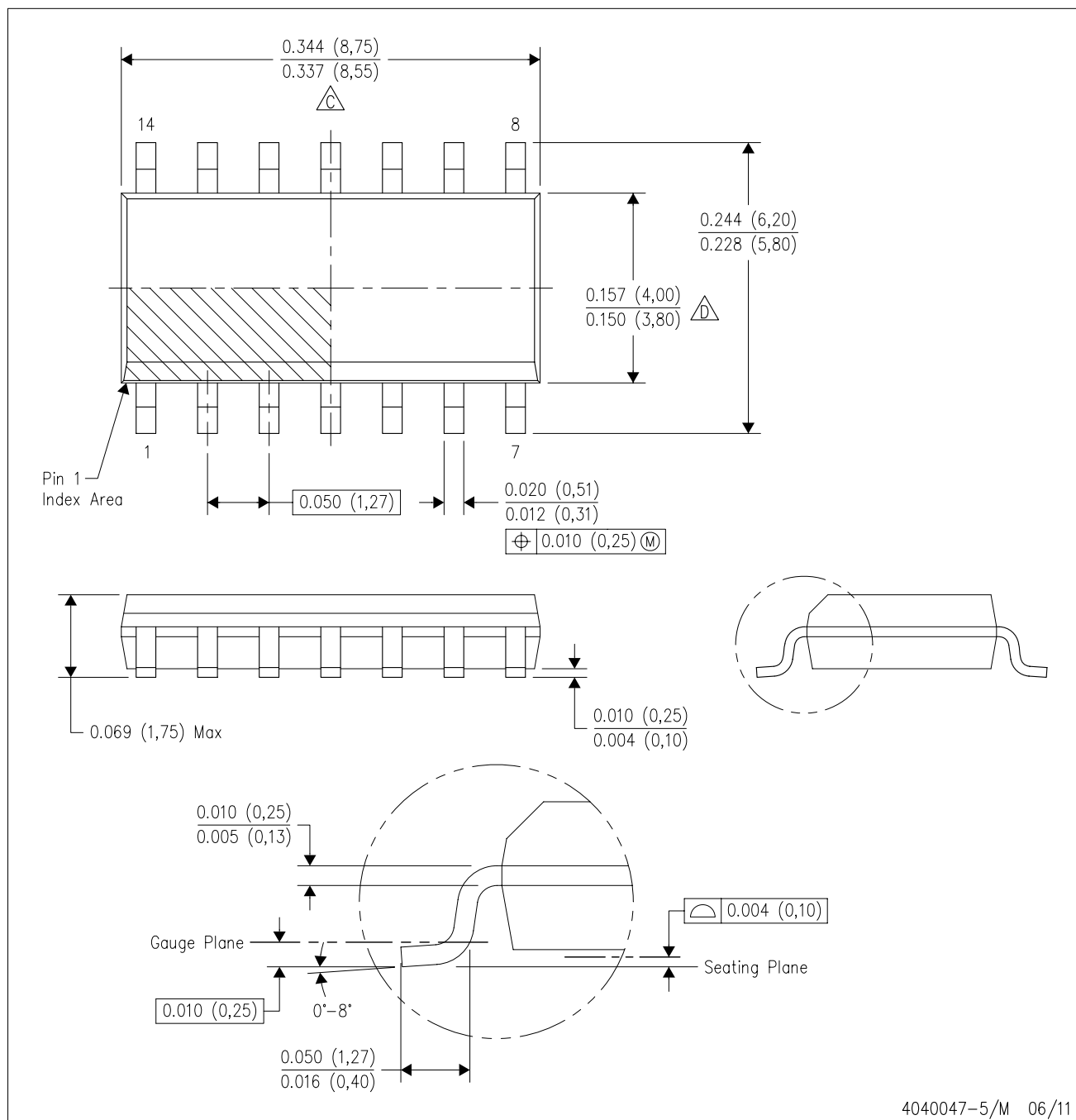
PLASTIC SMALL-OUTLINE PACKAGE



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D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



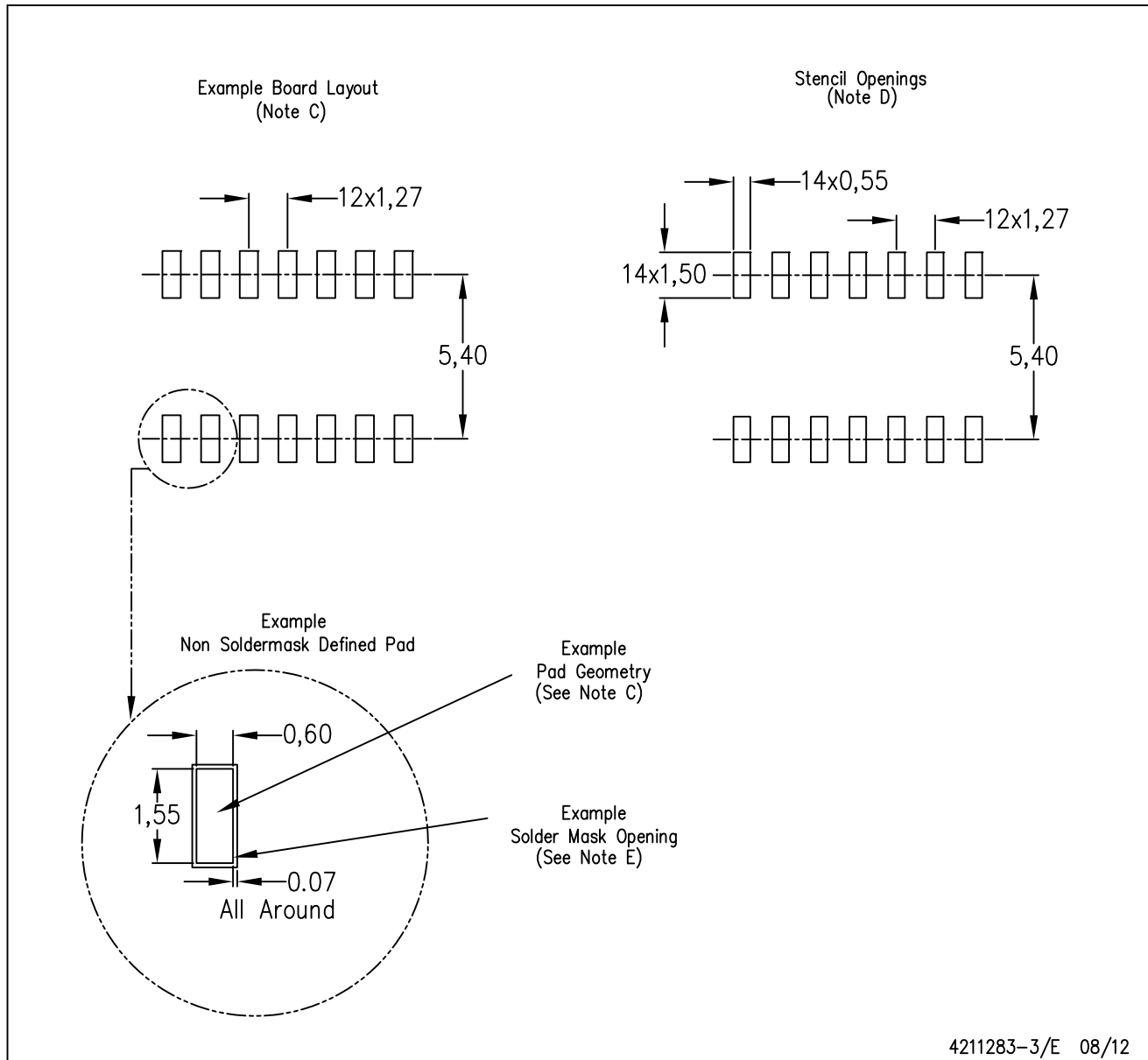
4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

D (R-PDSO-G14)

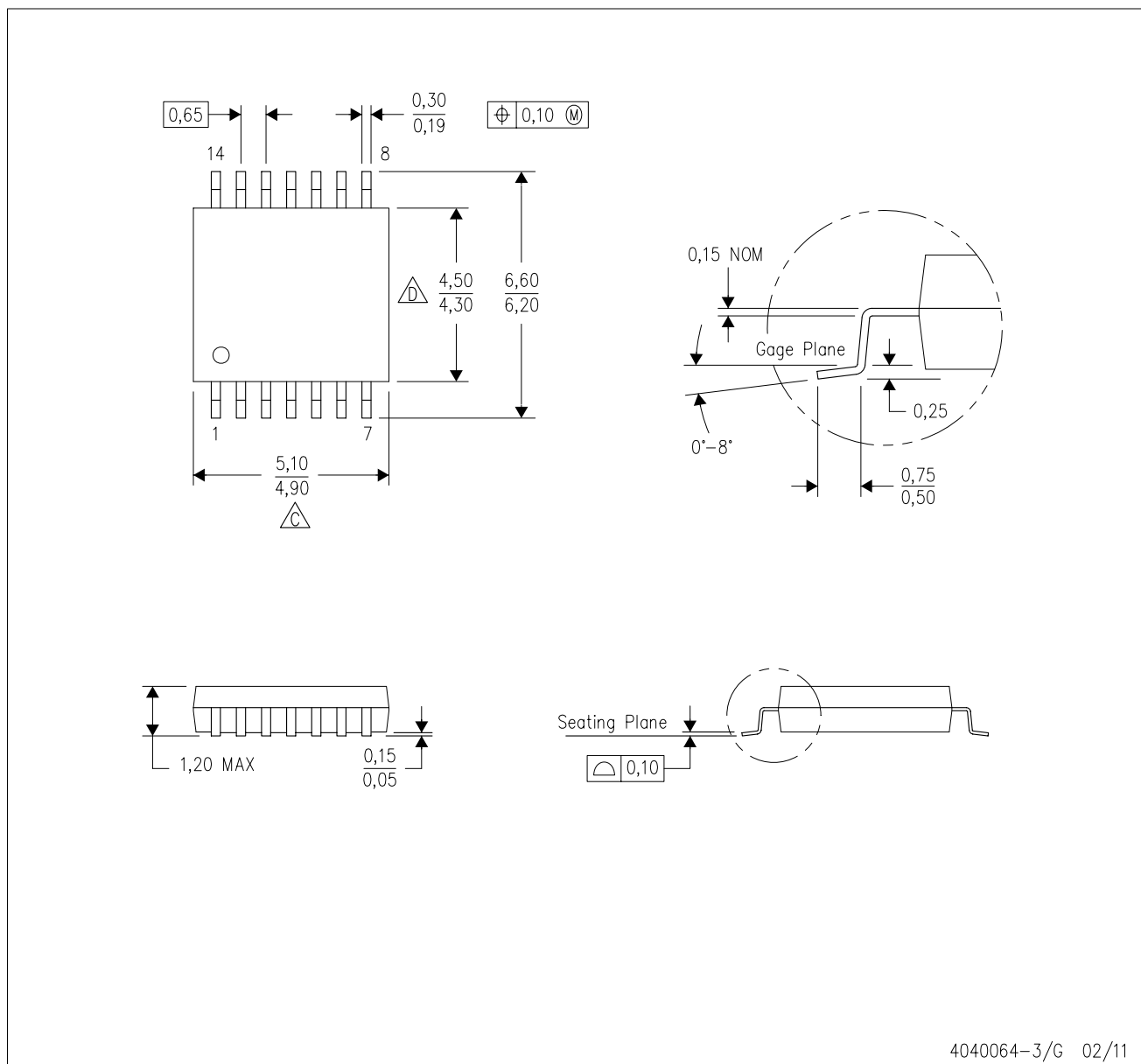
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

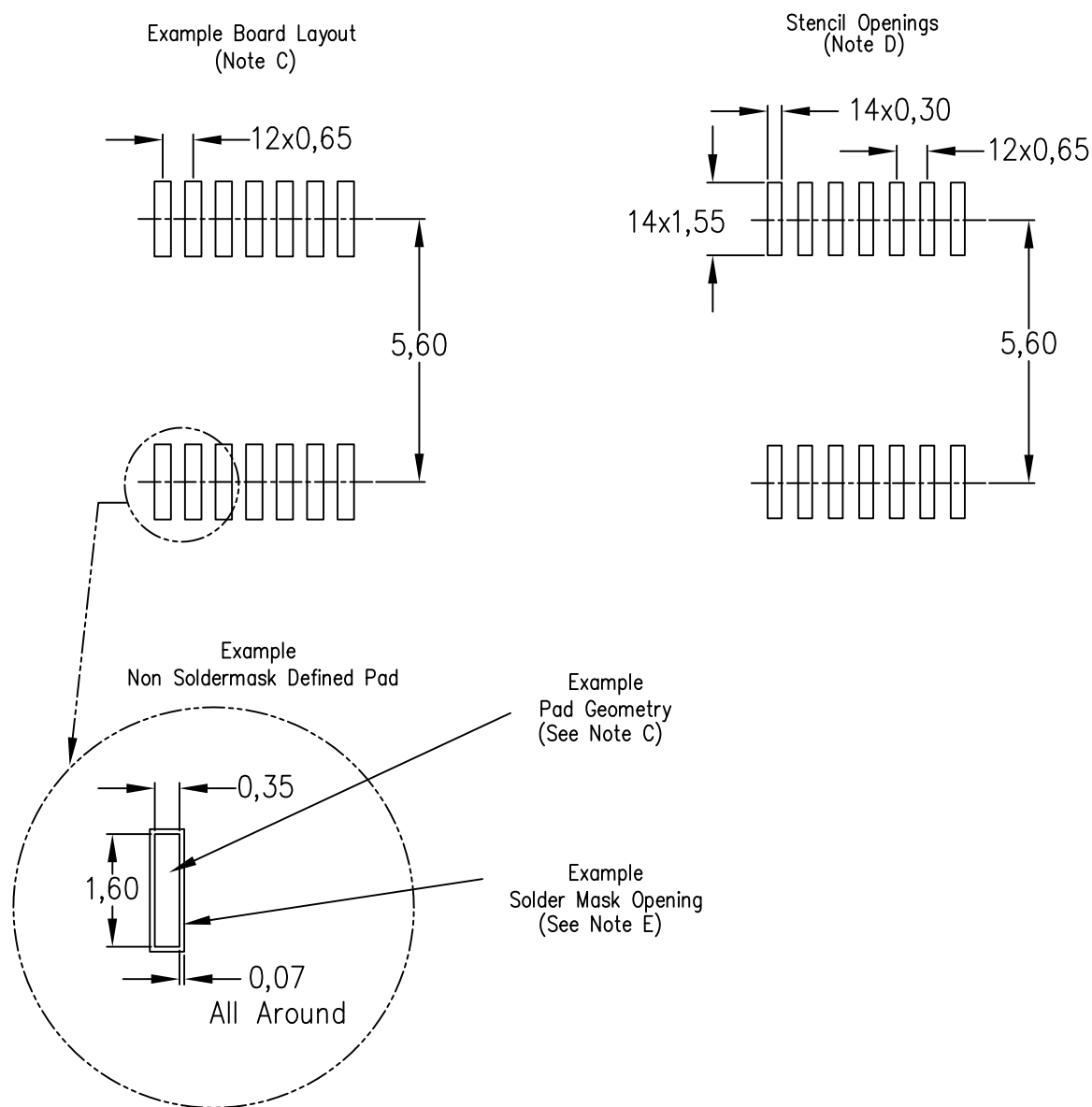
PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE

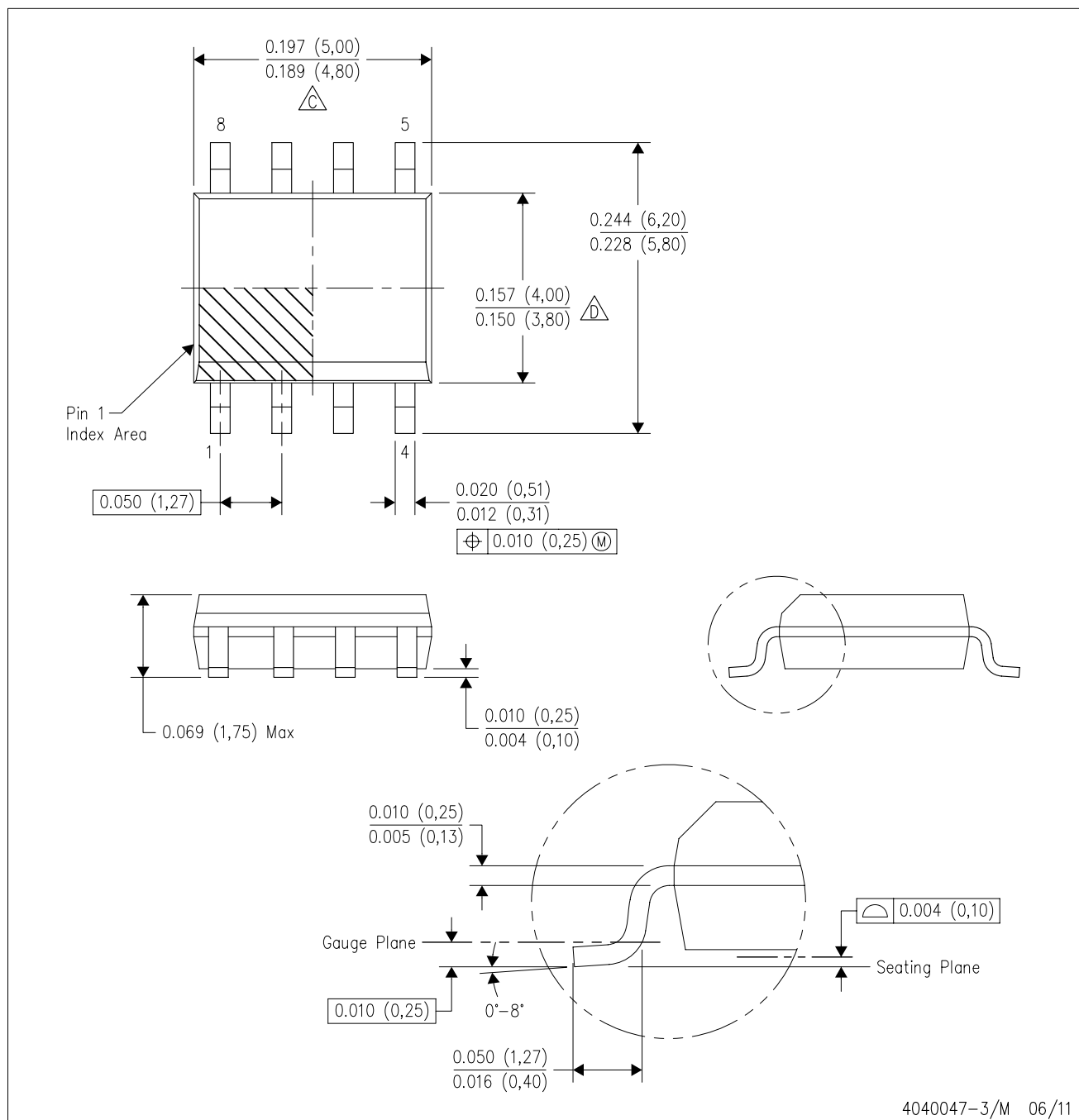


4211284-2/F 12/12

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D (R-PDSO-G8)

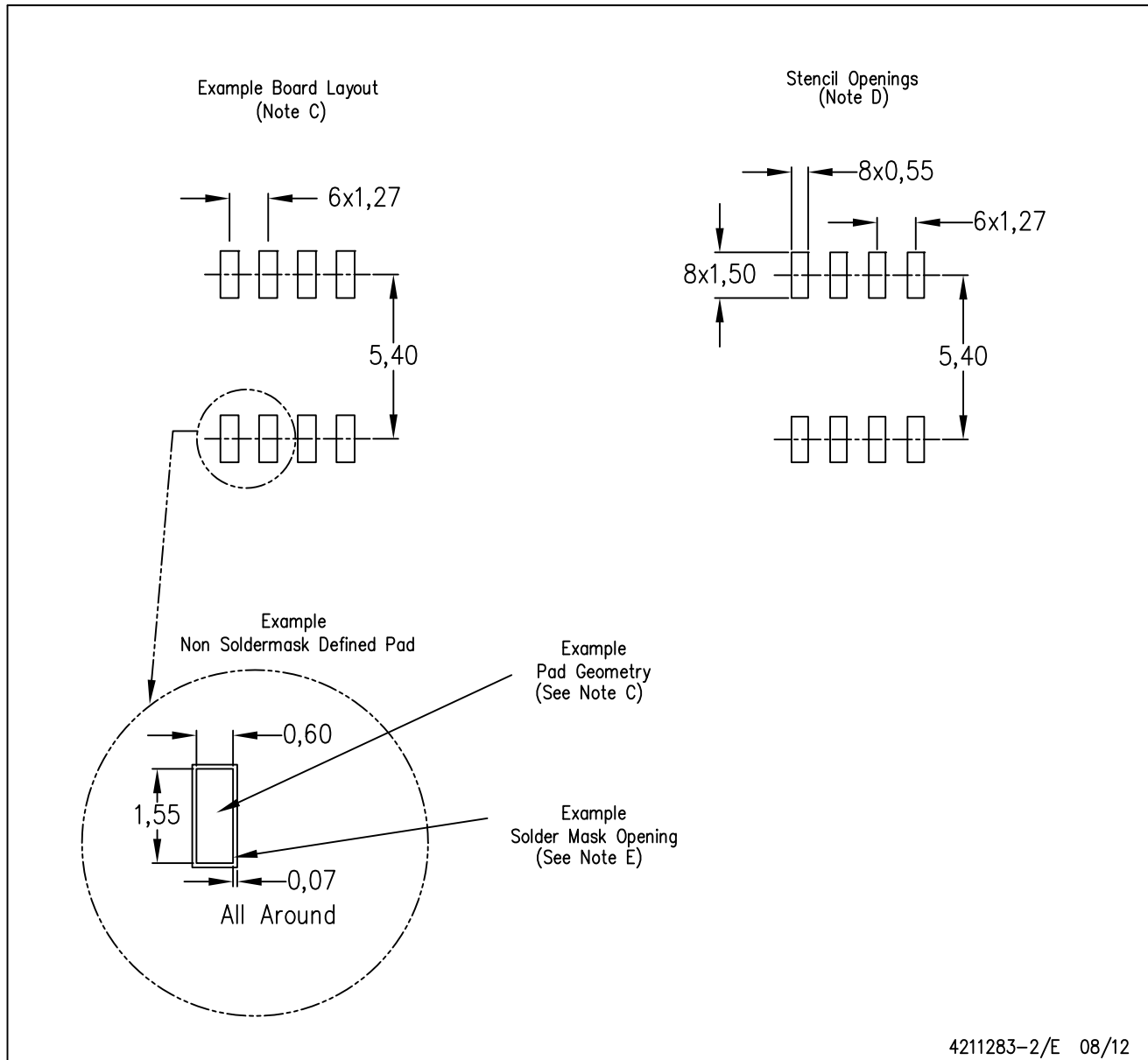
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
 - E. Reference JEDEC MS-012 variation AA.

D (R-PDSO-G8)

PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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