



Dual N-Channel 12-V (D-S) MOSFET

PRODUCT SUMMARY

V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) ^a	Q_g (Typ.)
12	0.040 at $V_{GS} = 4.5$ V	4.5	4.5 nC
	0.048 at $V_{GS} = 2.5$ V	4.5	
	0.063 at $V_{GS} = 1.8$ V	4.5	

FEATURES

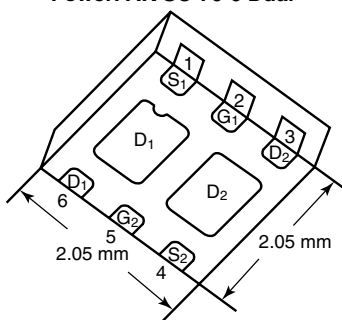
- Halogen-free
- TrenchFET[®] Power MOSFET
- New Thermally Enhanced PowerPAK[®] SC-70 Package
- Small Footprint Area

RoHS
COMPLIANT

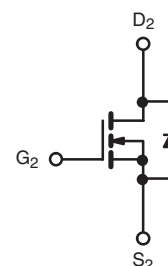
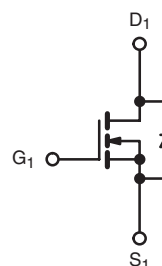
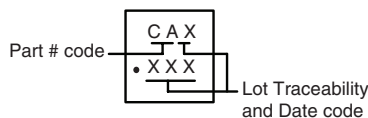
APPLICATIONS

- Load Switch for Portable Applications

PowerPAK SC-70-6 Dual



Marking Code



Ordering Information: SiA912DJ-T1-GE3 (Lead (Pb)-free and Halogen-free)

ABSOLUTE MAXIMUM RATINGS $T_A = 25^\circ\text{C}$, unless otherwise noted

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	12	V
Gate-Source Voltage	V_{GS}	± 8	
Continuous Drain Current ($T_J = 150^\circ\text{C}$)	$T_C = 25^\circ\text{C}$	4.5 ^a	A
	$T_C = 70^\circ\text{C}$	4.5 ^a	
	$T_A = 25^\circ\text{C}$	4.5 ^{a, b, c}	
	$T_A = 70^\circ\text{C}$	4.5 ^{a, b, c}	
Pulsed Drain Current	I_{DM}	20	A
Continuous Source-Drain Diode Current	$T_C = 25^\circ\text{C}$	4.5 ^a	
	$T_A = 25^\circ\text{C}$	1.6 ^{b, c}	
Maximum Power Dissipation	$T_C = 25^\circ\text{C}$	6.5	W
	$T_C = 70^\circ\text{C}$	5	
	$T_A = 25^\circ\text{C}$	1.9 ^{b, c}	
	$T_A = 70^\circ\text{C}$	1.2 ^{b, c}	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	- 55 to 150	$^\circ\text{C}$
Soldering Recommendations (Peak Temperature) ^{d, e}		260	

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Typical	Maximum	Unit
Maximum Junction-to-Ambient ^{b, f}	R_{thJA}	52	65	$^\circ\text{C}/\text{W}$
Maximum Junction-to-Case (Drain)	R_{thJC}	12.5	16	

Notes:

a. Package limited

b. Surface Mounted on 1" x 1" FR4 board.

c. $t = 5$ s.d. See Solder Profile (<http://www.vishay.com/ppg?73257>). The PowerPAK SC-70 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.

e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.

f. Maximum under Steady State conditions is $110^\circ\text{C}/\text{W}$.

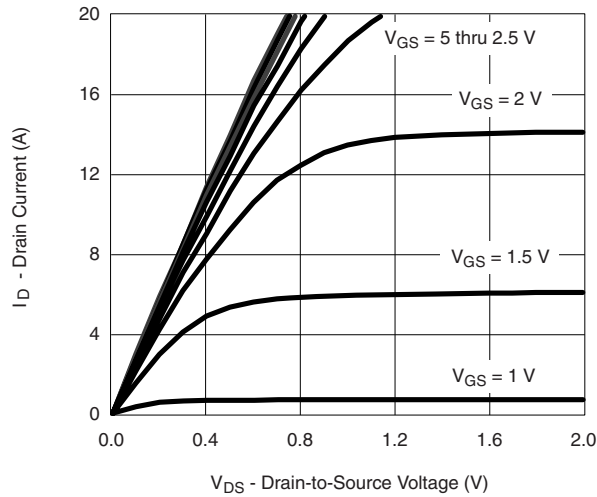
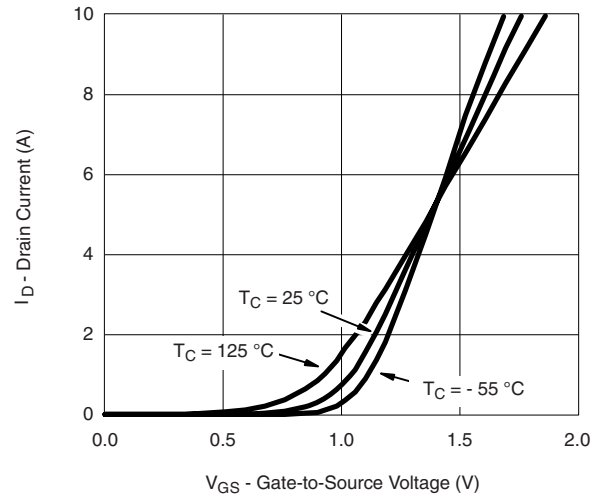
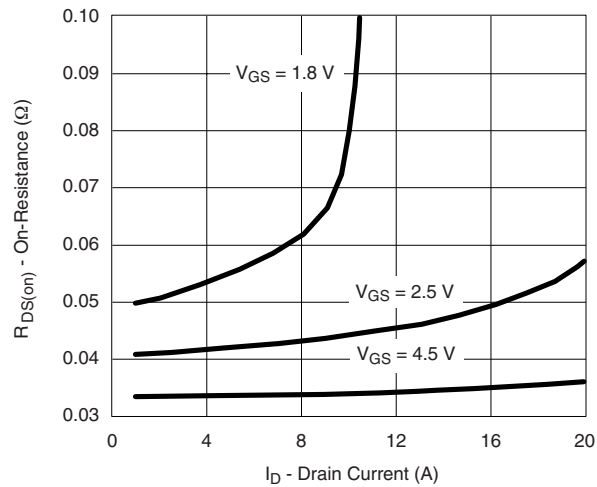
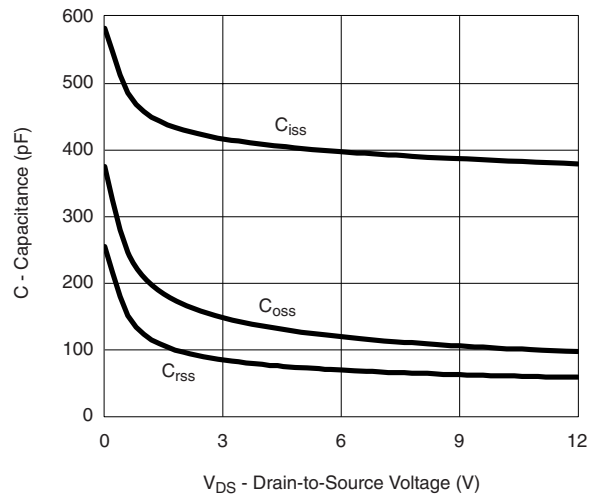
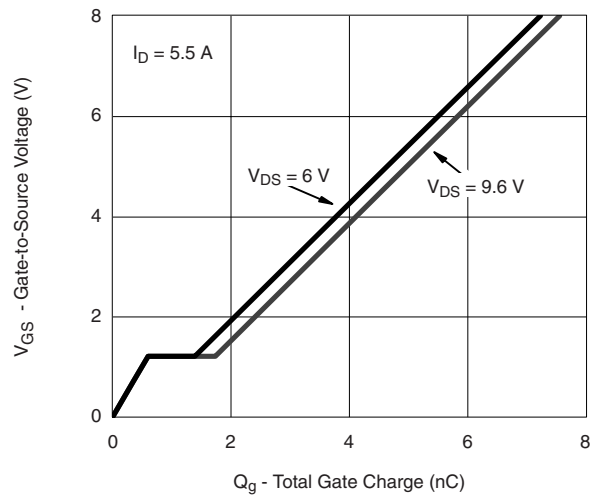
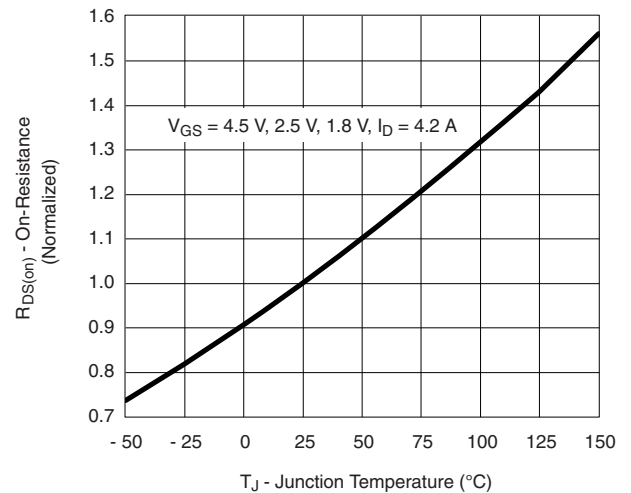
SPECIFICATIONS T _J = 25 °C, unless otherwise noted							
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit	
Static							
Drain-Source Breakdown Voltage	V _{DS}	V _{GS} = 0 V, I _D = 250 μA	12			V	
V _{DS} Temperature Coefficient	ΔV _{DS} /T _J	I _D = 250 μA		12		mV/°C	
V _{GS(th)} Temperature Coefficient	ΔV _{GS(th)} /T _J			- 2.8			
Gate-Source Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.4		1.0	V	
Gate-Source Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ± 8 V			± 100	ns	
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 12 V, V _{GS} = 0 V			- 1	μA	
		V _{DS} = 12 V, V _{GS} = 0 V, T _J = 55 °C			- 10		
On-State Drain Current ^a	I _{D(on)}	V _{DS} ≤ 5 V, V _{GS} = 4.5 V	- 20			A	
Drain-Source On-State Resistance ^a	R _{DS(on)}	V _{GS} = 4.5 V, I _D = 4.2 A		0.033	0.040	Ω	
		V _{GS} = 2.5 V, I _D = 3.8 A		0.039	0.048		
		V _{GS} = 1.8 V, I _D = 1.6 A		0.051	0.063		
Forward Transconductance ^a	g _{fs}	V _{DS} = 6 V, I _D = 4.2 A		13		S	
Dynamic ^b							
Input Capacitance	C _{iss}	V _{DS} = 6 V, V _{GS} = 0 V, f = 1 MHz		400		pF	
Output Capacitance	C _{oss}			120			
Reverse Transfer Capacitance	C _{rss}			70			
Total Gate Charge	Q _g	V _{DS} = 6 V, V _{GS} = 8 V, I _D = 5.5 A		7.5	11.5	nC	
Gate-Source Charge	Q _{gs}	V _{DS} = 6 V, V _{GS} = 4.5 V, I _D = 5.5 A		4.5	6.8		
Gate-Drain Charge	Q _{gd}			0.6			
Gate Resistance	R _g			0.8			
Turn-on Delay Time	t _{d(on)}	f = 1 MHz		2.5		Ω	
Rise Time	t _r		V _{DD} = 6 V, R _L = 1.4 Ω I _D ≅ 4.4 A, V _{GEN} = 4.5 V, R _g = 1 Ω		5	10	ns
Turn-Off Delay Time	t _{d(off)}				15	25	
Fall Time	t _f				35	55	
Turn-on Delay Time	t _{d(on)}	V _{DD} = 6 V, R _L = 1.6 Ω I _D ≅ 4.4 A, V _{GEN} = 8 V, R _g = 1 Ω			15	25	
Rise Time	t _r			5	10		
Turn-Off Delay Time	t _{d(off)}			10	15		
Fall Time	t _f			15	25		
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			4.5	A	
Pulse Diode Forward Current	I _{SM}				20		
Body Diode Voltage	V _{SD}	I _S = 4.4 A, V _{GS} = 0 V		0.8	1.2	V	
Body Diode Reverse Recovery Time	t _{rr}	I _F = 4.4 A, di/dt = 100 A/μs, T _J = 25 °C		15	30	ns	
Body Diode Reverse Recovery Charge	Q _{rr}			8	20	nC	
Reverse Recovery Fall Time	t _a			8.5		ns	
Reverse Recovery Rise Time	t _b			6.5			

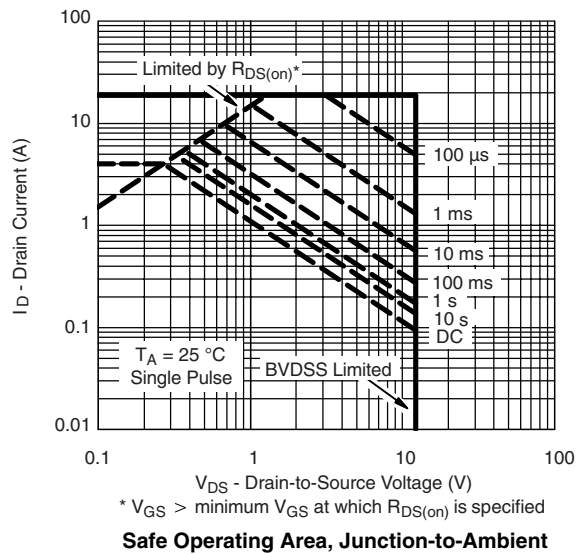
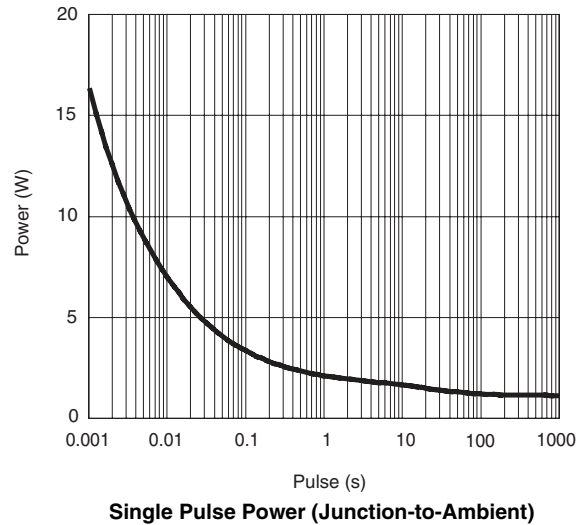
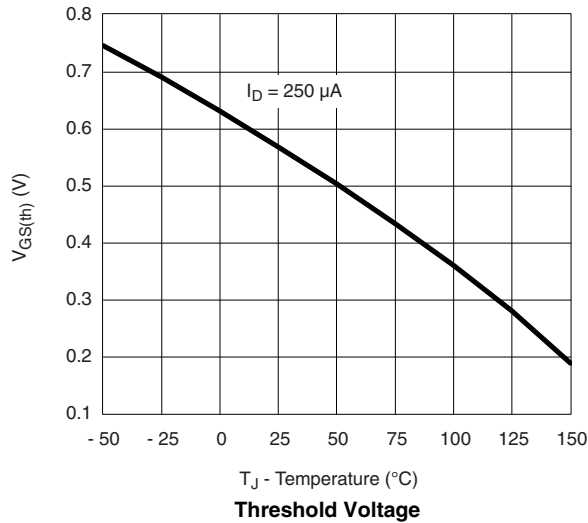
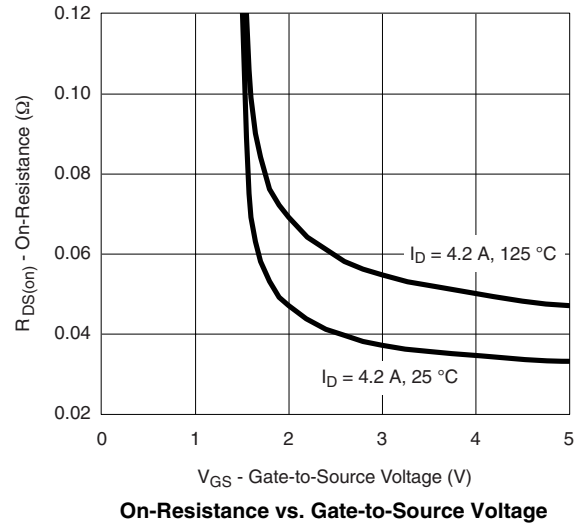
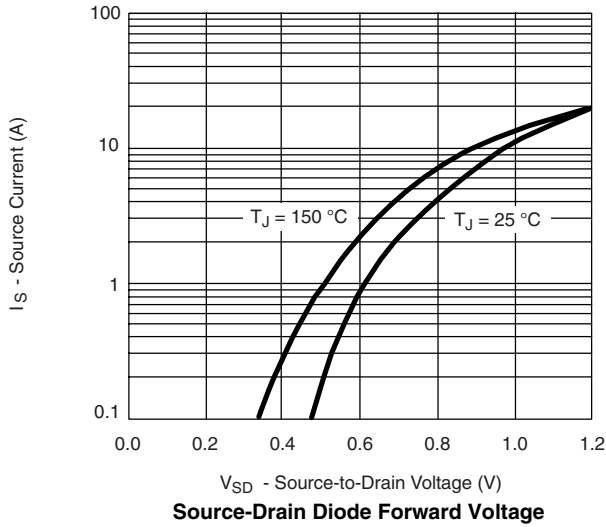
Notes:

a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$

b. Guaranteed by design, not subject to production testing.

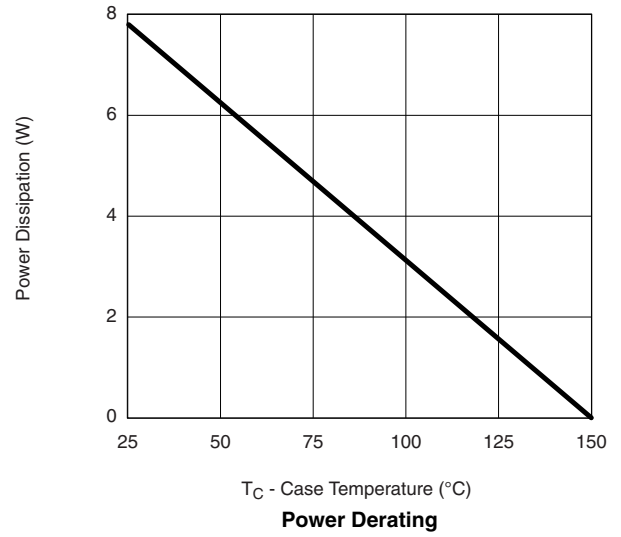
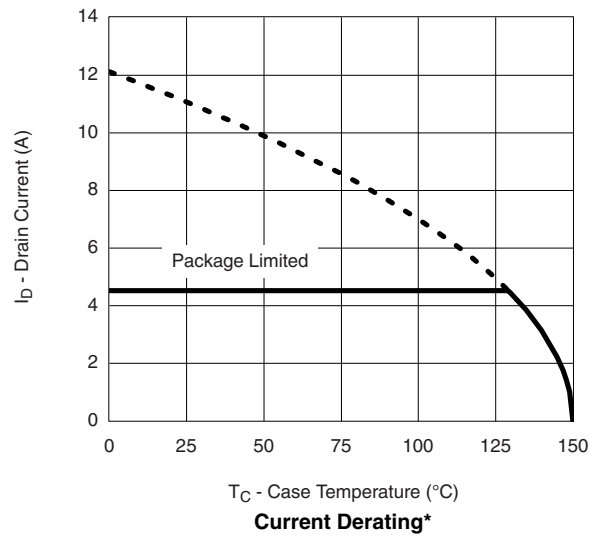
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted**Output Characteristics****Transfer Characteristics****On-Resistance vs. Drain Current and Gate Voltage****Capacitance****Gate Charge****On-Resistance vs. Junction Temperature**

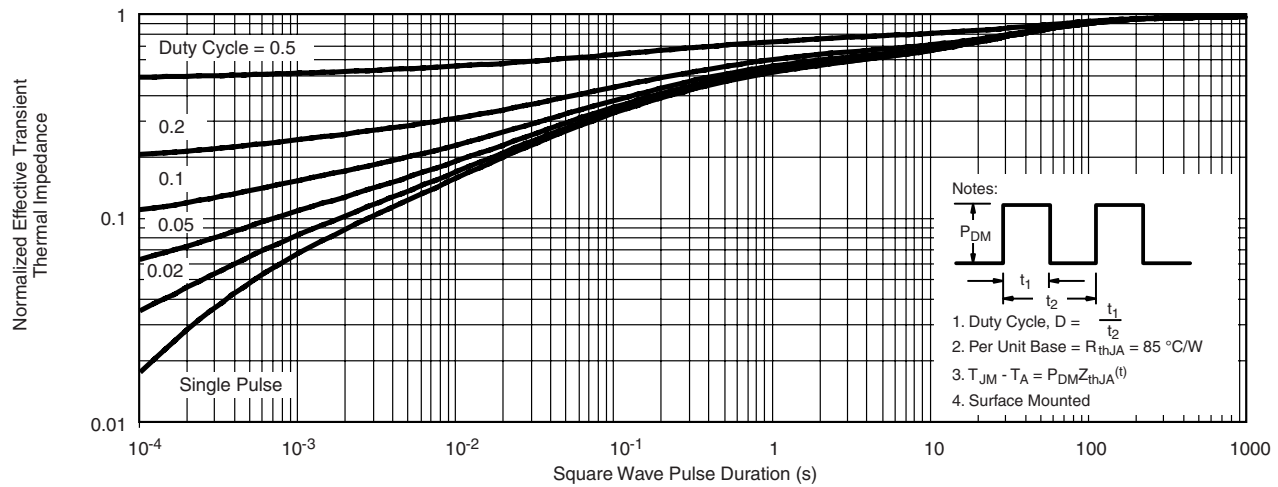
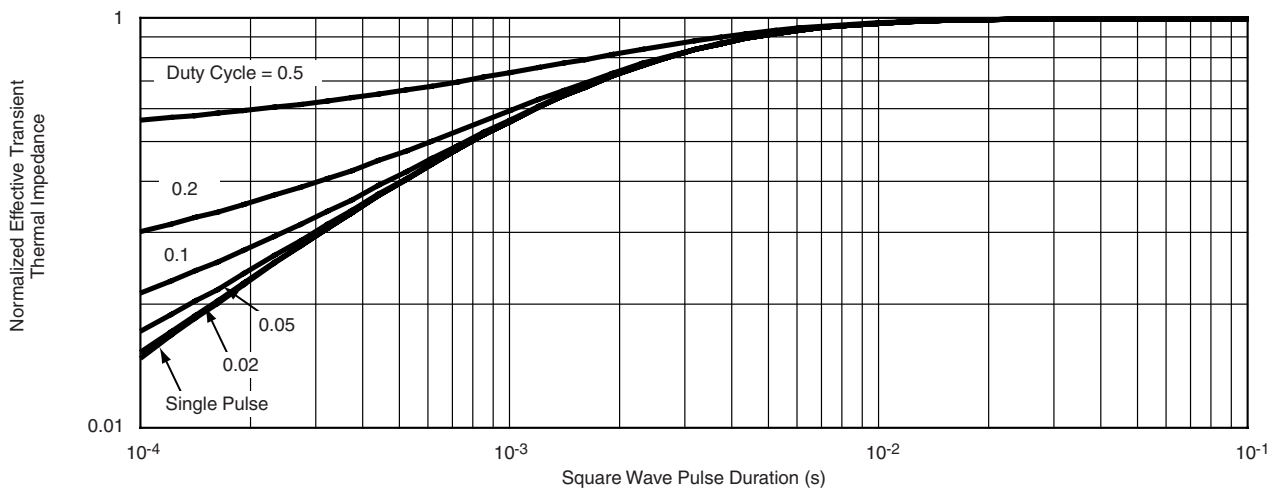
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



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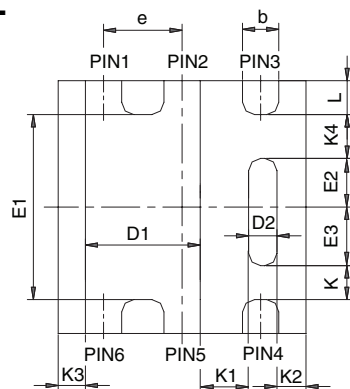
* The power dissipation P_D is based on $T_{J(max)} = 150$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted**Normalized Thermal Transient Impedance, Junction-to-Ambient****Normalized Thermal Transient Impedance, Junction-to-Foot**

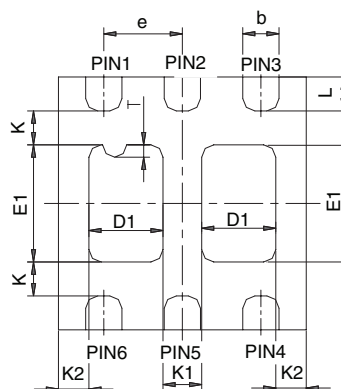
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg74953>.



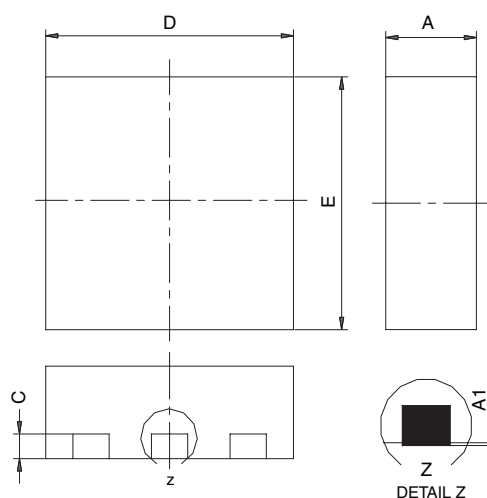
PowerPAK® SC70-6L



BACKSIDE VIEW OF SINGLE



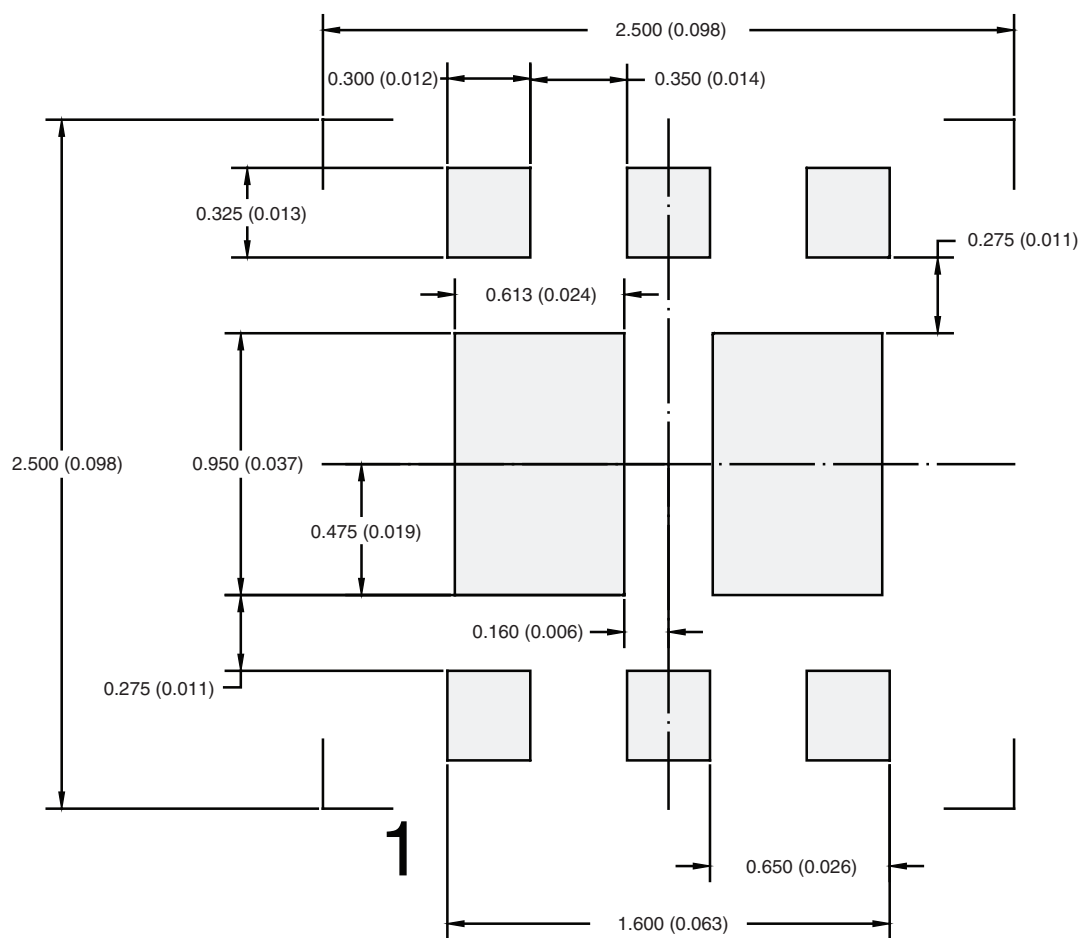
BACKSIDE VIEW OF DUAL



- Notes:
1. All dimensions are in millimeters
 2. Package outline exclusive of mold flash and metal burr
 3. Package outline inclusive of plating

DIM	SINGLE PAD						DUAL PAD					
	MILLIMETERS			INCHES			MILLIMETERS			INCHES		
	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max	Min	Nom	Max
A	0.675	0.75	0.80	0.027	0.030	0.032	0.675	0.75	0.80	0.027	0.030	0.032
A1	0	-	0.05	0	-	0.002	0	-	0.05	0	-	0.002
b	0.23	0.30	0.38	0.009	0.012	0.015	0.23	0.30	0.38	0.009	0.012	0.015
C	0.15	0.20	0.25	0.006	0.008	0.010	0.15	0.20	0.25	0.006	0.008	0.010
D	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
D1	0.85	0.95	1.05	0.033	0.037	0.041	0.513	0.613	0.713	0.020	0.024	0.028
D2	0.135	0.235	0.335	0.005	0.009	0.013						
E	1.98	2.05	2.15	0.078	0.081	0.085	1.98	2.05	2.15	0.078	0.081	0.085
E1	1.40	1.50	1.60	0.055	0.059	0.063	0.85	0.95	1.05	0.033	0.037	0.041
E2	0.345	0.395	0.445	0.014	0.016	0.018						
E3	0.425	0.475	0.525	0.017	0.019	0.021						
e	0.65 BSC			0.026 BSC			0.65 BSC			0.026 BSC		
K	0.275 TYP			0.011 TYP			0.275 TYP			0.011 TYP		
K1	0.400 TYP			0.016 TYP			0.320 TYP			0.013 TYP		
K2	0.240 TYP			0.009 TYP			0.252 TYP			0.010 TYP		
K3	0.225 TYP			0.009 TYP								
K4	0.355 TYP			0.014 TYP								
L	0.175	0.275	0.375	0.007	0.011	0.015	0.175	0.275	0.375	0.007	0.011	0.015
T							0.05	0.10	0.15	0.002	0.004	0.006
ECN: C-07431 – Rev. C, 06-Aug-07												
DWG: 5934												

RECOMMENDED PAD LAYOUT FOR PowerPAK® SC70-6L Dual



Dimensions in mm (inches)



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