

BLF6G10S-45

Power LDMOS transistor

Rev. 4 — 11 March 2013

Product data sheet

1. Product profile

1.1 General description

45 W LDMOS power transistor for base station applications at frequencies from 700 MHz to 1000 MHz.

Table 1. Typical performance

RF performance at $T_{case} = 25\text{ °C}$ in a common source class-AB production test circuit.

Mode of operation	f (MHz)	V _{DS} (V)	P _{L(AV)} (W)	G _p (dB)	η _D (%)	ACPR (dBc)
2-carrier W-CDMA	920 to 960	28	1.0	23	8	-48.5 ^[1]

[1] Test signal: 3GPP; test model 1; 64 DPCH; PAR = 7.5 dB at 0.01 % probability on CCDF per carrier; carrier spacing 5 MHz.

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Therefore care should be taken during transport and handling.

1.2 Features and benefits

- Typical 2-carrier W-CDMA performance at frequencies of 920 MHz and 960 MHz, a supply voltage of 28 V and an I_{DQ} of 350 mA:
 - ◆ Average output power = 1.0 W
 - ◆ Gain = 23 dB
 - ◆ Efficiency = 8 %
 - ◆ ACPR = -48.5 dBc
- Easy power control
- Integrated ESD protection
- Excellent ruggedness
- High efficiency
- Excellent thermal stability
- Designed for broadband operation (700 MHz to 1000 MHz)
- Internally matched for ease of use
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

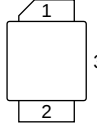
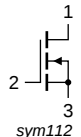


1.3 Applications

- RF power amplifiers for W-CDMA base stations and multi carrier applications in the 700 MHz to 1000 MHz frequency range.

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Symbol
1	drain		
2	gate		
3	source		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
BLF6G10S-45	-	ceramic earless flanged package; 2 leads	SOT608B

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-0.5	+13	V
I_D	drain current		-	13	A
T_{stg}	storage temperature		-65	+150	°C
T_j	junction temperature		-	225	°C

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-case)}$	thermal resistance from junction to case	$T_{case} = 80\text{ °C};$ $P_L = 12.5\text{ W}$	1.7	K/W

6. Characteristics

Table 6. Characteristics

$T_j = 25\text{ }^{\circ}\text{C}$ per section; unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.5\text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$V_{DS} = 10\text{ V}; I_D = 72\text{ mA}$	1.35	1.9	2.35	V
V_{GSq}	gate-source quiescent voltage	$V_{DS} = 28\text{ V}; I_D = 430\text{ mA}$	1.7	2.15	2.7	V
I_{DSS}	drain leakage current	$V_{GS} = 0\text{ V}; V_{DS} = 28\text{ V}$	-	-	1.4	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; V_{DS} = 10\text{ V}$	-	12.5	-	A
I_{GSS}	gate leakage current	$V_{GS} = 11\text{ V}; V_{DS} = 0\text{ V}$	-	-	140	nA
g_{fs}	forward transconductance	$V_{DS} = 10\text{ V}; I_D = 3.6\text{ A}$	-	5	-	S
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75\text{ V}; I_D = 2.52\text{ A}$	-	0.2	-	Ω

7. Application information

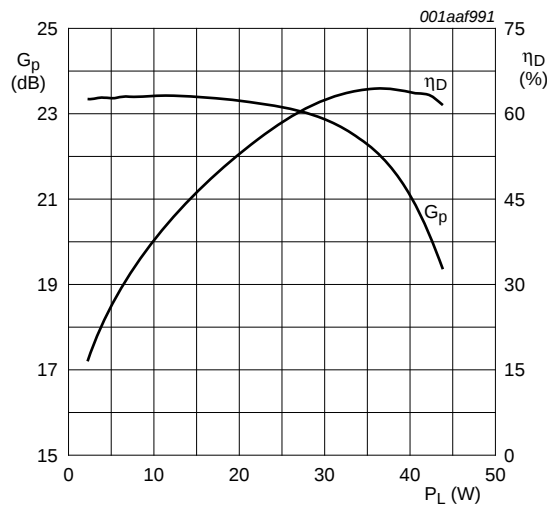
Table 7. Application information

Mode of operation: 2-carrier W-CDMA; PAR 7.5 dB at 0.01 % probability on CCDF; 3GPP test model 1; 1-64 PDPCH; $f_1 = 922.5\text{ MHz}$; $f_2 = 927.5\text{ MHz}$; $f_3 = 952.5\text{ MHz}$; $f_4 = 957.5\text{ MHz}$; RF performance at $V_{DS} = 28\text{ V}$; $I_{Dq} = 350\text{ mA}$; $T_{case} = 25\text{ }^{\circ}\text{C}$; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	$P_{L(AV)} = 1.0\text{ W}$	21.8	23	24.5	dB
RL_{in}	input return loss	$P_{L(AV)} = 1.0\text{ W}$	5.5	9	-	dB
η_D	drain efficiency	$P_{L(AV)} = 1.0\text{ W}$	7	8	-	%
ACPR	adjacent channel power ratio	$P_{L(AV)} = 1.0\text{ W}$	-	-48.5	-45.5	dBc

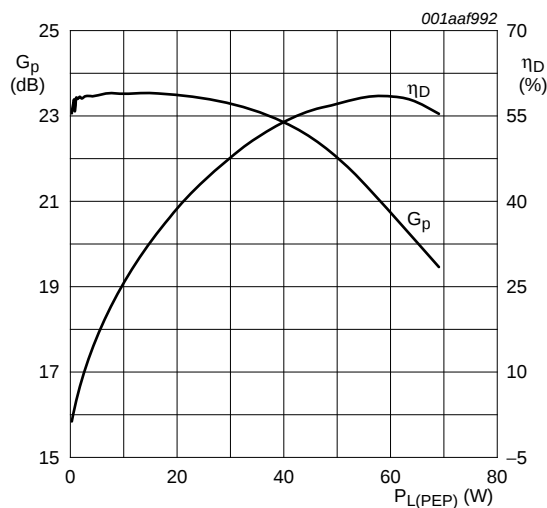
7.1 Ruggedness in class-AB operation

The BLF6G10S-45 is capable of withstanding a load mismatch corresponding to $VSWR = 10 : 1$ through all phases under the following conditions: $V_{DS} = 28\text{ V}$; $I_{Dq} = 350\text{ mA}$; $P_L = 35\text{ W (CW)}$; $f = 960\text{ MHz}$.



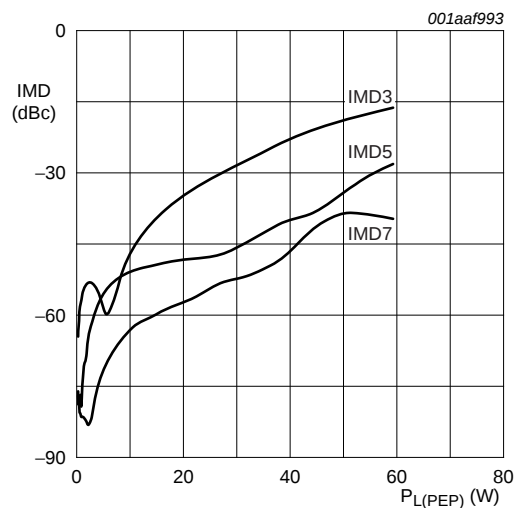
$V_{DS} = 28\text{ V}$; $I_{DQ} = 350\text{ mA}$; $f = 960\text{ MHz}$.

Fig 1. One-tone CW power gain and drain efficiency as functions of load power; typical values



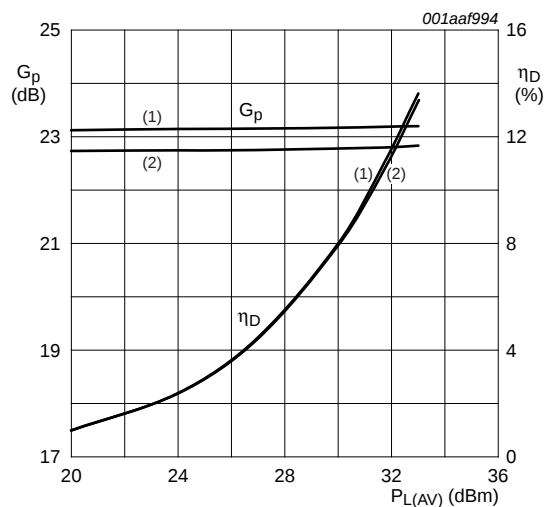
$V_{DS} = 28\text{ V}$; $I_{DQ} = 350\text{ mA}$; $f_1 = 960\text{ MHz}$;
 $f_2 = 960.1\text{ MHz}$.

Fig 2. Two-tone CW power gain and drain efficiency as functions of peak envelope load power; typical values



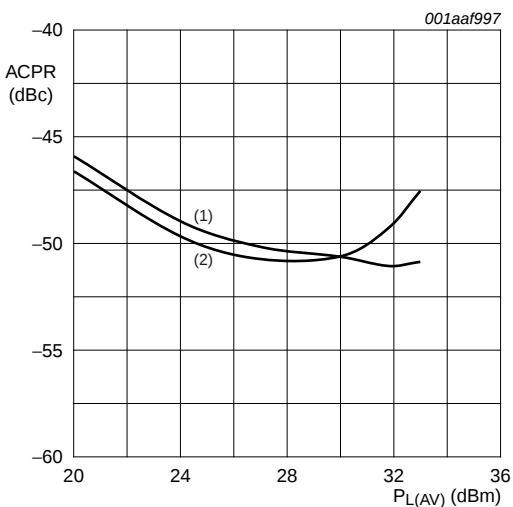
$V_{DS} = 28\text{ V}$; $I_{DQ} = 350\text{ mA}$; $f_1 = 960\text{ MHz}$;
 $f_2 = 960.1\text{ MHz}$.

Fig 3. Intermodulation distortion as a function of peak envelope load power; typical values



$V_{DS} = 28$ V; $I_{DQ} = 350$ mA; $f_1 = 952.5$ MHz;
 $f_2 = 957.5$ MHz; carrier spacing 5 MHz.
(1) $f = 955$ MHz.
(2) $f = 925$ MHz.

Fig 4. 2-carrier W-CDMA power gain and drain efficiency as functions of average load power; typical values



$V_{DS} = 28$ V; $I_{DQ} = 350$ mA; carrier spacing 5 MHz.
(1) $f = 955$ MHz.
(2) $f = 925$ MHz.

Fig 5. 2-carrier W-CDMA adjacent channel power ratio as function of average load power; typical values

8. Test information

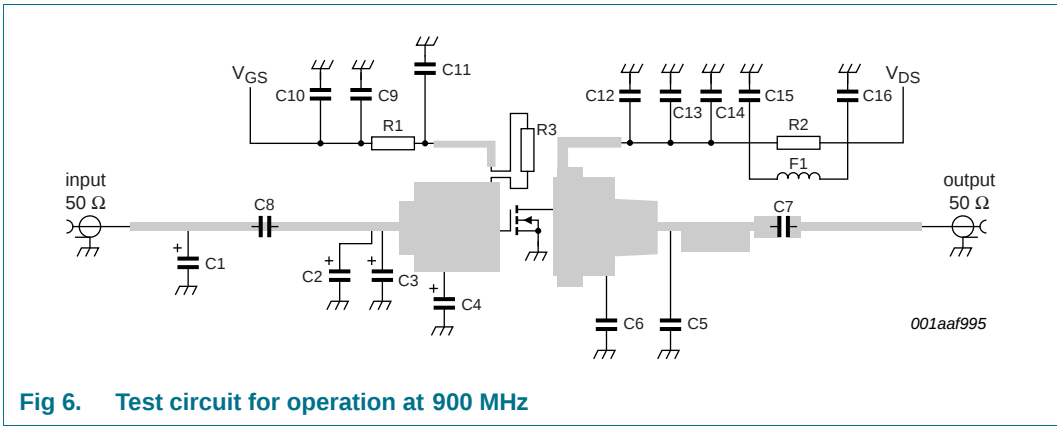


Fig 6. Test circuit for operation at 900 MHz

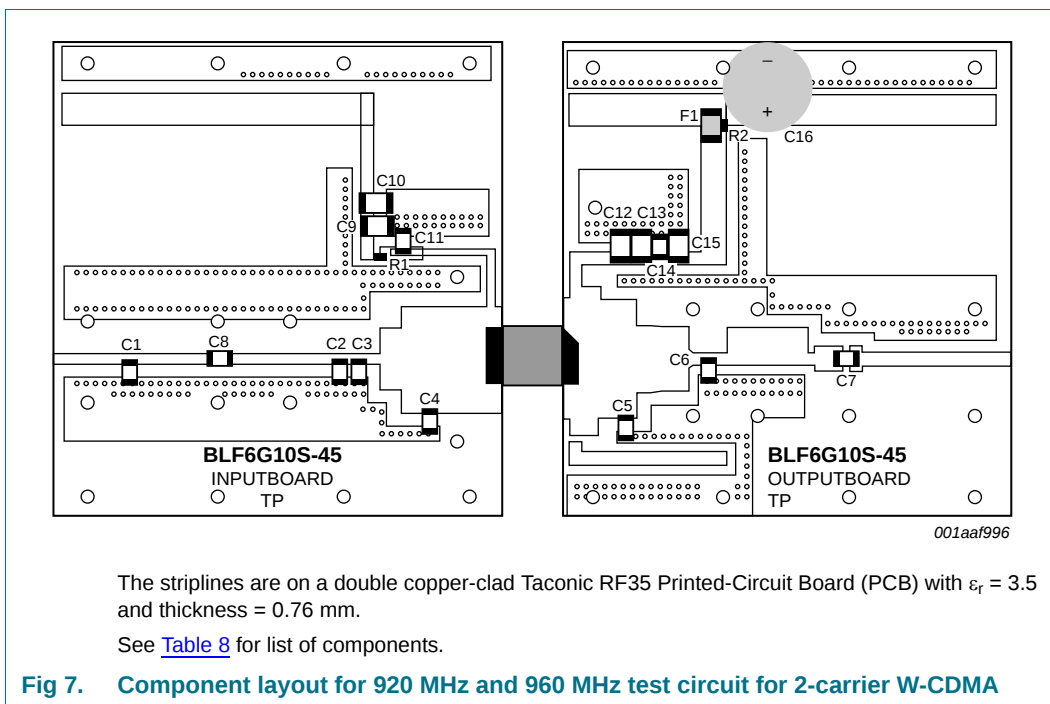


Table 8. List of components (see [Figure 6](#) and [Figure 7](#)).

All capacitors should be soldered vertically.

Component	Description	Value	Remarks
C1	multilayer ceramic chip capacitor	3.0 pF	[1]
C2	multilayer ceramic chip capacitor	1 pF	[1]
C3	multilayer ceramic chip capacitor	6.2 pF	[1]
C4	multilayer ceramic chip capacitor	1.8 pF	[1]
C5	multilayer ceramic chip capacitor	1.0 pF	[1]
C6	multilayer ceramic chip capacitor	6.8 pF	[1]
C7	multilayer ceramic chip capacitor	6.8 pF	[1]
C8, C11, C14	multilayer ceramic chip capacitor	68 pF	[1]
C9, C10, C12, C13	multilayer ceramic chip capacitor	330 nF; 50 V	[2]
C15	multilayer ceramic chip capacitor	4.5 μ F; 50 V	[2]
C16	Electrolytic capacitor	220 μ F	
F1	Ferrite SMD bead	-	Ferroxcube BDS 3/3/8.9-4S2 or equivalent
Q3	BLF6G10S-45	-	
R1	SMD resistor	4.7 Ω ; 0.1 W	
R2	SMD resistor	6.8 Ω ; 0.1 W	

[1] American Technical Ceramics type 100B or capacitor of same quality.

[2] TDK or capacitor of same quality.

10. Abbreviations

Table 9. Abbreviations

Acronym	Description
3GPP	3rd Generation Partnership Project
CCDF	Complementary Cumulative Distribution Function
CW	Continuous Waveform
DPCH	Dedicated Physical CHannel
LDMOS	Laterally Diffused Metal Oxide Semiconductor
PAR	Peak-to-Average power Ratio
PDPCH	transmission Power of the Dedicated Physical CHannel
RF	Radio Frequency
SMD	Surface-Mount Device
VSWR	Voltage Standing-Wave Ratio
W-CDMA	Wideband Code Division Multiple Access

11. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
BLF6G10S-45 v.4	20130311	Product data sheet	-	BLF6G10S-45_3
Modifications:	• Update of Package Outline drawing.			
BLF6G10S-45_3	20100120	Product data sheet	-	BLF6G10S-45_2
BLF6G10S-45_2	20090210	Product data sheet	-	BLF6G10S-45_1
BLF6G10S-45_1	20070223	Preliminary data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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