

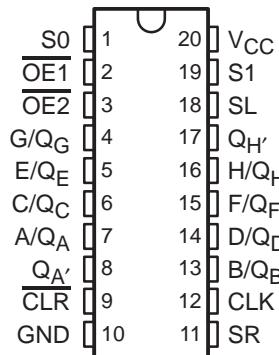
The SN54F299 is obsolete and no longer supplied.

# SN54F299, SN74F299 8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS WITH 3-STATE OUTPUTS

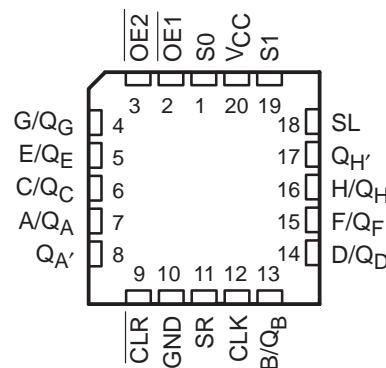
SDFS071B - MARCH 1987 - REVISED APRIL 2004

- Four Modes of Operation:
  - Hold (Store)
  - Shift Right
  - Shift Left
  - Load Data
- Operates With Outputs Enabled or at High Impedance
- 3-State Outputs Drive Bus Lines Directly
- Can Be Cascaded for N-Bit Word Lengths
- Direct Overriding Clear
- Applications:
  - Stacked or Pushdown Registers
  - Buffer Storage
  - Accumulator Registers

SN54F299 . . . J PACKAGE  
SN74F299 . . . DW, N, OR NS PACKAGE  
(TOP VIEW)



SN54F299 . . . FK PACKAGE  
(TOP VIEW)



## description/ordering information

These 8-bit universal shift/storage registers feature multiplexed I/O ports to achieve full 8-bit data handling in a single 20-pin package. Two function-select (S0, S1) inputs and two output-enable ( $\overline{OE}_1$ ,  $\overline{OE}_2$ ) inputs can be used to choose the modes of operation listed in the function table.

Synchronous parallel loading is accomplished by taking both S0 and S1 high. This places the 3-state outputs in a high-impedance state and permits data that is applied on the I/O ports to be clocked into the register. Reading out of the register can be accomplished while the outputs are enabled in any mode. Clearing occurs when the clear (CLR) input is low. Taking either  $\overline{OE}_1$  or  $\overline{OE}_2$  high disables the outputs but has no effect on clearing, shifting, or storage of data.

## ORDERING INFORMATION

TA	PACKAGE <sup>†</sup>		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 70°C	PDIP – N	Tube of 20	SN74F299N	SN74F299N
	SOIC – DW	Tube of 25	SN74F299DW	F299
		Reel of 2000	SN74F299DWR	
	SOP – NS	Reel of 2000	SN74F299NSR	74F299

<sup>†</sup> Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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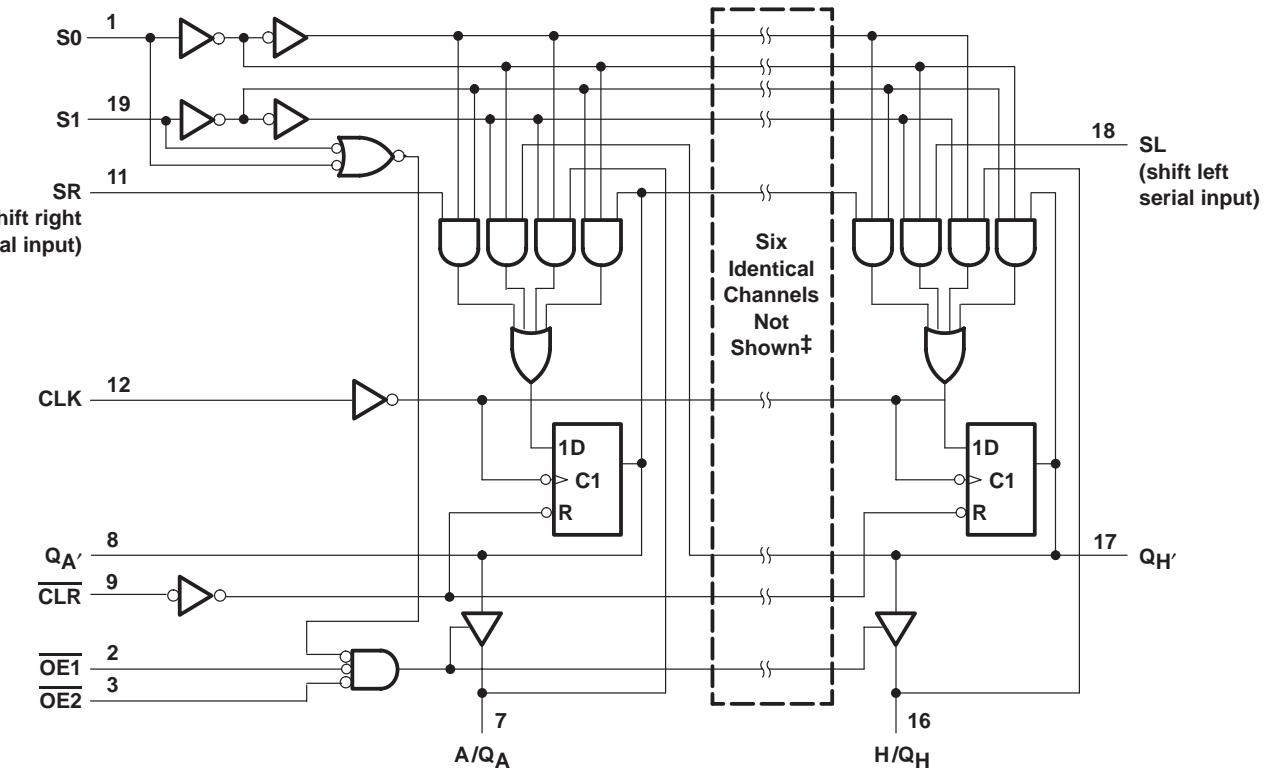
FUNCTION TABLE

MODE	INPUTS							I/O PORTS								OUTPUTS		
	CLR	S1	S0	$\overline{OE1}^\dagger$	$\overline{OE2}^\dagger$	CLK	SL	SR	A/Q <sub>A</sub>	B/Q <sub>B</sub>	C/Q <sub>C</sub>	D/Q <sub>D</sub>	E/Q <sub>E</sub>	F/Q <sub>F</sub>	G/Q <sub>G</sub>	H/Q <sub>H</sub>	Q <sub>A'</sub>	Q <sub>H'</sub>
Clear	L	X	L	L	X	X	X		L	L	L	L	L	L	L	L	L	L
	L	L	X	L	L	X	X	X	L	L	L	L	L	L	L	L	L	L
	L	H	H	X	X	X	X	X	X	X	X	X	X	X	X	X	L	L
Hold	H	L	L	L	L	X	X	X	QA <sub>0</sub>	QB <sub>0</sub>	QC <sub>0</sub>	QD <sub>0</sub>	QE <sub>0</sub>	QF <sub>0</sub>	QG <sub>0</sub>	QH <sub>0</sub>	QA <sub>0</sub>	QH <sub>0</sub>
	H	X	X	L	L	X	X	X	QA <sub>0</sub>	QB <sub>0</sub>	QC <sub>0</sub>	QD <sub>0</sub>	QE <sub>0</sub>	QF <sub>0</sub>	QG <sub>0</sub>	QH <sub>0</sub>	QA <sub>0</sub>	QH <sub>0</sub>
Shift Right	H	L	H	L	L	$\uparrow$	X	H	H	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	H	Q <sub>Gn</sub>
Shift Left	H	L	H	L	L	$\uparrow$	X	L	L	Q <sub>An</sub>	Q <sub>Bn</sub>	Q <sub>Cn</sub>	Q <sub>Dn</sub>	Q <sub>En</sub>	Q <sub>Fn</sub>	Q <sub>Gn</sub>	L	Q <sub>Gn</sub>
Shift Left	H	H	L	L	L	$\uparrow$	H	X	QB <sub>n</sub>	QC <sub>n</sub>	QD <sub>n</sub>	QE <sub>n</sub>	QF <sub>n</sub>	QG <sub>n</sub>	QH <sub>n</sub>	H	QB <sub>n</sub>	
Load	H	H	H	X	X	$\uparrow$	X	X	a	b	c	d	e	f	g	h	a	h

NOTE: a . . . h = the level of the steady-state input at inputs A through H, respectively. This data is loaded into the flip-flops while the flip-flop outputs are isolated from the I/O terminals.

† When one or both output-enable inputs are high, the eight I/O terminals are disabled to the high-impedance state; however, sequential operation or clearing of the register is not affected.

**logic diagram (positive logic)**



‡ I/O ports not shown: B/Q<sub>B</sub> (13), C/Q<sub>C</sub> (6), D/Q<sub>D</sub> (14), E/Q<sub>E</sub> (5), F/Q<sub>F</sub> (15), and G/Q<sub>G</sub> (4).

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

<sup>†</sup> Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input voltage ratings may be exceeded provided the input current ratings are observed.  
2. The package thermal impedance is calculated in accordance with JESD 51-7.

### **recommended operating conditions (see Note 3)**

		SN54F299			SN74F299			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V <sub>CC</sub>	Supply voltage	4.5	5	5.5	4.5	5	5.5	V
V <sub>IH</sub>	High-level input voltage		2		2			V
V <sub>IL</sub>	Low-level input voltage			0.8			0.8	V
I <sub>IK</sub>	Input clamp current			-18			-18	mA
I <sub>OH</sub>	High-level output current	Q <sub>A'</sub> or Q <sub>H'</sub>		-1			-1	mA
		Q <sub>A</sub> thru Q <sub>H</sub>		-3			-3	
I <sub>OL</sub>	Low-level output current	Q <sub>A'</sub> or Q <sub>H'</sub>		20		20		mA
		Q <sub>A</sub> thru Q <sub>H</sub>		20		24		
T <sub>A</sub>	Operating free-air temperature	-55		125	0		70	°C

NOTE 3: All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

**SN54F299, SN74F299**  
**8-BIT UNIVERSAL SHIFT/STORAGE REGISTERS**  
**WITH 3-STATE OUTPUTS**

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	SN54F299			SN74F299			UNIT
		MIN	TYP†	MAX	MIN	TYP†	MAX	
V <sub>IK</sub>	V <sub>CC</sub> = 4.5 V, I <sub>I</sub> = -18 mA			-1.2			-1.2	V
V <sub>OH</sub>	Q <sub>A</sub> ' or Q <sub>H</sub> ' V <sub>CC</sub> = 4.5 V Q <sub>A</sub> thru Q <sub>H</sub>	I <sub>OH</sub> = -1 mA	2.5	3.4	2.5	3.4		V
		I <sub>OH</sub> = -1 mA	2.5	3.4	2.5	3.4		
		I <sub>OH</sub> = -3 mA	2.4	3.3	2.4	3.3		
Any output	V <sub>CC</sub> = 4.75 V, I <sub>OH</sub> = -1 mA to -3 mA				2.7			
V <sub>OL</sub>	Q <sub>A</sub> ' or Q <sub>H</sub> ' V <sub>CC</sub> = 4.5 V Q <sub>A</sub> thru Q <sub>H</sub>	I <sub>OL</sub> = 20 mA	0.3	0.5	0.3	0.5		V
		I <sub>OL</sub> = 20 mA	0.3	0.5				
		I <sub>OL</sub> = 24 mA			0.35	0.5		
I <sub>I</sub>	A thru H V <sub>CC</sub> = 5.5 V	V <sub>I</sub> = 5.5 V		1		1		mA
		V <sub>I</sub> = 7 V		0.1		0.1		
I <sub>IH</sub> ‡	A thru H V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 2.7 V		70		70			µA
			20		20			
I <sub>IL</sub> ‡	A thru H S0 or S1 V <sub>CC</sub> = 5.5 V, V <sub>I</sub> = 0.5 V		-0.65		-0.65			mA
			-1.2		-1.2			
			-0.6		-0.6			
I <sub>OS</sub> §	V <sub>CC</sub> = 5.5 V, V <sub>O</sub> = 0		-60	-150	-60	-150		mA
I <sub>CC</sub>	V <sub>CC</sub> = 5.5 V, See Note 4		68	95	68	95		mA

† All typical values are at V<sub>CC</sub> = 5 V, T<sub>A</sub> = 25°C.

‡ For I/O ports (Q<sub>A</sub> thru Q<sub>H</sub>), the parameters I<sub>IH</sub> and I<sub>IL</sub> include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

NOTE 4: I<sub>CC</sub> is measured with OE1, OE2, and CLK at 4.5 V.

timing requirements over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

			V <sub>CC</sub> = 5 V, T <sub>A</sub> = 25°C		SN54F299		SN74F299		UNIT	
			'F299							
			MIN	MAX	MIN	MAX	MIN	MAX		
f <sub>clock</sub>	Clock frequency			70		65		70	MHz	
t <sub>w</sub>	Pulse duration	CLK high or low			7	8	7		ns	
		CLR low			7	8	7			
t <sub>su</sub>	Setup time before CLK↑	S0 or S1	High or low	8.5	9.5	8.5			ns	
		A/Q <sub>A</sub> thru H/Q <sub>H</sub> , SR, or SL	High or low	5.5	6.5	5.5				
t <sub>h</sub>	Hold time after CLK↑	CLR	High	7	13	7			ns	
		S0 or S1	High or low	0	0	0				
		A/Q <sub>A</sub> thru H/Q <sub>H</sub> , SR, or SL	High or low	2	2	2				

¶ Inactive-state setup time also is referred to as recovery time.

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**WITH 3-STATE OUTPUTS**

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switching characteristics (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub> = 5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = 25°C			V <sub>CC</sub> = 4.5 V to 5.5 V, C <sub>L</sub> = 50 pF, R <sub>L</sub> = 500 Ω, T <sub>A</sub> = MIN to MAX <sup>†</sup>			UNIT	
			'F299			SN54F299		SN74F299		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f <sub>max</sub>			70	100		65		70		MHz
t <sub>PLH</sub>	CLK	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.2	6.6	9	2.7	10.5	3.2	10	ns
t <sub>PHL</sub>			2.7	6.1	8.5	2.2	10	2.7	9.5	
t <sub>PLH</sub>	CLK	Q <sub>A</sub> thru Q <sub>H</sub>	3.2	6.6	9	2.7	11	3.2	10	ns
t <sub>PHL</sub>			4.2	8.1	11	3.7	12.5	4.2	12	
t <sub>PHL</sub>	CLR	Q <sub>A</sub> ' or Q <sub>H</sub> '	3.7	7.1	9.5	3.2	11.5	3.7	10.5	ns
		Q <sub>A</sub> thru Q <sub>H</sub>	5.7	10.6	14	5	15.5	5.7	15	
t <sub>PZH</sub>	OE1 or OE2	Q <sub>A</sub> thru Q <sub>H</sub>	2.7	5.6	8	2.2	10.5	2.7	9	ns
t <sub>PZL</sub>			3.2	6.6	10	2.7	12	3.2	11	
t <sub>PHZ</sub>	OE1 or OE2	Q <sub>A</sub> thru Q <sub>H</sub>	1.7	4.1	6	1.7	9	1.7	7	ns
t <sub>PLZ</sub>			1.2	3.6	5.5	1.2	7.5	1.2	6.5	

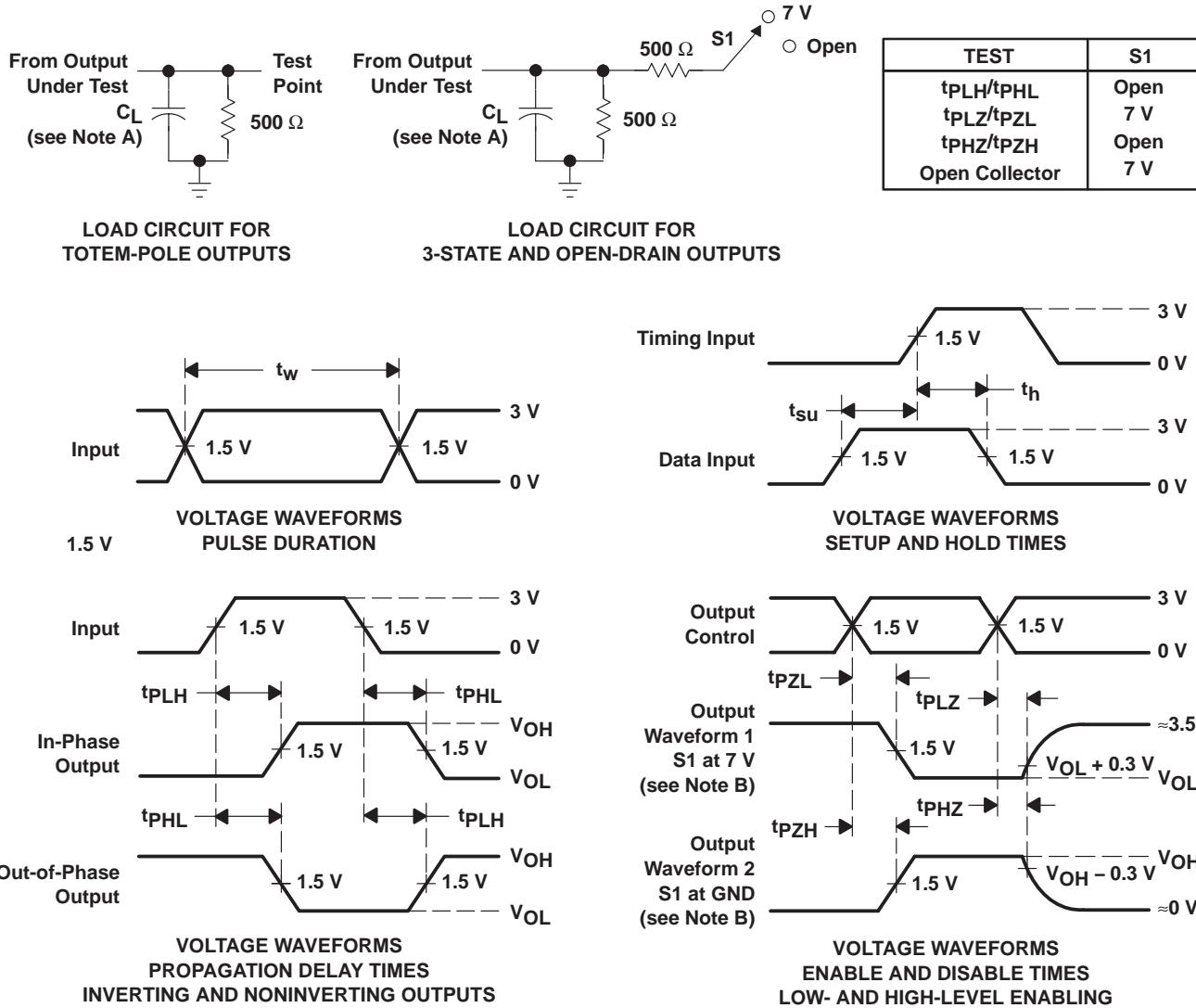
<sup>†</sup> For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

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**PARAMETER MEASUREMENT INFORMATION**



NOTES:

- $C_L$  includes probe and jig capacitance.
- Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- All input pulses are supplied by generators having the following characteristics: PRR  $\leq 1$  MHz,  $Z_O = 50 \Omega$ ,  $t_r \leq 2.5$  ns,  $t_f \leq 2.5$  ns, duty cycle = 50%.
- The outputs are measured one at a time, with one input transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74F299DW	ACTIVE	SOIC	DW	20	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F299	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74F299DWR	ACTIVE	SOIC	DW	20	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	F299	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74F299N	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74F299N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>
SN74F299N3	OBsolete	PDIP	N	20		TBD	Call TI	Call TI	0 to 70		
SN74F299NE4	ACTIVE	PDIP	N	20	20	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type	0 to 70	SN74F299N	<span style="background-color: red; color: white; padding: 2px;">Samples</span>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBsolete:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



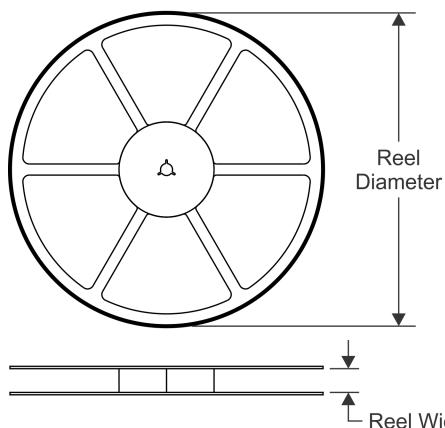
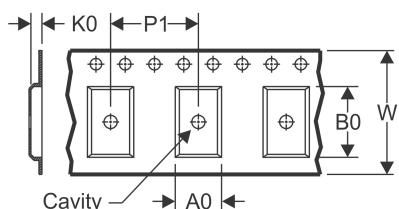
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## PACKAGE OPTION ADDENDUM

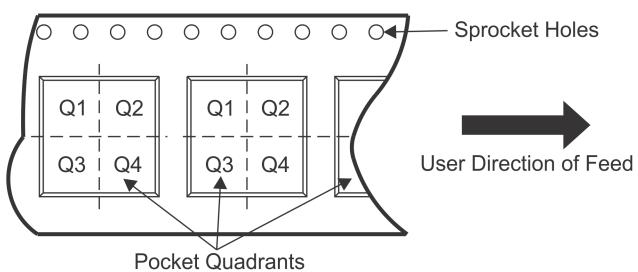
10-Jun-2014

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**TAPE AND REEL INFORMATION**
**REEL DIMENSIONS**

**TAPE DIMENSIONS**


A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74F299DWR	SOIC	DW	20	2000	330.0	24.4	10.8	13.0	2.7	12.0	24.0	Q1

**TAPE AND REEL BOX DIMENSIONS**

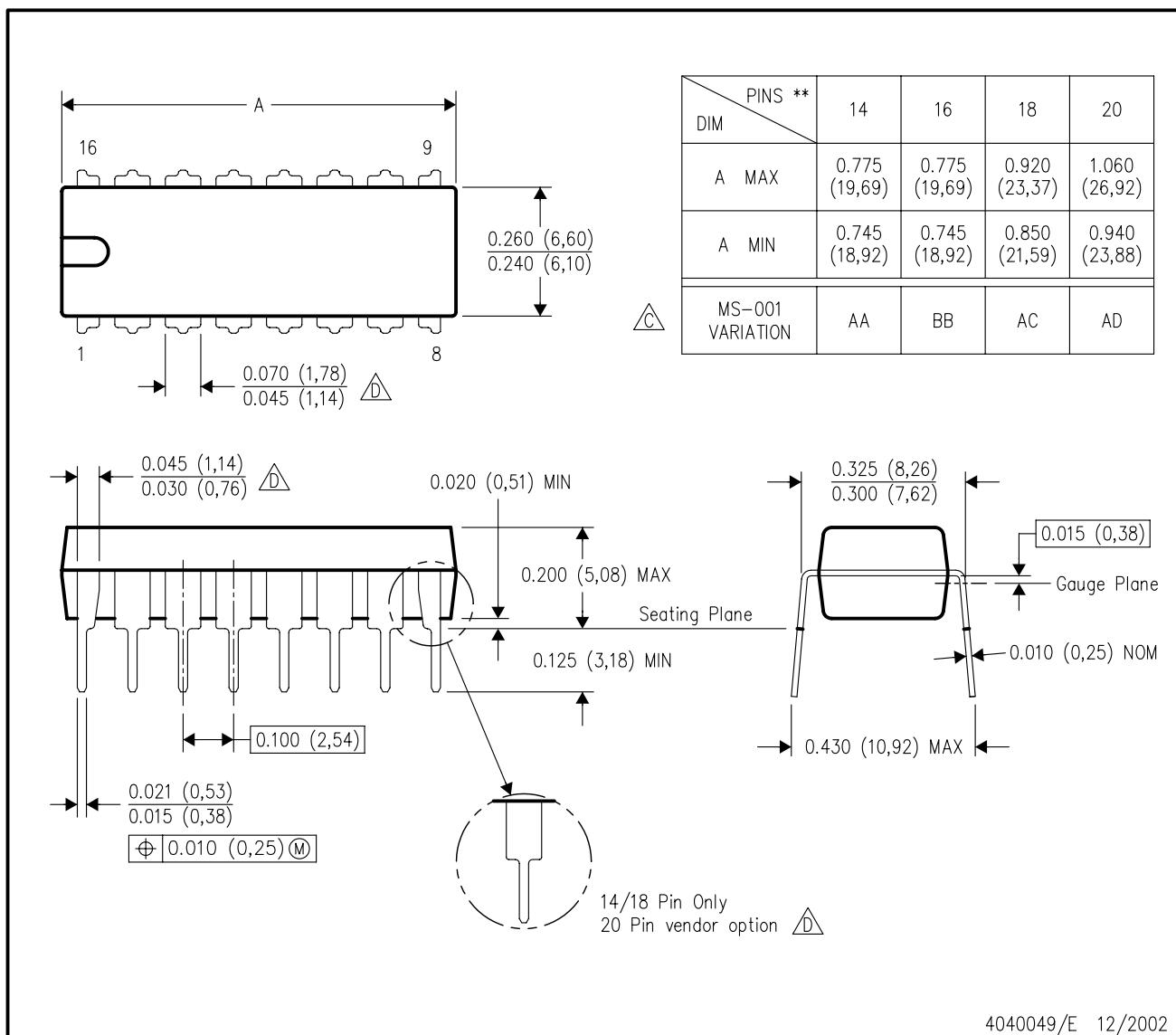
\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74F299DWR	SOIC	DW	20	2000	367.0	367.0	45.0

## N (R-PDIP-T\*\*)

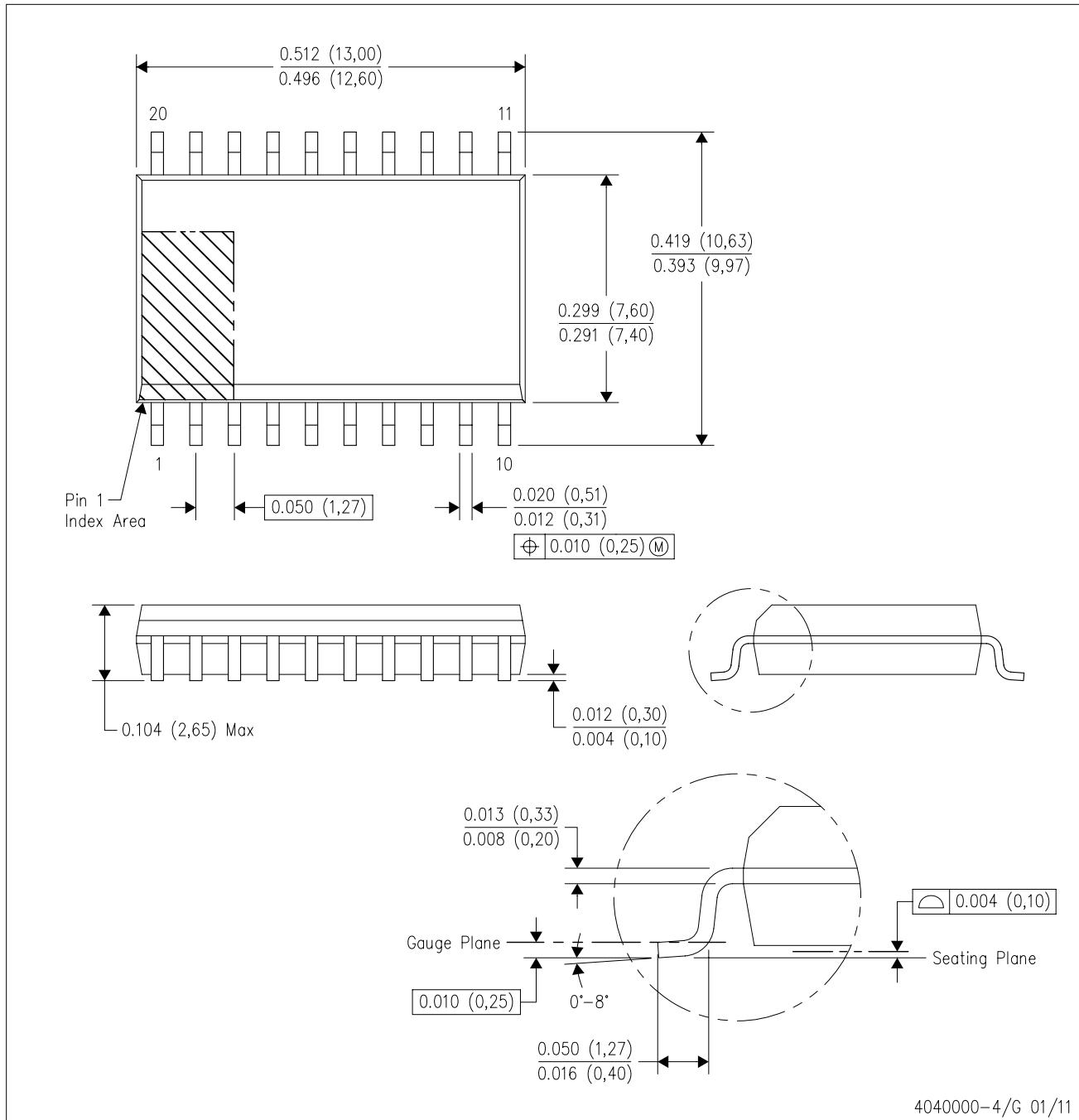
16 PINS SHOWN

## PLASTIC DUAL-IN-LINE PACKAGE



DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

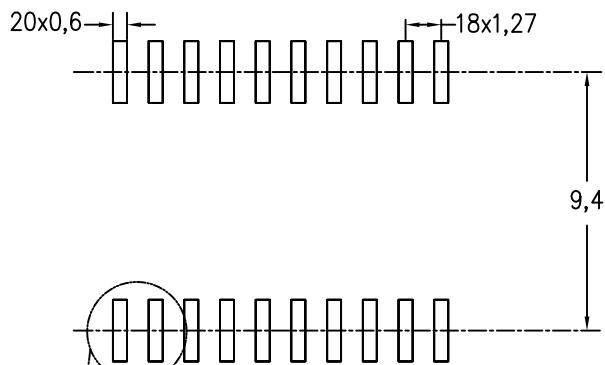
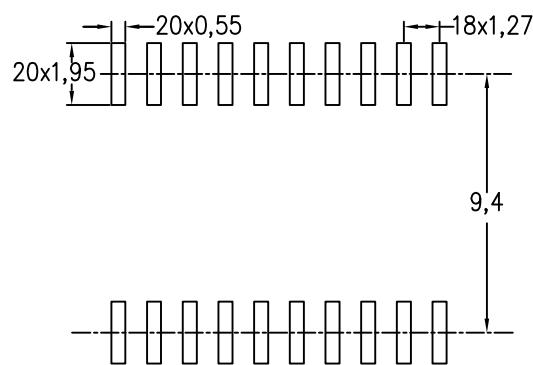


NOTES:

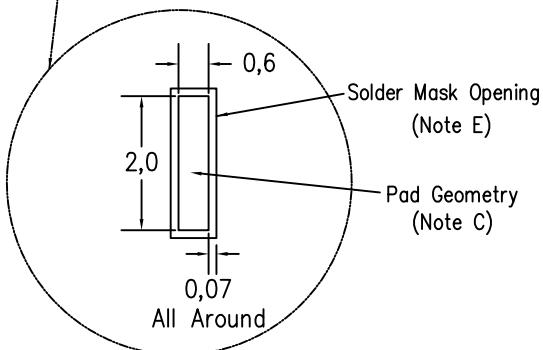
- All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M-1994.
- This drawing is subject to change without notice.
- Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0.15).
- Falls within JEDEC MS-013 variation AC.

DW (R-PDSO-G20)

PLASTIC SMALL OUTLINE

Example Board Layout  
(Note C)Stencil Openings  
(Note D)

Non Solder Mask Define Pad



4209202-4/F 08/13

NOTES:

- All linear dimensions are in millimeters.
- This drawing is subject to change without notice.
- Refer to IPC7351 for alternate board design.
- Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
- Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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