

# TC74HC193AP, TC74HC193AF

## Synchronous Up/Down Binary Counter

The TC74HC193A are high speed CMOS SYNCHRONOUS 4-BIT UP/DOWN COUNTER fabricated with silicon gate C<sup>2</sup>MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

They have a clear input (CLR), a load input ( $\overline{\text{LOAD}}$ ), load data inputs (A~D), two clock inputs (COUNT UP, COUNT DOWN), four count data outputs (QA~QD), and other outputs ( $\overline{\text{CARRY}}$ ,  $\overline{\text{BORROW}}$ ).

CLEAR is active high and forces QA thru QD outputs low independent of the other inputs.

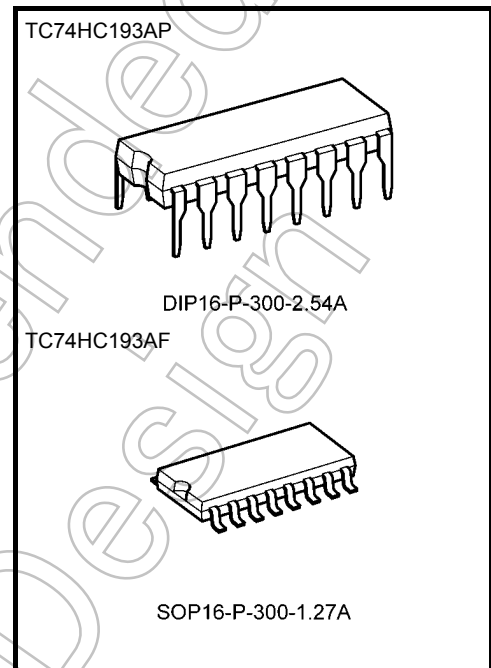
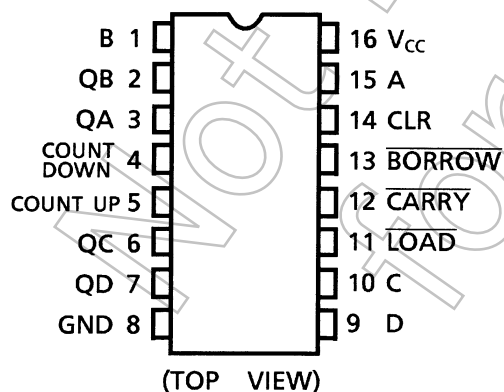
$\overline{\text{CARRY}}$  and  $\overline{\text{BORROW}}$  outputs are provided in order to make a cascade connection without external circuitry.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

### Features

- High speed:  $f_{\text{max}} = 54 \text{ MHz}$  (typ.) at  $V_{\text{CC}} = 5 \text{ V}$
- Low power dissipation:  $I_{\text{CC}} = 4 \mu\text{A}$  (max) at  $T_a = 25^\circ\text{C}$
- High noise immunity:  $V_{\text{NIH}} = V_{\text{NIL}} = 28\% V_{\text{CC}}$  (min)
- Output drive capability: 10 LSTTL loads
- Symmetrical output impedance:  $|I_{\text{OH}}| = I_{\text{OL}} = 4 \text{ mA}$  (min)
- Balanced propagation delays:  $t_{\text{PLH}} \approx t_{\text{PHL}}$
- Wide operating voltage range:  $V_{\text{CC}} (\text{opr}) = 2 \text{ to } 6 \text{ V}$
- Pin and function compatible with 74LS193

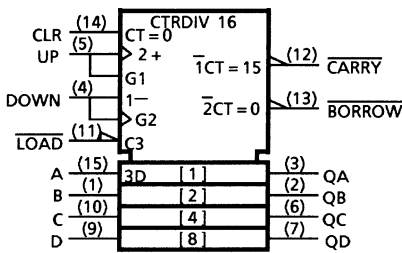
### Pin Assignment



Weight	
DIP16-P-300-2.54A	: 1.00 g (typ.)
SOP16-P-300-1.27A	: 0.18 g (typ.)

Start of commercial production  
1986-05

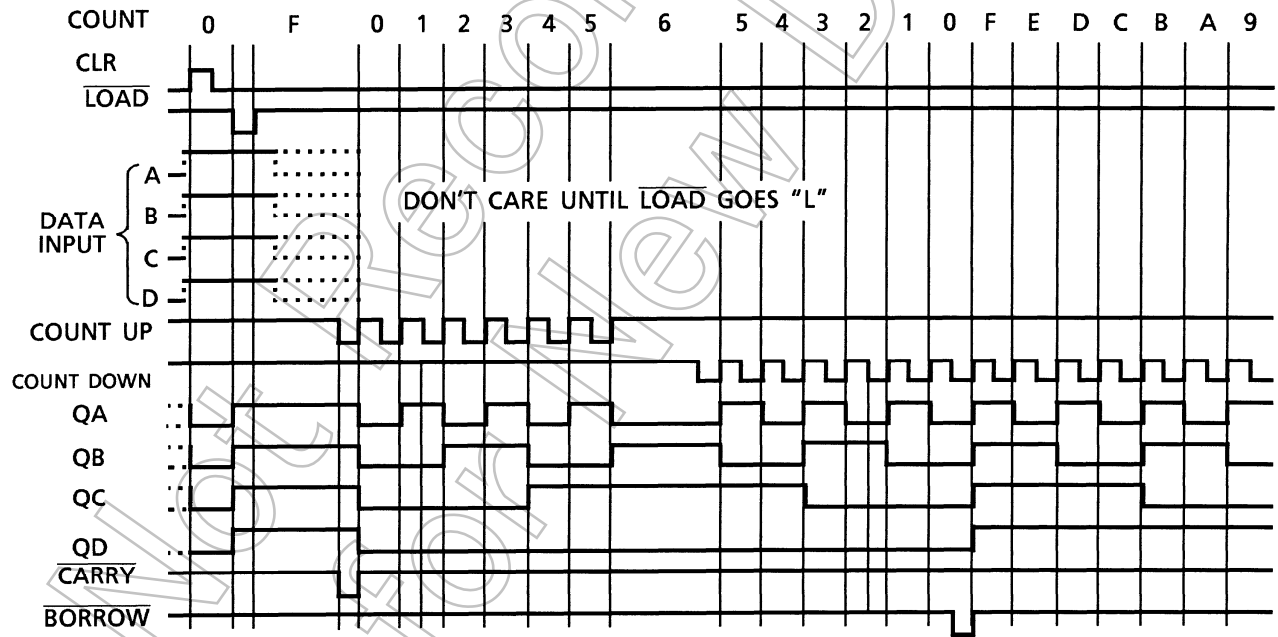
IEC Logic Symbol



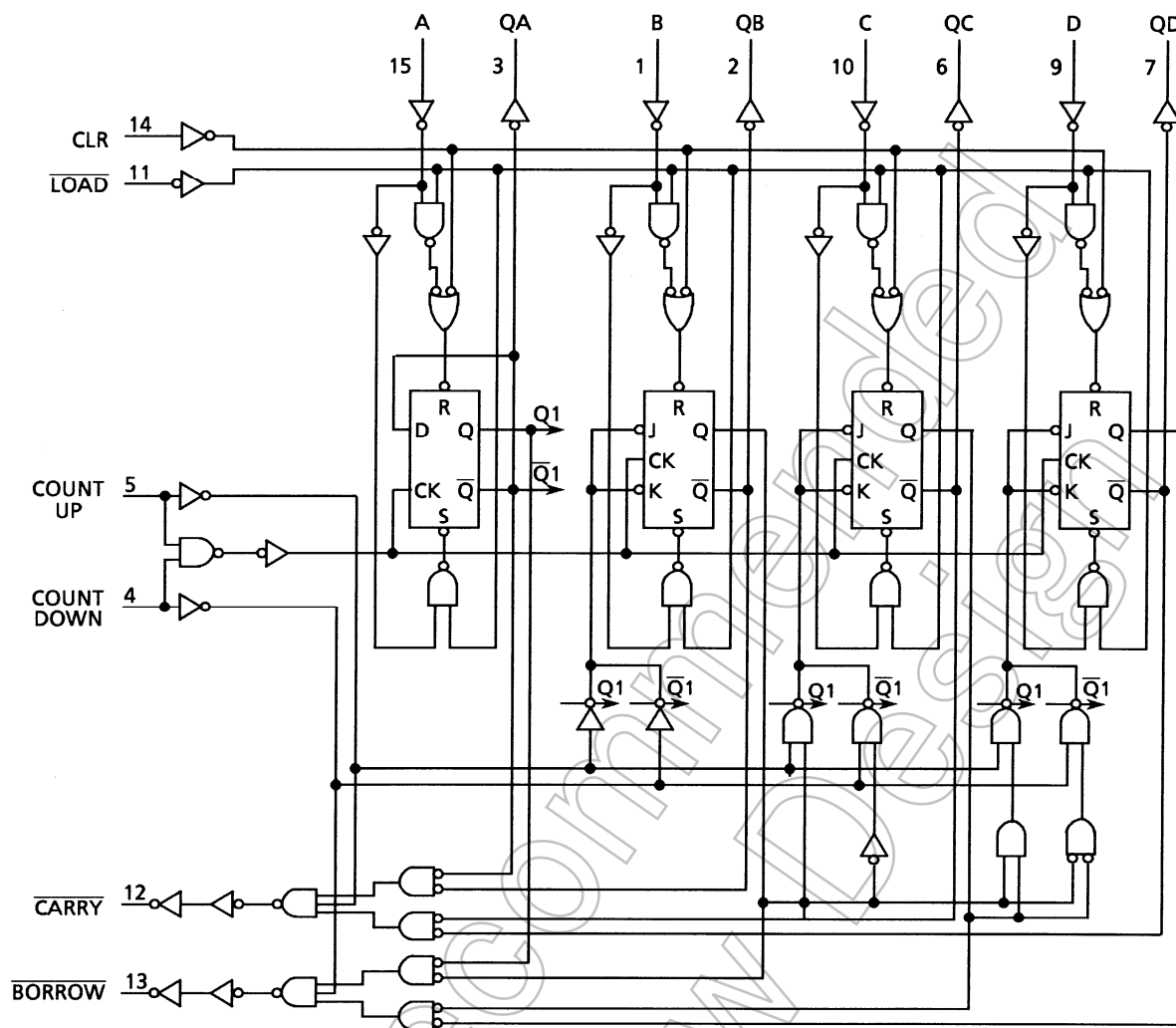
Truth Table

Inputs				Function
Count Up	Count Down	LOAD	CLR	
	H	H	L	Count Up
	H	H	L	No Count
H		H	L	Count Down
H		H	L	No Count
X	X	L	L	Preset
X	X	X	H	Reset

Timing Chart



## System Diagram



## Absolute Maximum Ratings (Note 1)

Characteristics	Symbol	Rating	Unit
Supply voltage range	$V_{CC}$	-0.5 to 7	V
DC input voltage	$V_{IN}$	-0.5 to $V_{CC} + 0.5$	V
DC output voltage	$V_{OUT}$	-0.5 to $V_{CC} + 0.5$	V
Input diode current	$I_{IK}$	$\pm 20$	mA
Output diode current	$I_{OK}$	$\pm 20$	mA
DC output current	$I_{OUT}$	$\pm 25$	mA
DC $V_{CC}$ /ground current	$I_{CC}$	$\pm 50$	mA
Power dissipation	$P_D$	500 (DIP) (Note 2)/180 (SOP)	mW
Storage temperature	$T_{stg}$	-65 to 150	$^{\circ}\text{C}$

Note 1: Exceeding any of the absolute maximum ratings, even briefly, lead to deterioration in IC performance or even destruction.

Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

Note 2: 500 mW in the range of  $T_a = -40$  to  $65^{\circ}\text{C}$ . From  $T_a = 65$  to  $85^{\circ}\text{C}$  a derating factor of  $-10$  mW/ $^{\circ}\text{C}$  shall be applied until 300 mW.

**Operating Ranges (Note)**

Characteristics	Symbol	Rating	Unit
Supply voltage	$V_{CC}$	2 to 6	V
Input voltage	$V_{IN}$	0 to $V_{CC}$	V
Output voltage	$V_{OUT}$	0 to $V_{CC}$	V
Operating temperature	$T_{opr}$	-40 to 85	°C
Input rise and fall time	$t_r, t_f$	0 to 1000 ( $V_{CC} = 2.0$ V) 0 to 500 ( $V_{CC} = 4.5$ V) 0 to 400 ( $V_{CC} = 6.0$ V)	ns

Note: The operating ranges must be maintained to ensure the normal operation of the device.  
Unused inputs must be tied to either  $V_{CC}$  or GND.

**Electrical Characteristics**
**DC Characteristics**

Characteristics	Symbol	Test Condition		Ta = 25°C				Ta = -40 to 85°C		Unit
				VCC (V)	Min	Typ.	Max	Min	Max	
High-level input voltage	VIH	—		2.0 4.5 6.0	1.50 3.15 4.20	— — —	— — —	1.50 3.15 4.20	— — —	V
Low-level input voltage	VIL	—		2.0 4.5 6.0	— — —	— — —	0.50 1.35 1.80	— — —	0.50 1.35 1.80	V
High-level output voltage	VOH	VIN = VIH or VIL	I <sub>OH</sub> = -20 μA	2.0 4.5 6.0	1.9 4.4 5.9	2.0 4.5 6.0	— — —	1.9 4.4 5.9	— — —	V
			I <sub>OH</sub> = -4 mA	4.5	4.18	4.31	—	4.13	—	
			I <sub>OH</sub> = -5.2 mA	6.0	5.68	5.80	—	5.63	—	
Low-level output voltage	VOL	VIN = VIH or VIL	I <sub>OL</sub> = 20 μA	2.0 4.5 6.0	— — —	0.0 0.0 0.0	0.1 0.1 0.1	— — —	0.1 0.1 0.1	V
			I <sub>OL</sub> = 4 mA	4.5	—	0.17	0.26	—	0.33	
			I <sub>OL</sub> = 5.2 mA	6.0	—	0.18	0.26	—	0.33	
Input leakage current	IIN	VIN = VCC or GND		6.0	—	—	±0.1	—	±1.0	μA
Quiescent supply current	ICC	VIN = VCC or GND		6.0	—	—	4.0	—	40.0	μA

Timing Requirements (input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C		Ta = -40 to 85°C	Unit
			V <sub>CC</sub> (V)	Typ.	Limit	
Minimum pulse width (CK)	$t_W$ (H) $t_W$ (L)	—	2.0	—	100	ns
			4.5	—	20	
			6.0	—	17	
Minimum pulse width ( $\overline{\text{LOAD}}$ )	$t_W$ (L)	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum hold time (CLR)	$t_W$ (H)	—	2.0	—	100	ns
			4.5	—	20	
			6.0	—	17	
Minimum set-up time (DATA- $\overline{\text{LOAD}}$ )	$t_s$	—	2.0	—	75	ns
			4.5	—	15	
			6.0	—	13	
Minimum hold time (DATA- $\overline{\text{LOAD}}$ )	$t_h$	—	2.0	—	0	ns
			4.5	—	0	
			6.0	—	0	
Minimum removal time ( $\overline{\text{LOAD}}$ )	$t_{\text{rem}}$	—	2.0	—	50	ns
			4.5	—	10	
			6.0	—	9	
Minimum removal time (CLR)	$t_{\text{rem}}$	—	2.0	—	50	ns
			4.5	—	10	
			6.0	—	9	
Clock frequency	$f$	—	2.0	—	5	MHz
			4.5	—	25	
			6.0	—	29	

AC Characteristics ( $C_L = 15 \text{ pF}$ ,  $V_{CC} = 5 \text{ V}$ ,  $T_a = 25^\circ\text{C}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Output transition time	$t_{TLH}$ $t_{THL}$	—	—	6	12	ns
Propagation delay time (UP, DOWN-Q)	$t_{PLH}$ $t_{PHL}$	—	—	16	33	ns
Propagation delay time (UP- $\overline{\text{CARRY}}$ )	$t_{PLH}$ $t_{PHL}$	—	—	10	22	ns
Propagation delay time (DOWN- $\overline{\text{BORROW}}$ )	$t_{PLH}$ $t_{PHL}$	—	—	10	22	ns
Propagation delay time ( $\overline{\text{LOAD}}$ -Q)	$t_{PLH}$ $t_{PHL}$	—	—	21	38	ns
Propagation delay time ( $\overline{\text{LOAD}}$ - $\overline{\text{CARRY}}$ )	$t_{PLH}$ $t_{PHL}$	—	—	25	44	ns
Propagation delay time ( $\overline{\text{LOAD}}$ - $\overline{\text{BORROW}}$ )	$t_{PLH}$ $t_{PHL}$	—	—	26	44	ns
Propagation delay time (DATA IN-Q)	$t_{PLH}$ $t_{PHL}$	—	—	21	33	ns
Propagation delay time (DATA IN- $\overline{\text{CARRY}}$ )	$t_{PLH}$ $t_{PHL}$	—	—	29	44	ns
Propagation delay time (DATA IN- $\overline{\text{BORROW}}$ )	$t_{PLH}$ $t_{PHL}$	—	—	26	44	ns
Propagation delay time (CLR-Q)	$t_{PHL}$	—	—	25	39	ns
Propagation delay time (CLR- $\overline{\text{CARRY}}$ )	$t_{PLH}$	—	—	30	44	ns
Propagation delay time (CLR- $\overline{\text{BORROW}}$ )	$t_{PHL}$	—	—	30	44	ns
Maximum clock frequency	$f_{\text{max}}$	—	27	52	—	MHz

AC Characteristics ( $C_L = 50 \text{ pF}$ , input:  $t_r = t_f = 6 \text{ ns}$ )

Characteristics	Symbol	Test Condition	Ta = 25°C				Ta = -40 to 85°C		Unit	
			VCC (V)	Min	Typ.	Max	Min	Max		
Output transition time	t <sub>TLH</sub> t <sub>THL</sub>	—	2.0	—	30	75	—	95	ns	
			4.5	—	8	15	—	19		
			6.0	—	7	13	—	16		
Propagation delay time (UP, DOWN-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	65	190	—	240	ns	
			4.5	—	20	38	—	48		
			6.0	—	16	32	—	41		
Propagation delay time (UP- CARRY )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	40	130	—	165	ns	
			4.5	—	13	26	—	33		
			6.0	—	11	22	—	28		
Propagation delay time (DOWN- BORROW )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	40	130	—	165	ns	
			4.5	—	13	26	—	33		
			6.0	—	11	22	—	28		
Propagation delay time ( LOAD -Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	85	220	—	275	ns	
			4.5	—	25	44	—	55		
			6.0	—	20	37	—	47		
Propagation delay time ( LOAD - CARRY )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	110	250	—	315	ns	
			4.5	—	30	50	—	63		
			6.0	—	25	43	—	54		
Propagation delay time ( LOAD - BORROW )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	110	250	—	315	ns	
			4.5	—	30	50	—	63		
			6.0	—	25	43	—	54		
Propagation delay time (DATA IN-Q)	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	80	190	—	240	ns	
			4.5	—	25	38	—	48		
			6.0	—	20	32	—	41		
Propagation delay time (DATA IN- CARRY )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	120	250	—	315	ns	
			4.5	—	34	50	—	63		
			6.0	—	28	43	—	54		
Propagation delay time (DATA IN- BORROW )	t <sub>pLH</sub> t <sub>pHL</sub>	—	2.0	—	110	250	—	315	ns	
			4.5	—	31	50	—	63		
			6.0	—	25	43	—	54		
Propagation delay time (CLR-Q)	t <sub>pHL</sub>	—	2.0	—	100	225	—	280	ns	
			4.5	—	30	45	—	56		
			6.0	—	25	38	—	48		
Propagation delay time (CLR- CARRY )	t <sub>pLH</sub>	—	2.0	—	120	250	—	315	ns	
			4.5	—	35	50	—	63		
			6.0	—	29	43	—	54		
Propagation delay time (CLR- BORROW )	t <sub>pHL</sub>	—	2.0	—	120	250	—	315	ns	
			4.5	—	35	50	—	63		
			6.0	—	29	43	—	54		
Maximum clock frequency	f <sub>max</sub>	—	2.0	5	12	—	4	—	MHz	
			4.5	25	48	—	20	—		
			6.0	29	55	—	24	—		
Input capacitance	C <sub>IN</sub>	—			—	5	10	—	10	pF

Characteristics	Symbol	Test Condition	Ta = 25°C			Ta = -40 to 85°C		Unit
			V <sub>CC</sub> (V)	Min	Typ.	Max	Min	Max
Power dissipation capacitance	C <sub>PD</sub> (Note)	—	—	—	67	—	—	pF

Note: C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}$$

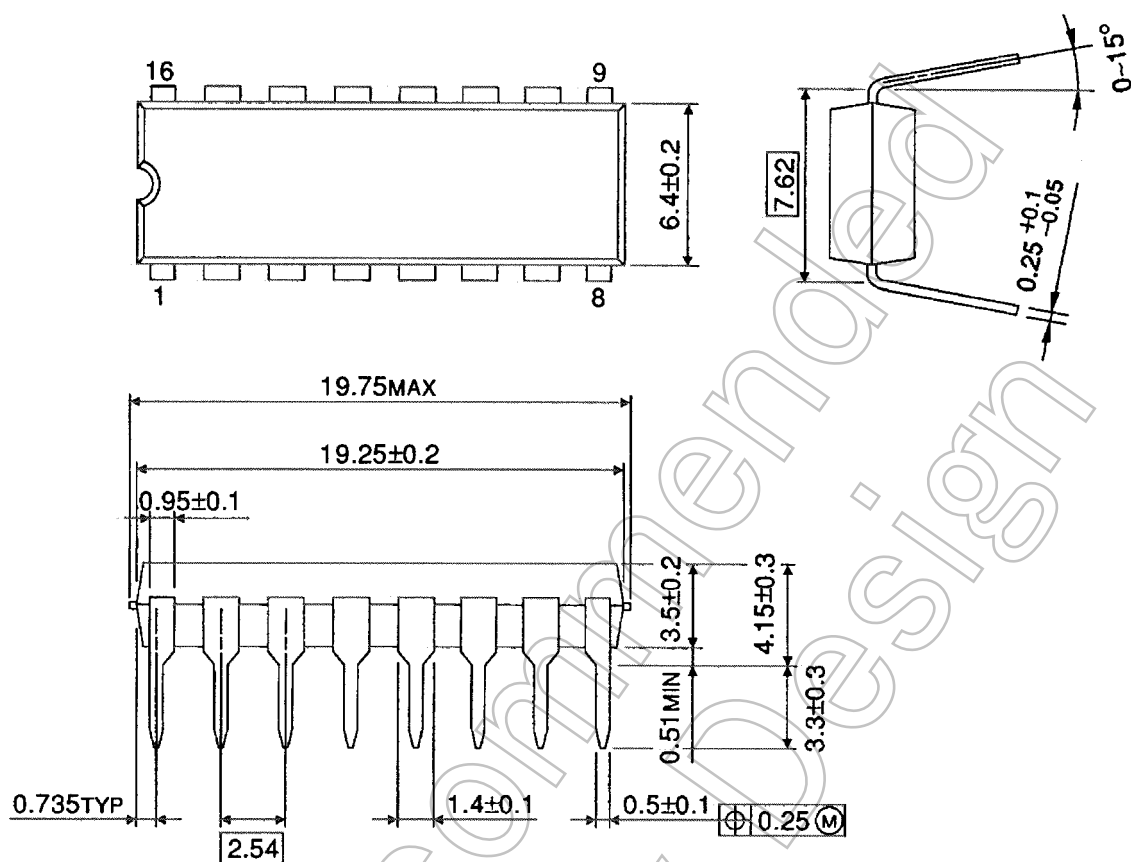
Not Recommended  
for New Design



## Package Dimensions

DIP16-P-300-2.54A

Unit : mm

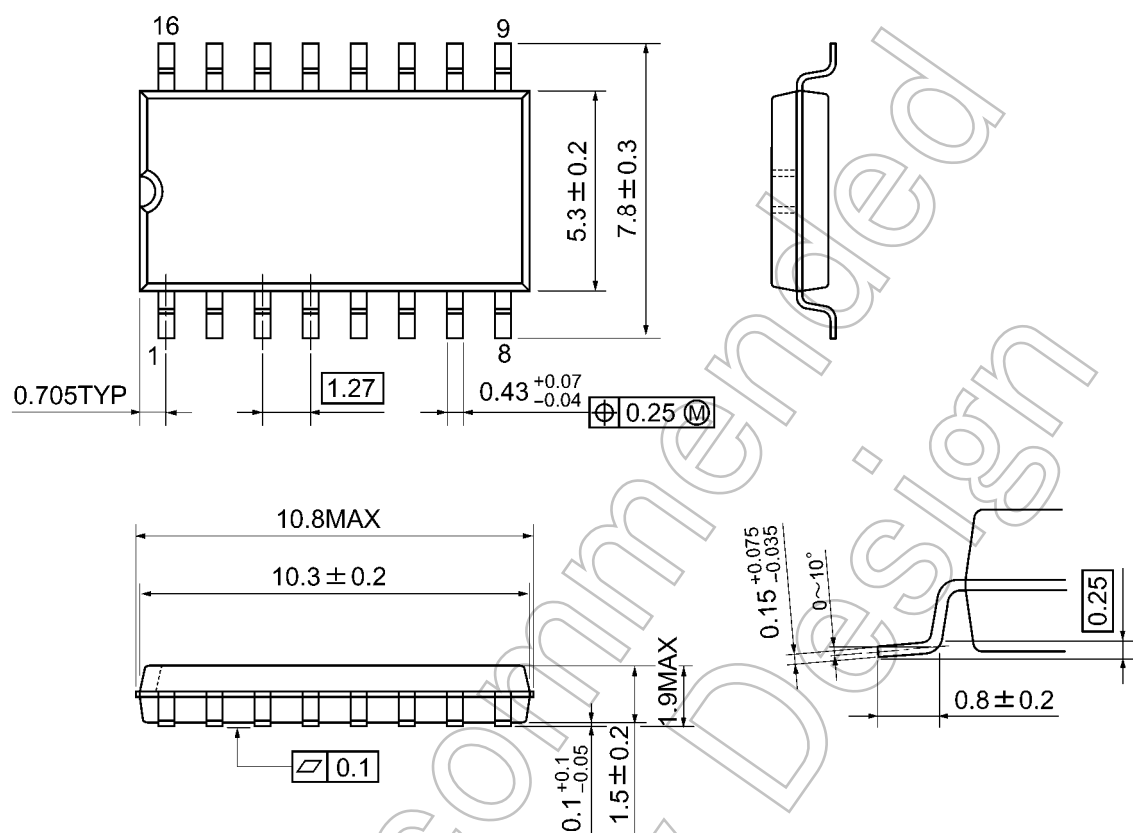


Weight: 1.00 g (typ.)

## Package Dimensions

SOP16-P-300-1.27A

Unit: mm



Weight: 0.18 g (typ.)

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