



74LVC157A

Quad 2-input multiplexer

Rev. 13 — 9 May 2025

Product data sheet

1. General description

The 74LVC157A is a quad 2-input multiplexer. The device features select (S) and enable $\bar{E}$ inputs. A HIGH on S selects data source 1, a LOW data source 0. A HIGH on $\bar{E}$ forces all the outputs (1Y to 4Y) LOW. Inputs can be driven from either 3.3 V or 5 V devices. This feature allows the use of these devices as translators in mixed 3.3 V and 5 V applications.

Schmitt-trigger action at all inputs makes the circuit tolerant of slower input rise and fall times.

2. Features and benefits

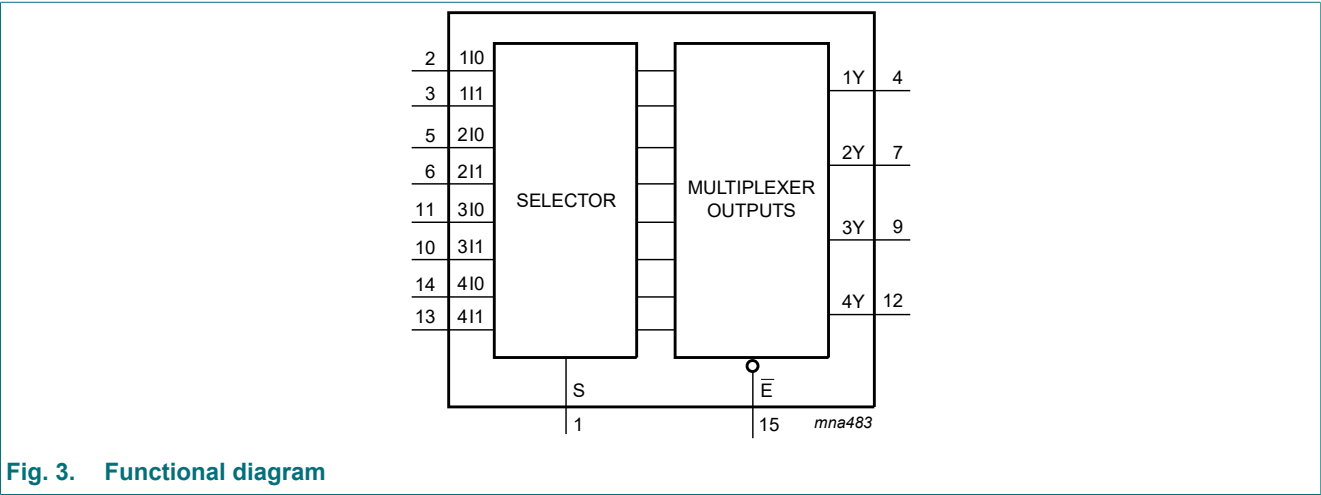
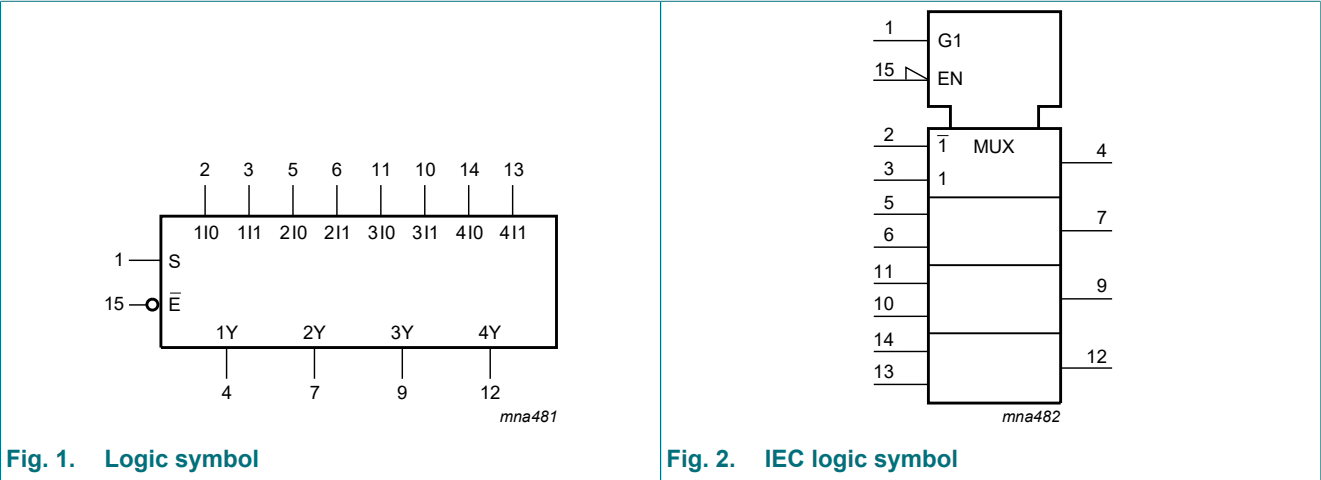
- Overvoltage tolerant inputs to 5.5 V
- Wide supply voltage range from 1.2 V to 3.6 V
- CMOS low power consumption
- Direct interface with TTL levels
- Complies with JEDEC standard:
 - JESD8-7A (1.65 V to 1.95 V)
 - JESD8-5A (2.3 V to 2.7 V)
 - JESD8-C/JESD36 (2.7 V to 3.6 V)
- ESD protection:
 - HBM: ANSI/ESDA/JEDEC JS-001 class 2 exceeds 2000 V
 - CDM: ANSI/ESDA/JEDEC JS-002 class C3 exceeds 1000 V
- Multiple package options
- Specified from -40 °C to +85 °C and -40 °C to +125 °C

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LVC157AD	-40 °C to +125 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LVC157APW	-40 °C to +125 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1
74LVC157ABQ	-40 °C to +125 °C	DHVQFN16	plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 16 terminals; body 2.5 × 3.5 × 0.85 mm	SOT763-1
74LVC157ABZ	-40 °C to +125 °C	DHXQFN16	plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package; no leads; 16 terminals; 0.4 mm pitch; body 2 mm × 2.4 mm × 0.48 mm	SOT8016-1

3.1. Functional diagram



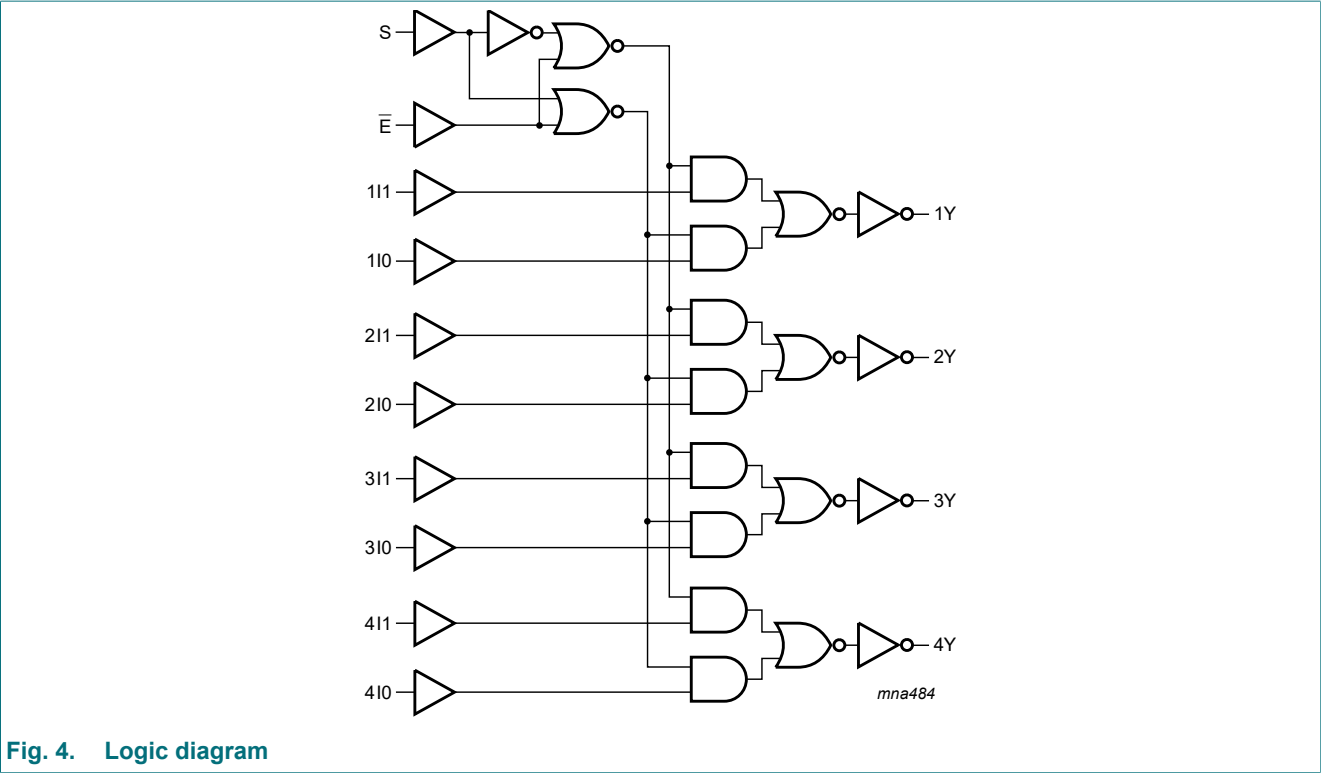
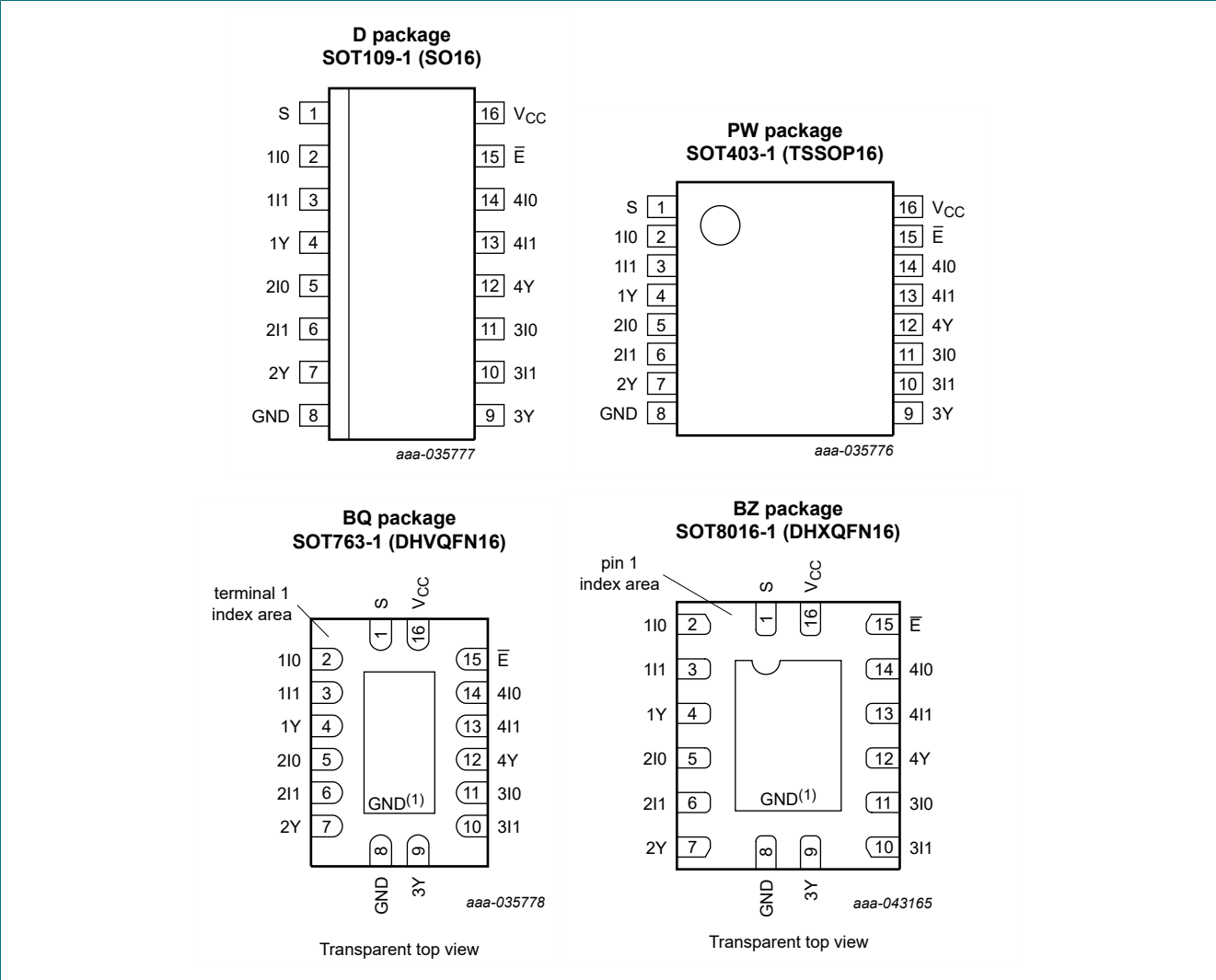


Fig. 4. Logic diagram

4. Pinning information

4.1. Pinning



4.2. Pin description

Table 2. Pin description

Symbol	Pin	Description
S	1	common data select input
1I0, 2I0, 3I0, 4I0	2, 5, 11, 14	data input from source 0
1I1, 2I1, 3I1, 4I1	3, 6, 10, 13	data input from source 1
1Y, 2Y, 3Y, 4Y	4, 7, 9, 12	multiplexer output
GND	8	ground (0 V)
E	15	enable input (active LOW)
V _{CC}	16	supply voltage

5. Functional description

Table 3. Function table

H = HIGH voltage level; L = LOW voltage level; X = don't care

Input				Output
E	S	nI0	nI1	nY
H	X	X	X	L
L	L	L	X	L
L	L	H	X	H
L	H	X	L	L
L	H	X	H	H

6. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+6.5	V
I _{IK}	input clamping current	V _I < 0	-50	-	mA
V _I	input voltage	[1]	-0.5	+6.5	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0	-	±50	mA
V _O	output voltage	[2]	-0.5	V _{CC} + 0.5	V
I _O	output current	V _O = 0 V to V _{CC}	-	±50	mA
I _{CC}	supply current		-	100	mA
I _{GND}	ground current		-100	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +125 °C			
		SOT109-1 (SO16) [3]	-	500	mW
		SOT403-1 (TSSOP16) [4]			
		SOT763-1 (DHVQFN16) [5]			
		SOT8016-1 (DHXQFN16)	-	250	mW

- [1] The minimum input voltage ratings may be exceeded if the input current ratings are observed.
[2] The output voltage ratings may be exceeded if the output current ratings are observed.
[3] For SOT109-1 (SO16) package: P_{tot} derates linearly with 12.4 mW/K above 110 °C.
[4] For SOT403-1 (TSSOP16) package: P_{tot} derates linearly with 8.5 mW/K above 91 °C.
[5] For SOT763-1 (DHVQFN16) package: P_{tot} derates linearly with 11.2 mW/K above 106 °C.

7. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		1.65	-	3.6	V
		functional	1.2	-	-	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+125	°C

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta t/\Delta V$	input transition rise and fall rate	$V_{CC} = 1.65\text{ V to }2.7\text{ V}$	0	-	20	ns/V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	0	-	10	ns/V

8. Static characteristics

Table 6. Static characteristics

At recommended operating conditions. Voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$V_{CC} = 1.2\text{ V}$	1.08	-	-	1.08	-	V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	$0.65 \times V_{CC}$	-	-	$0.65 \times V_{CC}$	-	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	1.7	-	-	1.7	-	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	2.0	-	-	2.0	-	V
V_{IL}	LOW-level input voltage	$V_{CC} = 1.2\text{ V}$	-	-	0.12	-	0.12	V
		$V_{CC} = 1.65\text{ V to }1.95\text{ V}$	-	-	$0.35 \times V_{CC}$	-	$0.35 \times V_{CC}$	V
		$V_{CC} = 2.3\text{ V to }2.7\text{ V}$	-	-	0.7	-	0.7	V
		$V_{CC} = 2.7\text{ V to }3.6\text{ V}$	-	-	0.8	-	0.8	V
V_{OH}	HIGH-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$						
		$I_O = -100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }3.6\text{ V}$	$V_{CC} - 0.2$	-	-	$V_{CC} - 0.3$	-	V
		$I_O = -4\text{ mA}; V_{CC} = 1.65\text{ V}$	1.2	-	-	1.05	-	V
		$I_O = -8\text{ mA}; V_{CC} = 2.3\text{ V}$	1.8	-	-	1.65	-	V
		$I_O = -12\text{ mA}; V_{CC} = 2.7\text{ V}$	2.2	-	-	2.05	-	V
		$I_O = -18\text{ mA}; V_{CC} = 3.0\text{ V}$	2.4	-	-	2.25	-	V
		$I_O = -24\text{ mA}; V_{CC} = 3.0\text{ V}$	2.2	-	-	2.0	-	V
V_{OL}	LOW-level output voltage	$V_I = V_{IH}\text{ or }V_{IL}$						
		$I_O = 100\text{ }\mu\text{A}; V_{CC} = 1.65\text{ V to }3.6\text{ V}$	-	-	0.2	-	0.3	V
		$I_O = 4\text{ mA}; V_{CC} = 1.65\text{ V}$	-	-	0.45	-	0.65	V
		$I_O = 8\text{ mA}; V_{CC} = 2.3\text{ V}$	-	-	0.6	-	0.8	V
		$I_O = 12\text{ mA}; V_{CC} = 2.7\text{ V}$	-	-	0.4	-	0.6	V
		$I_O = 24\text{ mA}; V_{CC} = 3.0\text{ V}$	-	-	0.55	-	0.8	V
I_I	input leakage current	$V_{CC} = 3.6\text{ V}; V_I = 5.5\text{ V or GND}$	-	± 0.1	± 5	-	± 20	μA
I_{CC}	supply current	$V_{CC} = 3.6\text{ V}; V_I = V_{CC}\text{ or GND}; I_O = 0\text{ A}$	-	0.1	10	-	40	μA
ΔI_{CC}	additional supply current	per input pin; $V_I = V_{CC} - 0.6\text{ V}; V_{CC} = 2.7\text{ V to }3.6\text{ V}; I_O = 0\text{ A}$	-	5	500	-	5000	μA
C_I	input capacitance	$V_{CC} = 0\text{ V to }3.6\text{ V}; V_I = \text{GND to }V_{CC}$	-	5.0	-	-	-	pF

[1] All typical values are measured at $V_{CC} = 3.3\text{ V}$ (unless stated otherwise) and $T_{amb} = 25\text{ }^\circ\text{C}$.

9. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V). For test circuit see Fig. 7.

Symbol	Parameter	Conditions	-40 °C to +85 °C			-40 °C to +125 °C		Unit
			Min	Typ[1]	Max	Min	Max	
t_{pd}	propagation delay	nI0, nI1 to nY; see Fig. 5 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	16	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	4.8	10.2	1.0	11.8	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	2.8	5.8	1.5	6.7	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.9	5.9	1.0	7.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.5	5.2	1.0	6.5	ns
		$\bar{E}$ to nY; see Fig. 6 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	17	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	0.5	4.8	12.8	0.5	14.7	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	2.8	7.2	1.5	8.3	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	2.9	7.8	1.0	10.0	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.6	6.5	1.0	8.5	ns
		S to nY; see Fig. 5 [2]						
		$V_{CC} = 1.2 \text{ V}$	-	16	-	-	-	ns
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	1.0	5.1	12.4	1.0	14.3	ns
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	1.5	3.0	7.0	1.5	8.1	ns
		$V_{CC} = 2.7 \text{ V}$	1.0	3.1	7.3	1.0	9.5	ns
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	1.0	2.7	6.3	1.0	8.0	ns
$t_{sk(o)}$	output skew time	$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$ [3]	-	-	1.0	-	1.5	ns
C_{PD}	power dissipation capacitance	per input; $V_I = \text{GND to } V_{CC}$ [4]						
		$V_{CC} = 1.65 \text{ V to } 1.95 \text{ V}$	-	9.4	-	-	-	pF
		$V_{CC} = 2.3 \text{ V to } 2.7 \text{ V}$	-	12.8	-	-	-	pF
		$V_{CC} = 3.0 \text{ V to } 3.6 \text{ V}$	-	15.9	-	-	-	pF

[1] Typical values are measured at $T_{amb} = 25 \text{ °C}$ and $V_{CC} = 1.2 \text{ V}$, 1.8 V , 2.5 V , 2.7 V , and 3.3 V respectively.

[2] t_{pd} is the same as t_{PLH} and t_{PHL} .

[3] Skew between any two outputs of the same package switching in the same direction. This parameter is guaranteed by design.

[4] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).

$P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum (C_L \times V_{CC}^2 \times f_o)$ where:

f_i = input frequency in MHz; f_o = output frequency in MHz

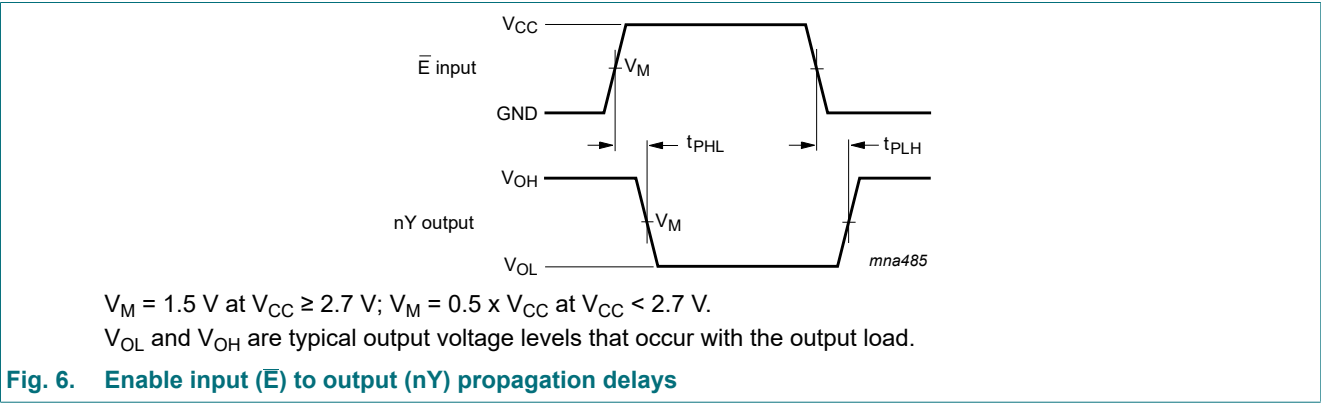
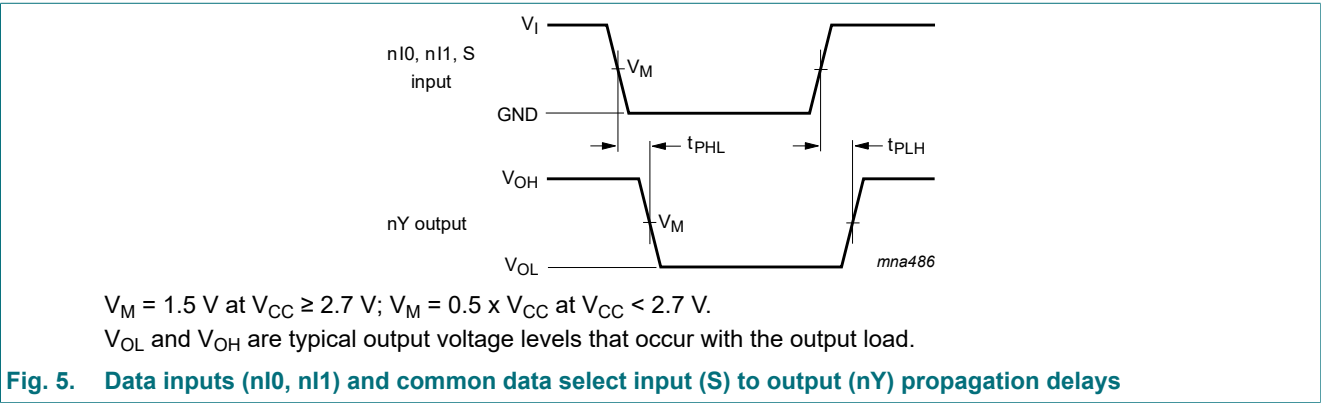
C_L = output load capacitance in pF

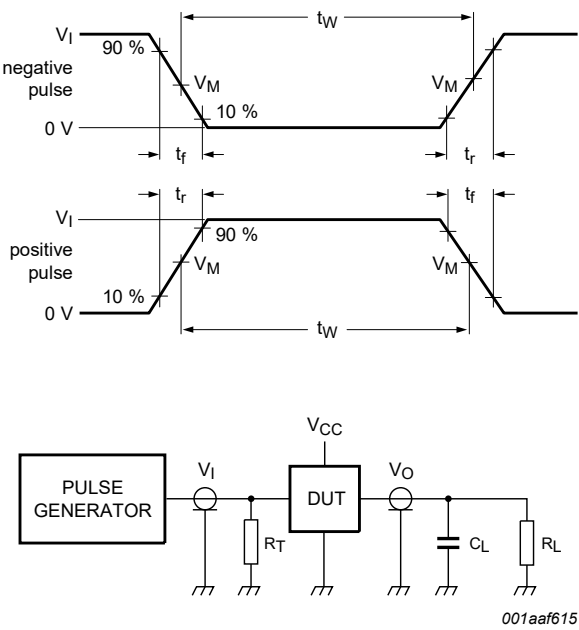
V_{CC} = supply voltage in V

N = number of inputs switching

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

9.1. Waveforms and test circuit





Test data is given in [Table 8](#).
Definitions for test circuit:
 R_L = Load resistance;
 C_L = Load capacitance including jig and probe capacitance;
 R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig. 7. Test circuit for measuring switching times

Table 8. Test data

Supply voltage	Input		Load	
	V_I	t_r, t_f	C_L	R_L
1.2 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
1.65 V to 1.95 V	V_{CC}	≤ 2 ns	30 pF	1 k Ω
2.3 V to 2.7 V	V_{CC}	≤ 2 ns	30 pF	500 Ω
2.7 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω
3.0 V to 3.6 V	2.7 V	≤ 2.5 ns	50 pF	500 Ω

10. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm SOT109-1

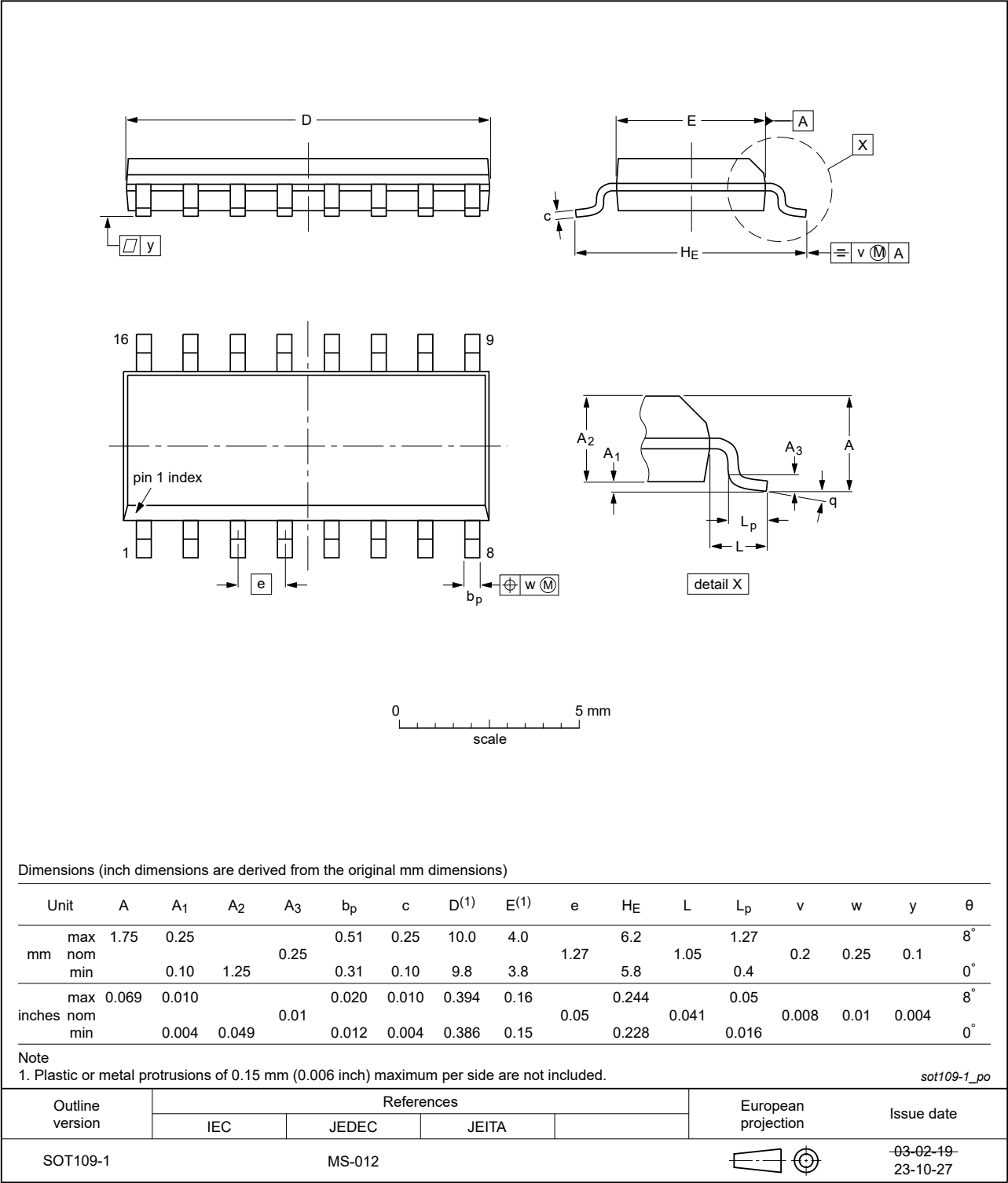


Fig. 8. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

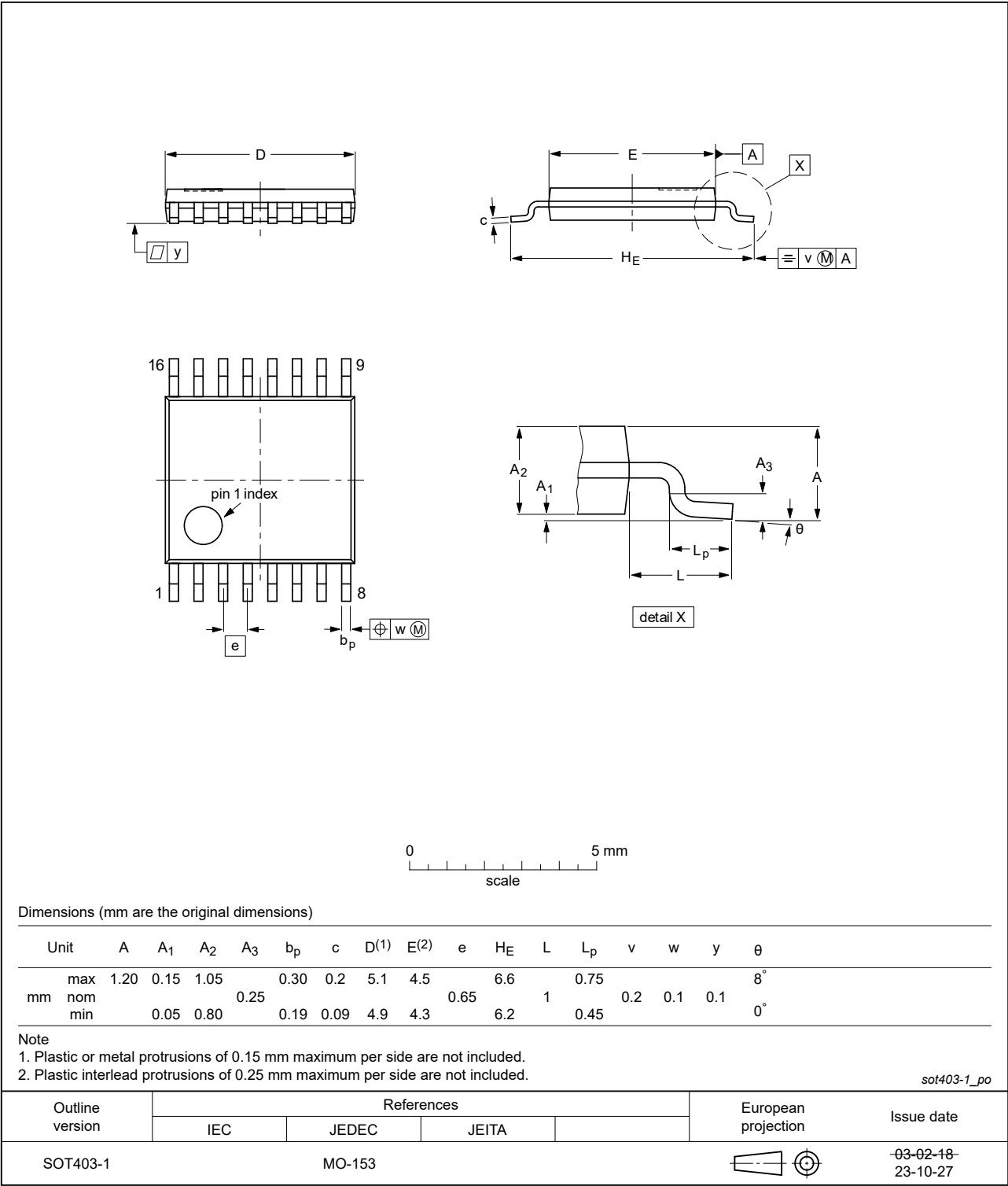


Fig. 9. Package outline SOT403-1 (TSSOP16)

DHVQFN16: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads;
16 terminals; body 2.5 x 3.5 x 0.85 mm SOT763-1

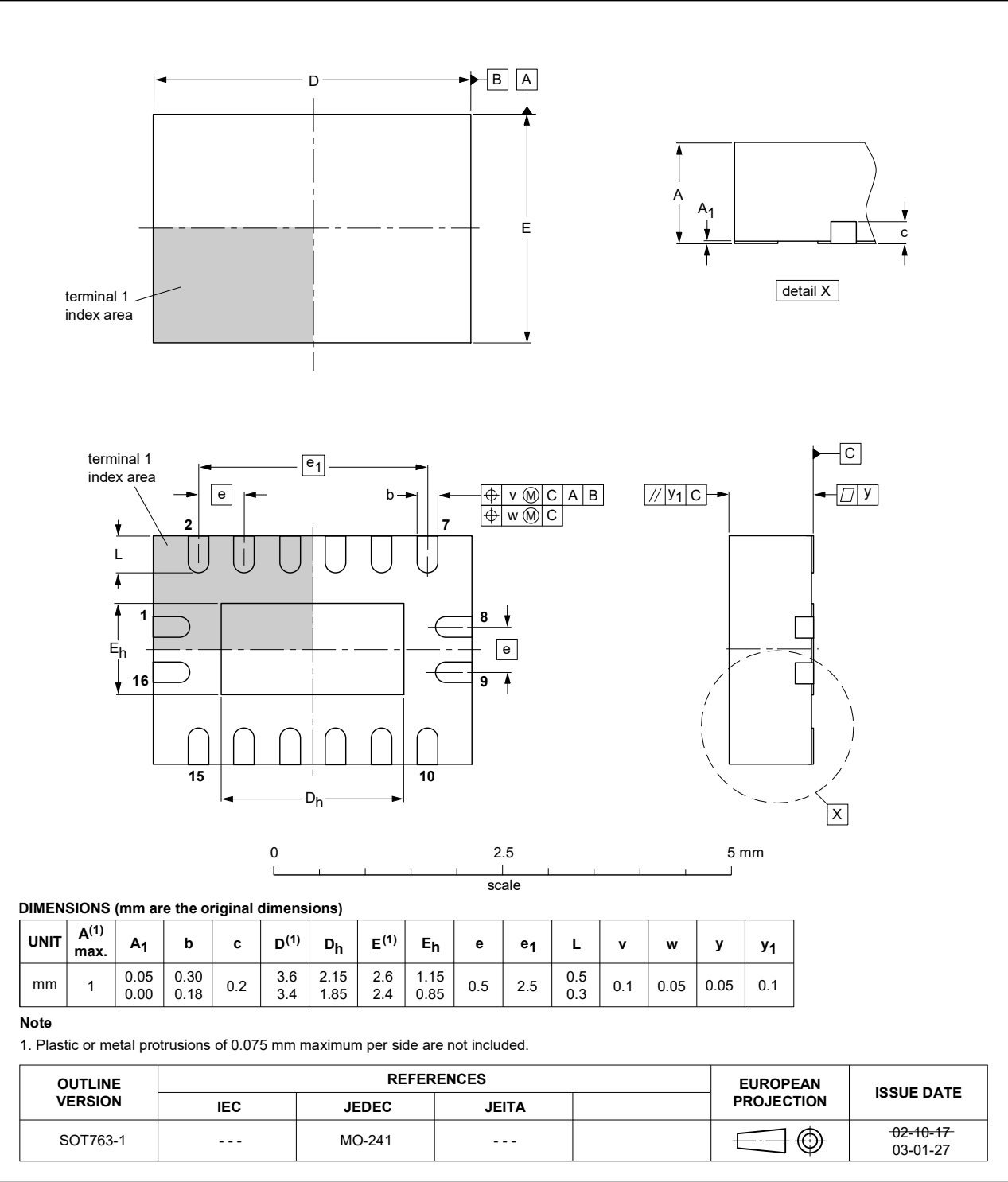


Fig. 10. Package outline SOT763-1 (DHVQFN16)

DHXQFN16: plastic, leadless dual in-line compatible thermal enhanced extreme thin quad flat package;
no leads; 16 terminals; 0.4 mm pitch; body 2 mm x 2.4 mm x 0.48 mm

SOT8016-1

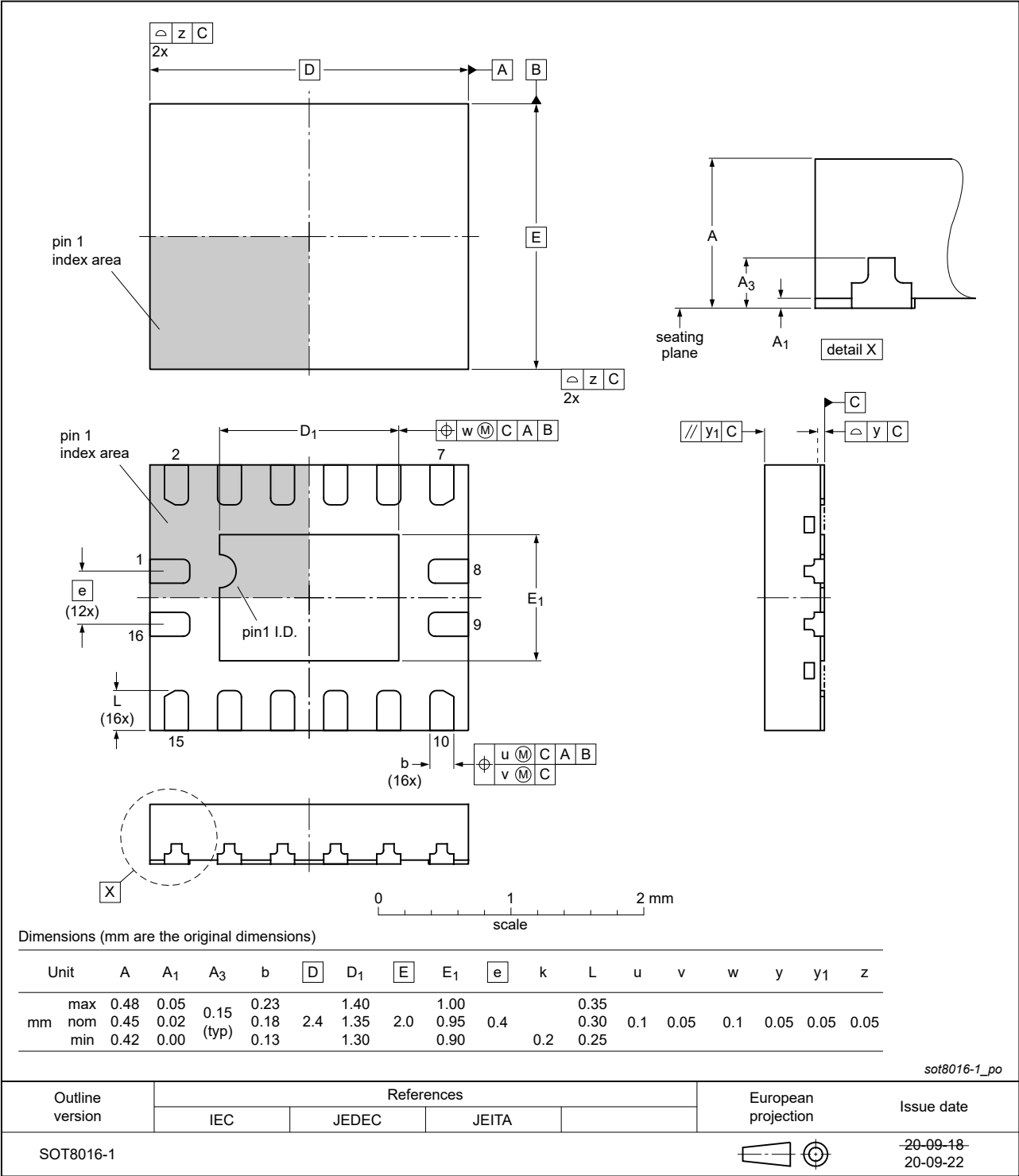


Fig. 11. Package outline SOT8016-1 (DHXQFN16)

11. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANSI	American National Standards Institute
CDM	Charged Device Model
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESDA	ElectroStatic Discharge Association
HBM	Human Body Model
JEDEC	Joint Electron Device Engineering Council
TTL	Transistor-Transistor Logic

12. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LVC157A v.13	20250509	Product data sheet	-	74LVC157A v.12
Modifications:	• Type number 74LVC157ABZ (SOT8016-1/DHXQFN16 added.			
74LVC157A v.12	20240212	Product data sheet	-	74LVC157A v.11
Modifications:	• Fig. 8 , Fig. 9 : Aligned SO and TSSOP package outline drawings to JEDEC MS-012 and MO-153.			
74LVC157A v.11	20230804	Product data sheet	-	74LVC157A v.10
Modifications:	• Section 2 : ESD specification updated according to the latest JEDEC standard.			
74LVC157A v.10	20210920	Product data sheet	-	74LVC157A v.9
Modifications:	• Type number 74LVC157ADB (SOT338-1/SSOP16) removed. • Section 1 updated.			
74LVC157A v.9	20200319	Product data sheet	-	74LVC157A v.8
Modifications:	• Table 4 : Derating values for P _{tot} total power dissipation updated.			
74LVC157A v.8	20171011	Product data sheet	-	74LVC157A v.7
Modifications:	• The format of this data sheet has been redesigned to comply with the identity guidelines of Nexperia. • Legal texts have been adapted to the new company name where appropriate.			
74LVC157A v.7	20111125	Product data sheet	-	74LVC157A v.6
Modifications:	• Table 7 : maximum values for lower voltage ranges changed (errata).			
74LVC157A v.6	20111027	Product data sheet	-	74LVC157A v.5
Modifications:	• The format of this document has been redesigned to comply with the new identity guidelines of NXP Semiconductors. • Legal texts have been adapted to the new company name where appropriate. • Table 4 , Table 5 , Table 6 , Table 7 , and Table 8 : values added for lower voltage ranges.			
74LVC157A v.5	031202	Product specification	-	74LVC157A v.4
74LVC157A v.4	030617	Product specification	-	74LVC157A v.3
74LVC157A v.3	020315	Product specification	-	74LVC157A v.2
74LVC157A v.2	980729	Product specification	-	-

13. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

- [1] Please consult the most recently issued document before initiating or completing a design.
- [2] The term 'short data sheet' is explained in section "Definitions".
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Contents

1. General description..... 1

2. Features and benefits..... 1

3. Ordering information..... 1

3.1. Functional diagram..... 2

4. Pinning information..... 4

4.1. Pinning..... 4

4.2. Pin description..... 4

5. Functional description..... 5

6. Limiting values..... 5

7. Recommended operating conditions..... 5

8. Static characteristics..... 6

9. Dynamic characteristics..... 7

9.1. Waveforms and test circuit..... 8

10. Package outline..... 10

11. Abbreviations..... 14

12. Revision history..... 14

13. Legal information..... 15

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