

# MC100EPT26

## 3.3V 1:2 Fanout Differential LVPECL to LVTTTL Translator

The MC100EPT26 is a 1:2 Fanout Differential LVPECL to LVTTTL translator. Because LVPECL (Positive ECL) levels are used only +3.3 V and ground are required. The small outline 8-lead package and the 1:2 fanout design of the EPT26 makes it ideal for applications which require the low skew duplication of a signal in a tightly packed PC board.

The  $V_{BB}$  output allows the EPT26 to be used in a single-ended input mode. In this mode the  $V_{BB}$  output is tied to the  $\overline{D0}$  input for a non-inverting buffer or the D0 input for an inverting buffer. If used, the  $V_{BB}$  pin should be bypassed to ground via a 0.01  $\mu$ F capacitor.

- 1.4 ns Typical Propagation Delay
- Maximum Frequency > 275 MHz Typical
- The 100 Series Contains Temperature Compensation
- Operating Range:  $V_{CC} = 3.0$  V to 3.6 V with GND = 0 V
- Open Input Default State
- Safety Clamp on Inputs
- 24 mA TTL outputs
- Q Outputs Will Default LOW with Inputs Open or at  $V_{EE}$
- $V_{BB}$  Output



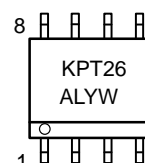
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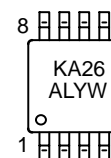
### MARKING DIAGRAMS\*



**SO-8  
D SUFFIX  
CASE 751**



**TSSOP-8  
DT SUFFIX  
CASE 948R**



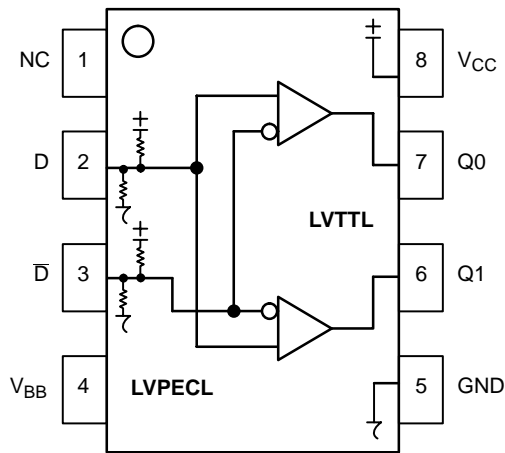
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week

\*For additional information, see Application Note AND8002/D

### ORDERING INFORMATION

Device	Package	Shipping
MC100EPT26D	SO-8	98 Units/Rail
MC100EPT26DR2	SO-8	2500 Tape & Reel
MC100EPT26DT	TSSOP-8	100 Units/Rail
MC100EPT26DTR2	TSSOP-8	2500 Tape & Reel

# MC100EPT26



## PIN DESCRIPTION

PIN	FUNCTION
Q0, Q1	LVTTTL Outputs
D**, D**	Differential LVPECL Input Pair
V <sub>CC</sub>	Positive Supply
V <sub>BB</sub>	Output Reference Voltage
GND	Ground
NC	No Connect

\*\* Pins will default to V<sub>CC</sub>/2 when left open.

Figure 1. 8-Lead Pinout (Top View) and Logic Diagram

## ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistor	75 kΩ
Internal Input Pullup Resistor	37.5 kΩ
ESD Protection	Human Body Model Machine Model Charged Device Model
	> 2 kV > 100 V > 2 kV
Moisture Sensitivity, Indefinite Time Out of Drypack (Note 1)	Level 1
Flammability Rating	Oxygen Index: 28 to 34
	UL 94 V-0 @ 0.125 in
Transistor Count	117 Devices
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

## MAXIMUM RATINGS (Note 2)

Symbol	Parameter	Condition 1	Condition 2	Rating	Units
V <sub>CC</sub>	Positive Power Supply	GND = 0 V		3.8	V
V <sub>IN</sub>	Input Voltage	GND = 0 V	V <sub>I</sub> ≤ V <sub>CC</sub>	0 to 3.8	V
I <sub>BB</sub>	V <sub>BB</sub> Sink/Source			± 0.5	mA
T <sub>A</sub>	Operating Temperature Range			-40 to +85	°C
T <sub>stg</sub>	Storage Temperature Range			-65 to +150	°C
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 SOIC 8 SOIC	190 130	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	8 SOIC	41 to 44	°C/W
θ <sub>JA</sub>	Thermal Resistance (Junction-to-Ambient)	0 LFPM 500 LFPM	8 TSSOP 8 TSSOP	185 140	°C/W °C/W
θ <sub>JC</sub>	Thermal Resistance (Junction-to-Case)	std bd	8 TSSOP	41 to 44	°C/W
T <sub>sol</sub>	Wave Solder	< 2 to 3 sec @ 248°C		265	°C

2. Maximum Ratings are those values beyond which device damage may occur.

# MC100EPT26

## PECL INPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$ ; GND = 0.0 V (Note 3)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$V_{IH}$	Input HIGH Voltage (Single-Ended)	2075		2420	2075		2420	2075		2420	mV
$V_{IL}$	Input LOW Voltage (Single-Ended)	1355		1675	1355		1675	1355		1675	mV
$V_{BB}$	Output Voltage Reference	1775	1875	1975	1775	1875	1975	1775	1875	1975	V
$V_{IHCMR}$	Input HIGH Voltage Common Mode Range (Differential) (Note 4)	2.0		3.3	2.0		3.3	2.0		3.3	V
$I_{IH}$	Input HIGH Current			150			150			150	$\mu\text{A}$
$I_{IL}$	Input LOW Current	$\overline{D}$ 0.5 $\overline{D}$ -150			0.5 -150			0.5 -150			$\mu\text{A}$

NOTE: Devices are designed to meet the DC specifications shown in the above table, after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse air flow greater than 500 lfm is maintained.

3. Input parameters vary 1:1 with  $V_{CC}$ .

4.  $V_{IHCMR}$  min varies 1:1 with GND,  $V_{IHCMR}$  max varies 1:1 with  $V_{CC}$ . The  $V_{IHCMR}$  range is referenced to the most positive side of the differential input signal.

## TTL OUTPUT DC CHARACTERISTICS $V_{CC} = 3.3\text{ V}$ ; GND = 0.0 V; $T_A = -40^\circ\text{C}$ to $85^\circ\text{C}$

Symbol	Characteristic	Condition	Min	Typ	Max	Unit
$V_{OH}$	Output HIGH Voltage (Note 5)	$I_{OH} = -3.0\text{ mA}$	2.4			V
$V_{OL}$	Output LOW Voltage (Note 5)	$I_{OL} = 24\text{ mA}$			0.5	V
$I_{CCH}$	Power Supply Current		10	20	18	mA
$I_{CCL}$	Power Supply Current		15	28	35	mA
$I_{OS}$	Output Short Circuit Current		-50		-150	mA

5. All loading with 500  $\Omega$  to GND,  $C_L = 20\text{ pF}$ .

## AC CHARACTERISTICS $V_{CC} = 3.0\text{ V}$ to $3.6\text{ V}$ ; GND = 0.0 V (Note 6)

Symbol	Characteristic	-40 °C			25 °C			85 °C			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$f_{max}$	Maximum Frequency (See Figure 2. $F_{max}/JITTER$ )	275	350		275	350		275	350		MHz
$t_{PLH}$ , $t_{PHL}$	Propagation Delay to Output Differential (Note 7)	1.2 1.2	1.5 1.5	1.8 1.8	1.2 1.2	1.5 1.5	1.8 1.8	1.3 1.2	1.7 1.5	2.2 1.8	ns
$t_{SK+ +}$ $t_{SK- -}$ $t_{SKPP}$	Within Device Skew++ Within Device Skew- - Device- to- Device Skew (Note 8)			60 25 500			60 25 500			60 25 500	ps
$t_{JITTER}$	Cycle-to-Cycle Jitter (See Figure 2. $F_{max}/JITTER$ )		TBD			TBD			TBD		ps
$V_{PP}$	Input Voltage Swing (Differential)	150	800	1200	150	800	1200	150	800	1200	mV
$t_r$ $t_f$	Output Rise/Fall Times (0.8V - 2.0V) $Q, \overline{Q}$	330	600	900	330	600	900	330	650	900	ps

6. Measured with a 750 mV 50% duty-cycle clock source.  $R_L = 500\text{ }\Omega$  to GND and  $C_L = 20\text{ pF}$  to GND. Refer to Figure 3.

7. Reference ( $V_{CC} = 3.3\text{ V} \pm 5\%$ ; GND = 0V)

8. Skews are measured between outputs under identical transitions.

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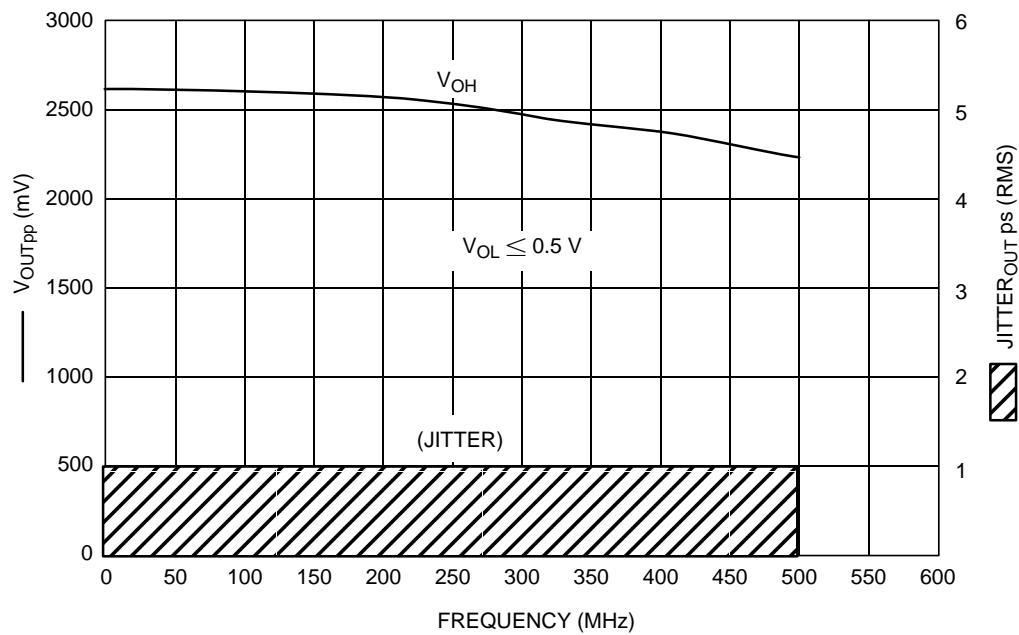


Figure 2.  $F_{max}/Jitter$

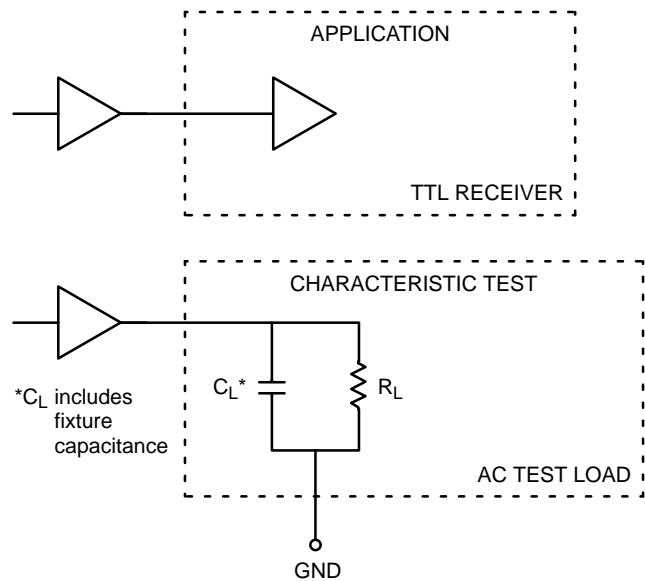


Figure 3. TTL Output Loading Used for Device Evaluation


## Resource Reference of Application Notes

- AN1404** - ECLinPS Circuit Performance at Non-Standard  $V_{IH}$  Levels
- AN1405** - ECL Clock Distribution Techniques
- AN1406** - Designing with PECL (ECL at +5.0 V)
- AN1503** - ECLinPS I/O SPICE Modeling Kit
- AN1504** - Metastability and the ECLinPS Family
- AN1560** - Low Voltage ECLinPS SPICE Modeling Kit
- AN1568** - Interfacing Between LVDS and ECL
- AN1596** - ECLinPS Lite Translator ELT Family SPICE I/O Model Kit
- AN1650** - Using Wire-OR Ties in ECLinPS Designs
- AN1672** - The ECL Translator Guide
- AND8001** - Odd Number Counters Design
- AND8002** - Marking and Date Codes
- AND8020** - Termination of ECL Logic Devices

For an updated list of Application Notes, please see our website at <http://onsemi.com>.



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