Features

- High-performance, Low-power Atmel® AVR® 8-bit Microcontroller
- Advanced RISC Architecture
  - 131 Powerful Instructions – Most Single-clock Cycle Execution
  - 32 × 8 General Purpose Working Registers
  - Fully Static Operation
  - Up to 20 MIPS Throughput at 20 MHz
  - On-chip 2-cycle Multiplier
- High Endurance Non-volatile Memory segments
  - 16K/32K/64K Bytes of In-System Self-programmable Flash program memory
  - 512B/1K/2K Bytes EEPROM
  - 1K/2K/4K Bytes Internal SRAM
  - Write/Erase Cycles: 10,000 Flash/ 100,000 EEPROM
  - Data retention: 20 years at 85°C/100 years at 25°C[1]
  - Optional Boot Code Section with Independent Lock Bits
    - In-System Programming by On-chip Boot Program
    - True Read-While-Write Operation
  - Programming Lock for Software Security
- JTAG (IEEE std. 1149.1 Compliant) Interface
  - Boundary-scan Capabilities According to the JTAG Standard
  - Extensive On-chip Debug Support
  - Programming of Flash, EEPROM, Fuses, and Lock Bits through the JTAG Interface
- Peripheral Features
  - Two 8-bit Timer/Counters with Separate Prescalers and Compare Modes
  - One 16-bit Timer/Counter with Separate Prescaler, Compare Mode, and Capture Mode
  - Real Time Counter with Separate Oscillator
  - Six PWM Channels
  - 8-channel, 10-bit ADC
    - Differential mode with selectable gain at 1×, 10× or 200×
  - Byte-oriented Two-wire Serial Interface
  - Two Programmable Serial USART
  - Master/Slave SPI Serial Interface
  - Programmable Watchdog Timer with Separate On-chip Oscillator
  - On-chip Analog Comparator
  - Interrupt and Wake-up on Pin Change
- Special Microcontroller Features
  - Power-on Reset and Programmable Brown-out Detection
  - Internal Calibrated RC Oscillator
  - External and Internal Interrupt Sources
  - Six Sleep Modes: Idle, ADC Noise Reduction, Power-save, Power-down, Standby and Extended Standby
- I/O and Packages
  - 32 Programmable I/O Lines
  - 40-pin PDIP, 44-lead TQFP, 44-pad VQFN/QFN/MLF (ATmega164P/324P/644P)
  - 44-pad DRQFN (ATmega164P)
- Operating Voltages
  - 1.8V - 5.5V for ATmega164P/324P/644PV
  - 2.7V - 5.5V for ATmega164P/324P/644P
- Speed Grades
  - ATmega164P/324P/644PV: 0 - 4 MHz @ 1.8V - 5.5V, 0 - 10 MHz @ 2.7V - 5.5V
  - ATmega164P/324P/644P: 0 - 10 MHz @ 2.7V - 5.5V, 0 - 20 MHz @ 4.5V - 5.5V
- Power Consumption at 1 MHz, 1.8V, 25°C for ATmega164P/324P/644PV
  - Active: 0.4 mA
  - Power-down Mode: 0.1 µA
  - Power-save Mode: 0.6 µA (Including 32 kHz RTC)

Note: 1. See ”Data Retention” on page 8.

8-bit Atmel Microcontroller with 16K/32K/64K Bytes In-System Programmable Flash

ATmega164P/V
ATmega324P/V
ATmega644P/V

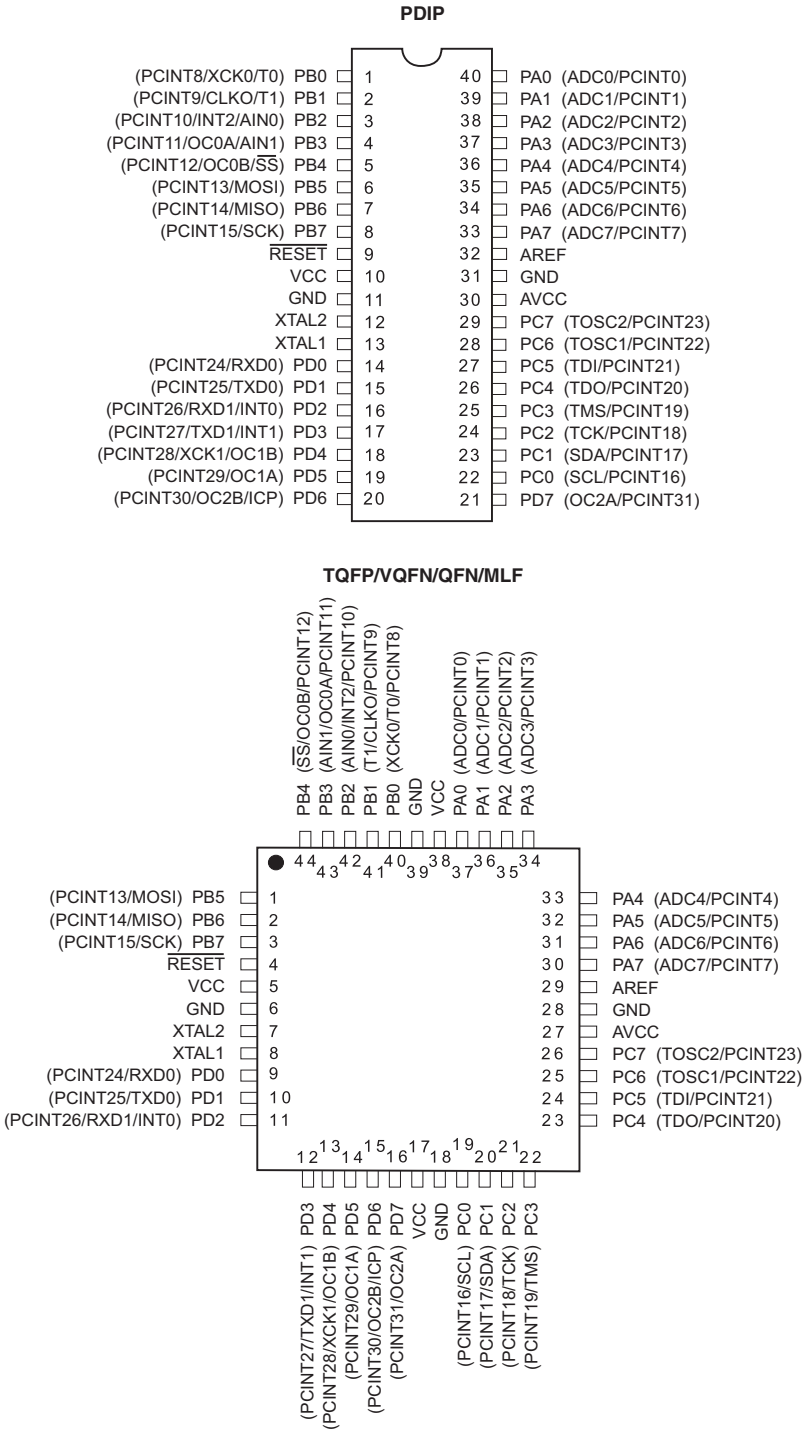
Summary

8011QS–AVR–02/2013

1. Pin Configurations

1.1 Pinout - PDIP/TQFP/VQFN/QFN/MLF

Figure 1-1. Pinout ATmega164P/324P/644P



Note: The large center pad underneath the VQFN/QFN/MLF package should be soldered to ground on the board to ensure good mechanical stability.

1.2 Pinout - DRQFN

Figure 1-2. DRQFN - Pinout ATmega164P

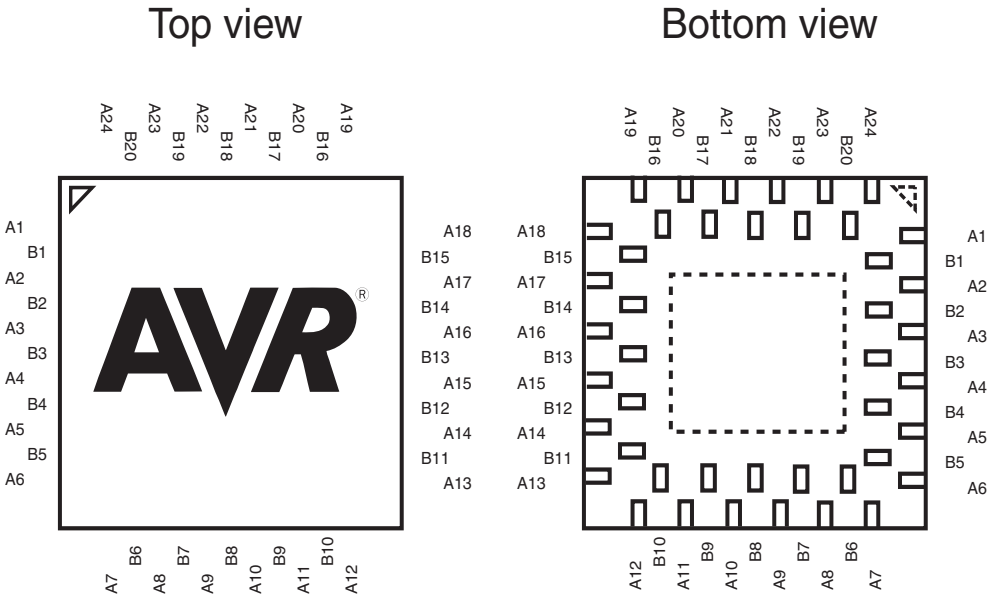


Table 1-1. DRQFN - Pinout ATmega164P/324P

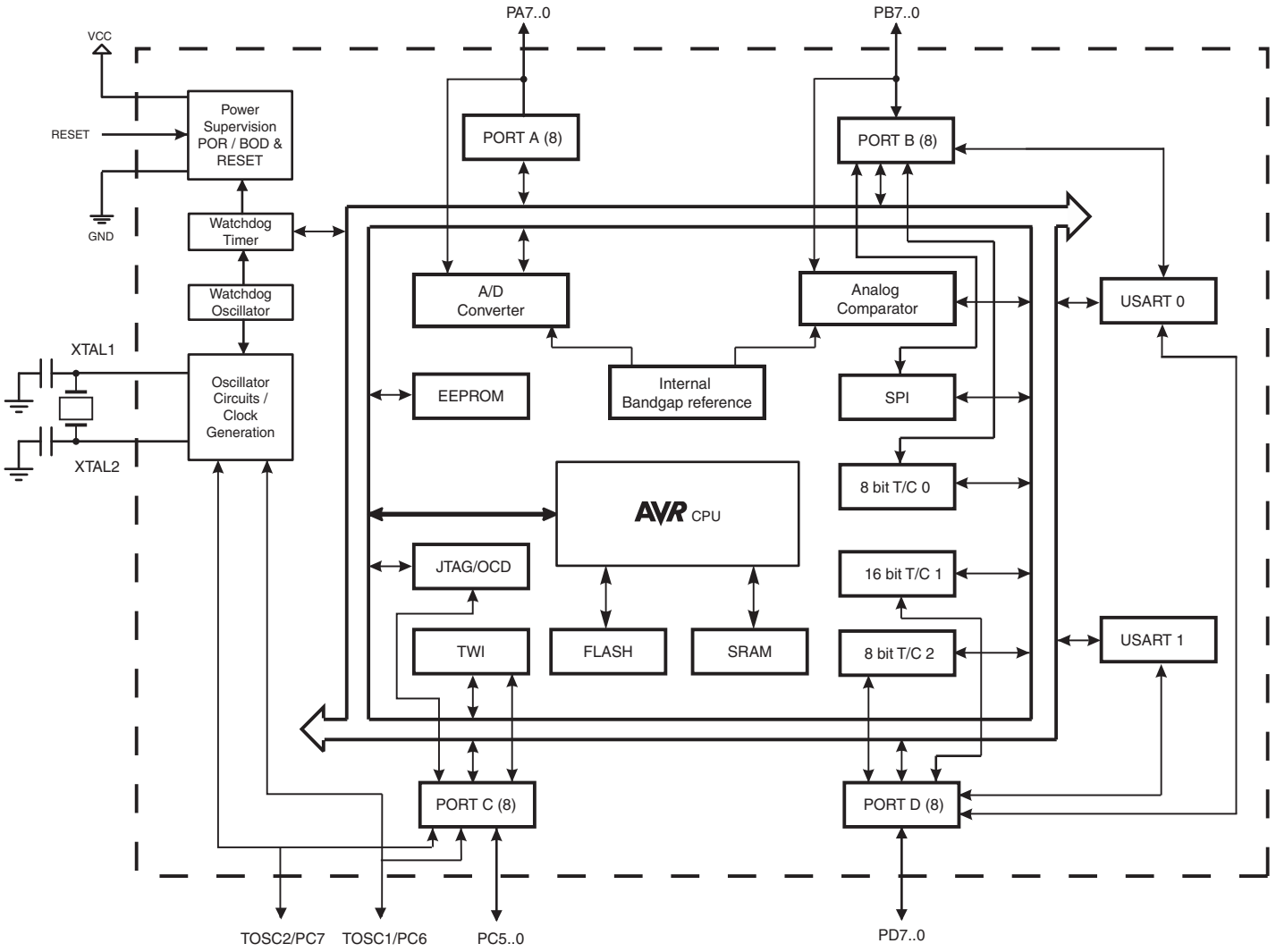
A1	PB5	**A7**	PD3	**A13**	PC4	**A19**	PA3
B1	PB6	**B6**	PD4	**B11**	PC5	**B16**	PA2
A2	PB7	**A8**	PD5	**A14**	PC6	**A20**	PA1
B2	$\overline{\text{RESET}}$	**B7**	PD6	**B12**	PC7	**B17**	PA0
A3	VCC	**A9**	PD7	**A15**	AVCC	**A21**	VCC
B3	GND	**B8**	VCC	**B13**	GND	**B18**	GND
A4	XTAL2	**A10**	GND	**A16**	AREF	**A22**	PB0
B4	XTAL1	**B9**	PC0	**B14**	PA7	**B19**	PB1
A5	PD0	**A11**	PC1	**A17**	PA6	**A23**	PB2
B5	PD1	**B10**	PC2	**B15**	PA5	**B20**	PB3
A6	PD2	**A12**	PC3	**A18**	PA4	**A24**	PB4

2. Overview

The ATmega164P/324P/644P is a low-power CMOS 8-bit microcontroller based on the AVR enhanced RISC architecture. By executing powerful instructions in a single clock cycle, the ATmega164P/324P/644P achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

2.1 Block Diagram

Figure 2-1. Block Diagram



The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU), allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

The ATmega164P/324P/644P provides the following features: 16K/32K/64K bytes of In-System Programmable Flash with Read-While-Write capabilities, 512B/1K/2K bytes EEPROM, 1K/2K/4K bytes SRAM, 32 general purpose I/O lines, 32 general purpose working registers, Real Time Counter (RTC), three flexible Timer/Counters with compare modes and PWM, 2 USARTs, a byte oriented 2-wire Serial Interface, a 8-channel, 10-bit ADC with optional differential input stage with programmable gain, programmable Watchdog Timer with Internal Oscillator, an SPI serial port, IEEE std. 1149.1 compliant JTAG test interface, also used for accessing the On-chip Debug system and programming and six software selectable power saving modes. The Idle mode stops the CPU while allowing the SRAM, Timer/Counters, SPI port, and interrupt system to continue functioning. The Power-down mode saves the register contents but freezes the Oscillator, disabling all other chip functions until the next interrupt or Hardware Reset. In Power-save mode, the asynchronous timer continues to run, allowing the user to maintain a timer base while the rest of the device is sleeping. The ADC Noise Reduction mode stops the CPU and all I/O modules except Asynchronous Timer and ADC, to minimize switching noise during ADC conversions. In Standby mode, the Crystal/Resonator Oscillator is running while the rest of the device is sleeping. This allows very fast start-up combined with low power consumption. In Extended Standby mode, both the main Oscillator and the Asynchronous Timer continue to run.

The device is manufactured using Atmel's high-density nonvolatile memory technology. The On-chip ISP Flash allows the program memory to be reprogrammed in-system through an SPI serial interface, by a conventional nonvolatile memory programmer, or by an On-chip Boot program running on the AVR core. The boot program can use any interface to download the application program in the application Flash memory. Software in the Boot Flash section will continue to run while the Application Flash section is updated, providing true Read-While-Write operation. By combining an 8-bit RISC CPU with In-System Self-Programmable Flash on a monolithic chip, the Atmel ATmega164P/324P/644P is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATmega164P/324P/644P AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

2.2 Comparison Between ATmega164P, ATmega324P and ATmega644P

Table 2-1. Differences between ATmega164P and ATmega644P

Device	Flash	EEPROM	RAM
ATmega164P	16 Kbyte	512 Bytes	1 Kbyte
ATmega324P	32 Kbyte	1 Kbyte	2 Kbyte
ATmega644P	64 Kbyte	2 Kbyte	4 Kbyte

2.3 Pin Descriptions

2.3.1 VCC

Digital supply voltage.

2.3.2 GND

Ground.

2.3.3 Port A (PA7:PA0)

Port A serves as analog inputs to the Analog-to-digital Converter.

Port A also serves as an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port A output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port A pins that are externally pulled low will source current if the pull-up resistors are activated. The Port A pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port A also serves the functions of various special features of the ATmega164P/324P/644P as listed on page 80.

2.3.4 Port B (PB7:PB0)

Port B is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port B output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port B pins that are externally pulled low will source current if the pull-up resistors are activated. The Port B pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port B also serves the functions of various special features of the ATmega164P/324P/644P as listed on page 82.

2.3.5 Port C (PC7:PC0)

Port C is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port C output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port C pins that are externally pulled low will source current if the pull-up resistors are activated. The Port C pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port C also serves the functions of the JTAG interface, along with special features of the ATmega164P/324P/644P as listed on page 85.

2.3.6 Port D (PD7:PD0)

Port D is an 8-bit bi-directional I/O port with internal pull-up resistors (selected for each bit). The Port D output buffers have symmetrical drive characteristics with both high sink and source capability. As inputs, Port D pins that are externally pulled low will source current if the pull-up resistors are activated. The Port D pins are tri-stated when a reset condition becomes active, even if the clock is not running.

Port D also serves the functions of various special features of the ATmega164P/324P/644P as listed on page 87.

2.3.7 $\overline{\text{RESET}}$

Reset input. A low level on this pin for longer than the minimum pulse length will generate a reset, even if the clock is not running. The minimum pulse length is given in ”System and Reset Characteristics” on page 331. Shorter pulses are not guaranteed to generate a reset.

2.3.8 XTAL1

Input to the inverting Oscillator amplifier and input to the internal clock operating circuit.

2.3.9 XTAL2

Output from the inverting Oscillator amplifier.

2.3.10 AVCC

AVCC is the supply voltage pin for Port A and the Analog-to-digital Converter. It should be externally connected to V_{CC}, even if the ADC is not used. If the ADC is used, it should be connected to V_{CC} through a low-pass filter.

2.3.11 AREF

This is the analog reference pin for the Analog-to-digital Converter.

3. Ordering Information

3.1 ATmega164P

Speed (MHz)[4]	Power Supply	Ordering Code[2]	Package[1]	Operational Range
10	1.8V - 5.5V	ATmega164PV-10AU ATmega164PV-10AUR[3] ATmega164PV-10PU ATmega164PV-10MU ATmega164PV-10MUR[3]	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	2.7V - 5.5V	ATmega164P-20AU ATmega164P-20AUR[3] ATmega164P-20PU ATmega164P-20MU ATmega164P-20MUR[3]	44A 44A 40P6 44M1 44M1	
10	1.8 - 5.5V	ATmega164PV-10AN ATmega164PV-10ANR[3] ATmega164PV-10PN	44A 44A 40P6	Extended (-40°C to 105°C)[5]
20	2.7 - 5.5V	ATmega164P-20AN ATmega164P-20ANR[3] ATmega164P-20PN ATmega164P-20MN ATmega164P-20MNR[3]	44A 44A 40P6 44M1 44M1	

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Tape & Reel.
4. For Speed vs. V_{CC} see ”Speed Grades” on page 329.
5. See characterization specifications at 105°C

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)

3.2 ATmega324P

Speed (MHz)[4]	Power Supply	Ordering Code[2]	Package[1]	Operational Range
10	1.8V - 5.5V	ATmega324PV-10AU ATmega324PV-10AUR[3] ATmega324PV-10PU ATmega324PV-10MU ATmega324PV-10MUR[3]	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	2.7V - 5.5V	ATmega324P-20AU ATmega324P-20AUR[3] ATmega324P-20PU ATmega324P-20MU ATmega324P-20MUR[3]	44A 44A 40P6 44M1 44M1	
10	1.8 - 5.5V	ATmega324PV-10AN ATmega324PV-10ANR[3] ATmega324PV-10PN ATmega324PV-10MN ATmega324PV-10MNR[3]	44A 44A 40P6 44M1 44M1	Extended (-40°C to 105°C)[5]
20	2.7 - 5.5V	ATmega324P-20AN ATmega324P-20ANR[3] ATmega324P-20PN ATmega324P-20MN ATmega324P-20MNR[3]	44A 44A 40P6 44M1 44M1	

Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Tape & Reel.
4. For Speed vs. V_{CC} see ”Speed Grades” on page 329.
5. See characterization specifications at 105°C

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm Body, lead pitch 0.50 mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)

3.3 ATmega644P

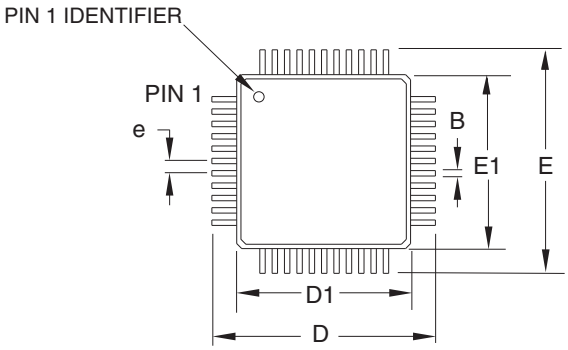
Speed (MHz)[4]	Power Supply	Ordering Code[2]	Package[1]	Operational Range
10	1.8V - 5.5V	ATmega644PV-10AU ATmega644PV-10AUR[3] ATmega644PV-10PU ATmega644PV-10MU ATmega644PV-10MUR[3]	44A 44A 40P6 44M1 44M1	Industrial (-40°C to 85°C)
20	2.7V - 5.5V	ATmega644P-20AU ATmega644P-20AUR[3] ATmega644P-20PU ATmega644P-20MU ATmega644P-20MUR[3]	44A 44A 40P6 44M1 44M1	
10	1.8 - 5.5V	ATmega644PV-10AN ATmega644PV-10ANR[3] ATmega644PV-10PN ATmega644PV-10MN ATmega644PV-10MNR[3]	44A 44A 40P6 44M1 44M1	Extended (-40°C to 105°C)[5]
20	2.7 - 5.5V	ATmega644P-20AN ATmega644P-20ANR[3] ATmega644P-20PN ATmega644P-20MN ATmega644P-20MNR[3]	44A 44A 40P6 44M1 44M1	

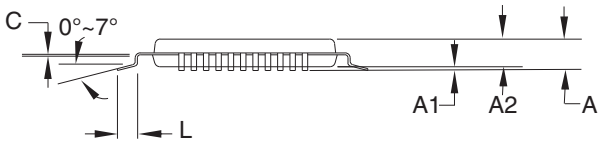
Notes:
1. This device can also be supplied in wafer form. Please contact your local Atmel sales office for detailed ordering information and minimum quantities.
2. Pb-free packaging, complies to the European Directive for Restriction of Hazardous Substances (RoHS directive). Also Halide free and fully Green.
3. Tape & Reel.
4. For Speed vs. V_{CC} see ”Speed Grades” on page 329.
5. See characterization specifications at 105°C

Package Type	
44A	44-lead, Thin (1.0mm) Plastic Gull Wing Quad Flat Package (TQFP)
40P6	40-pin, 0.600” Wide, Plastic Dual Inline Package (PDIP)
44M1	44-pad, 7 × 7 × 1.0mm body, lead pitch 0.50 mm, Thermally Enhanced Plastic Very Thin Quad Flat No-Lead (VQFN)

4. Packaging Information

4.1 44A





COMMON DIMENSIONS
(Unit of Measure = mm)

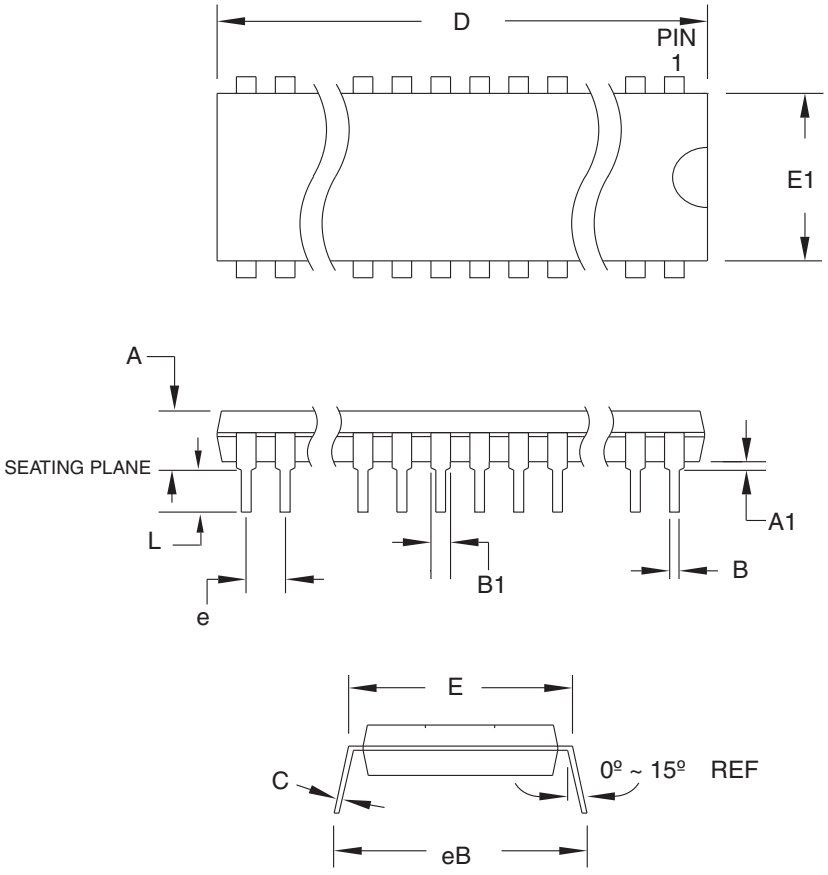
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	1.20	
A1	0.05	–	0.15	
A2	0.95	1.00	1.05	
D	11.75	12.00	12.25	
D1	9.90	10.00	10.10	Note 2
E	11.75	12.00	12.25	
E1	9.90	10.00	10.10	Note 2
B	0.30	–	0.45	
C	0.09	–	0.20	
L	0.45	–	0.75	
e	0.80 TYP			

Notes:
1. This package conforms to JEDEC reference MS-026, Variation ACB.
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side. Dimensions D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Lead coplanarity is 0.10mm maximum.

2010-10-20

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**44A,** 44-lead, 10 x 10mm body size, 1.0mm body thickness, 0.8 mm lead pitch, thin profile plastic quad flat package (TQFP)	44A	C

4.2 40P6



COMMON DIMENSIONS
(Unit of Measure = mm)

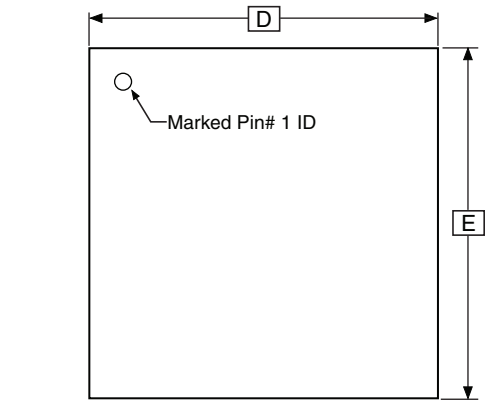
SYMBOL	MIN	NOM	MAX	NOTE
A	–	–	4.826	
A1	0.381	–	–	
D	52.070	–	52.578	Note 2
E	15.240	–	15.875	
E1	13.462	–	13.970	Note 2
B	0.356	–	0.559	
B1	1.041	–	1.651	
L	3.048	–	3.556	
C	0.203	–	0.381	
eB	15.494	–	17.526	
e	2.540 TYP			

Notes:
1. This package conforms to JEDEC reference MS-011, Variation AC.
2. Dimensions D and E1 do not include mold Flash or Protrusion.
   Mold Flash or Protrusion shall not exceed 0.25mm (0.010").

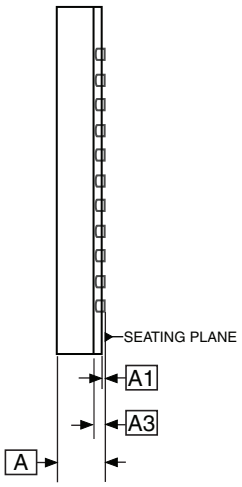
09/28/01

	TITLE	DRAWING NO.	REV.
2325 Orchard Parkway San Jose, CA 95131	**40P6**, 40-lead (0.600"/15.24mm Wide) Plastic Dual Inline Package (PDIP)	40P6	B

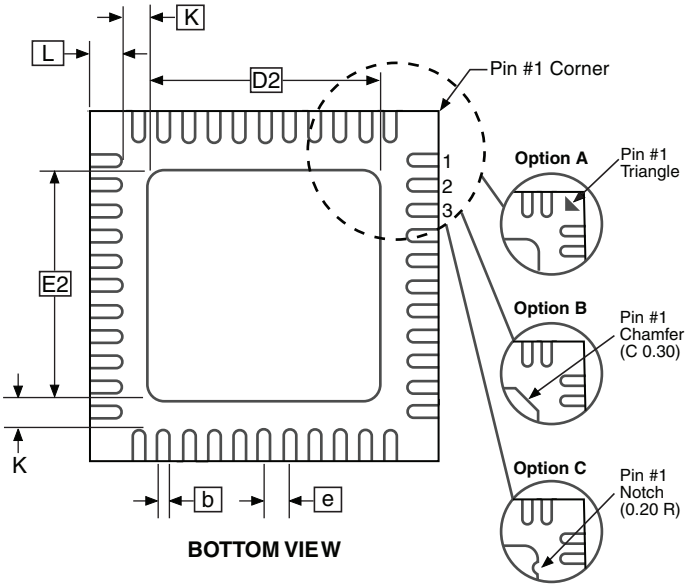
4.3 44M1



TOP VIEW



SIDE VIEW



BOTTOM VIEW

Note: JEDEC Standard MO-220, Fig. 1 (SAW Singulation) VKKD-3.

COMMON DIMENSIONS
(Unit of Measure = mm)

SYMBOL	MIN	NOM	MAX	NOTE
A	0.80	0.90	1.00	
A1	–	0.02	0.05	
A3		0.20 REF		
b	0.18	0.23	0.30	
D	6.90	7.00	7.10	
D2	5.00	5.20	5.40	
E	6.90	7.00	7.10	
E2	5.00	5.20	5.40	
e		0.50 BSC		
L	0.59	0.64	0.69	
K	0.20	0.26	0.41	

9/26/08

	TITLE	GPC	DRAWING NO.	REV.
Package Drawing Contact: packagedrawings@atmel.com	**44M1,** 44-pad, 7 x 7 x 1.0mm body, lead pitch 0.50mm, 5.20mm exposed pad, thermally enhanced plastic very thin quad flat no lead package (VQFN)	ZWS	44M1	H

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