Burr-Brown Products
from Texas Instruments

16-Bit, Quad Voltage Output Digital-to-Analog Converter

FEATURES

- **Low Glitch: 1nV-s (typ)**
- **Low Power: 18mW**
- **Unipolar or Bipolar Operation**
- **Settling Time: 12µs to 0.003%**
- **16-Bit Linearity and Monotonicity: –40°C to +85°C**
- **Programmable Reset to Mid-Scale or Zero-Scale**
- **Double-Buffered Data Inputs**
- **Internal Bandgap Voltage Reference**
- **Power-On Reset**
- **3V to 5V Logic Interface**

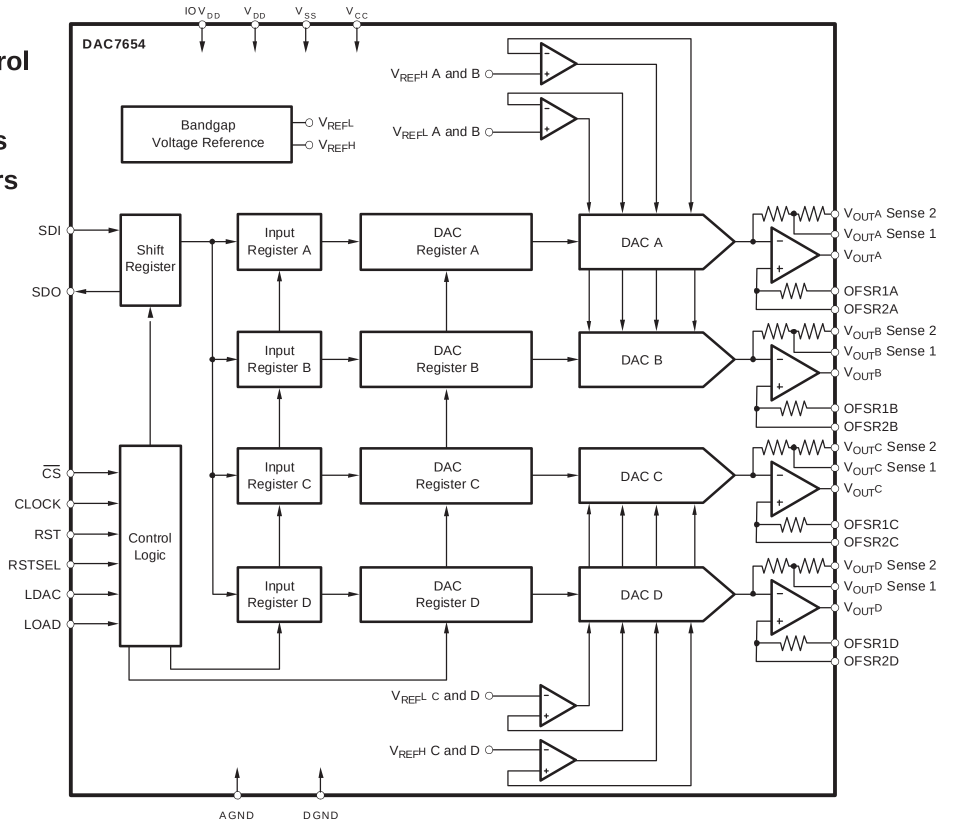
APPLICATIONS

- **Process Control**
- **Closed-Loop Servo-Control**
- **Motor Control**
- **Data Acquisition Systems**
- **DAC-per-Pin Programmers**

DESCRIPTION

The DAC7654 is a 16-bit, quad voltage output, digital-to-analog converter (DAC) with 16-bit monotonic performance over the specified temperature range. It accepts 24-bit serial input data, has double-buffered DAC input logic (allowing simultaneous update of all DACs), and provides a serial data output for daisy-chaining multiple DACs. Programmable asynchronous reset clears all registers to a mid-scale code of 8000h or to a zero-scale of 0000h. The DAC7654 can operate from a single +5V supply or from +5V and –5V supplies.

Low power and small size per DAC make the DAC7654 ideal for automatic test equipment, DAC-per-pin programmers, data acquisition systems, and closed-loop servo-control. The DAC7654 is available in an LQFP package and is specified for operation over the –40°C to +85°C temperature range.



This device has ESD-CDM sensitivity and special handling precautions must be taken.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ORDERING INFORMATION(1)

PRODUCT	PACKAGE−LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
DAC7654Y	LQFP−64	PM	−40°C to +85°C	DAC7654Y	DAC7654YT	Tape and Reel, 250
					DAC7654YR	Tape and Reel, 1500
DAC7654YB	LQFP−64	PM	−40°C to +85°C	DAC7654YB	DAC7654YBT	Tape and Reel, 250
					DAC7654YBR	Tape and Reel, 1500
DAC7654YC	LQFP−64	PM	−40°C to +85°C	DAC7654YC	DAC7654YCT	Tape and Reel, 250
					DAC7654YCR	Tape and Reel, 1500

(1) For the most current specification and package information, see the Package Ordering Addendum at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	DAC7654	UNIT
IOV_{DD}, V_{CC} and V_{DD} to V_{SS}	−0.3 to 11	V
IOV_{DD}, V_{CC} and V_{DD} to GND	−0.3 to 5.5	V
Digital Input Voltage to GND	−0.3 to V_{DD} + 0.3	V
Digital Output Voltage to GND	−0.3 to V_{DD} + 0.3	V
ESD-CDM	200	V
Maximum Junction Temperature	+150	°C
Operating Temperature Range	−40 to +85	°C
Storage Temperature Range	−65 to +125	°C
Lead Temperature (soldering, 10s)	+300	°C

(1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ELECTRICAL CHARACTERISTICS: V_{SS} = 0V

All specifications at $T_A = T_{MIN}$ to T_{MAX}, $IOV_{DD} = V_{DD} = V_{CC}$ = +5V, and V_{SS} = 0V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC7654Y			DAC7654YB			DAC7654YC			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Accuracy											
Linearity error			±3	±4		±2	±3		✻	✻	LSB
Linearity match			±4			±2			✻		LSB
Differential linearity error			±2	±3		±1	±2	−1		+2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			16			Bit
Unipolar zero error			±1	±5		✻	✻		✻	✻	mV
Unipolar zero error drift			5	10		✻	✻		✻	✻	ppm/°C
Full-scale error			±6	±20		±4	±12.5		✻	✻	mV
Full-scale error drift			7	15		✻	✻		✻	✻	ppm/°C
Unipolar zero matching	Channel-to-channel matching		±3	±7		±2	±5		✻	✻	mV
Full-Scale matching	Channel-to-channel matching		±4	±10		±2	±8		✻	✻	mV
Power-supply rejection ratio (PSRR)	At full-scale		10	100		✻	✻		✻	✻	ppm/V
Analog Output											
Voltage output	R_L = 10kΩ	0		2.5	✻		✻	✻		✻	V
Output current		−1.25		+1.25	✻		✻	✻		✻	mA
Maximum load capacitance	No oscillation		500			✻			✻		pF
Short-circuit current			±20			✻			✻		mA
Short-circuit duration	GND or V_{CC}		Indefinite			✻			✻		
Dynamic Performance											
Settling time	To ±0.003%, 2.5V output step		12	15		✻	✻		✻	✻	µs
Channel-to-channel crosstalk			0.5			✻			✻		LSB
Digital feedthrough			2			✻			✻		nV-s
Output noise voltage	f = 10kHz		130			✻			✻		nV/$\sqrt{\text{Hz}}$
DAC glitch	7FFFh to 8000h or 8000h to 7FFFh		1	5		✻	✻		✻	✻	nV-s
Digital Input											
V_{IH}		$0.7 \times IOV_{DD}$			✻			✻			V
V_{IL}				$0.3 \times IOV_{DD}$			✻			✻	V
I_{IH}				±10			✻			✻	µA
I_{IL}				±10			✻			✻	µA
Digital Output											
V_{OH}	I_{OH} = −0.8mA, IOV_{DD} = 5V	3.6	4.5		✻	✻		✻	✻		V
V_{OL}	I_{OL} = 1.6mA, IOV_{DD} = 5V		0.3	0.4		✻	✻		✻	✻	V
V_{OH}	I_{OH} = −0.4mA, IOV_{DD} = 3V	2.4	2.6		✻	✻		✻	✻		V
V_{OL}	I_{OL} = 0.8mA, IOV_{DD} = 3V		0.3	0.4		✻	✻		✻	✻	V
Power Supply											
V_{DD}		+4.75	+5.0	+5.25	✻	✻	✻	✻	✻	✻	V
IOV_{DD}		+2.7	+5.0	+5.25	✻	✻	✻	✻	✻	✻	V
V_{CC}		+4.75	+5.0	+5.25	✻	✻	✻	✻	✻	✻	V
V_{SS}		0	0	0	✻	✻	✻	✻	✻	✻	V
I_{CC}			3.5	5		✻	✻		✻	✻	mA
I_{DD}			50			✻			✻		µA
$I(IOV_{DD})$			50			✻			✻		µA
Power			18	25		✻	✻		✻		mW
Temperature Range											
Specified performance		−40		+85	✻		✻	✻		✻	°C

✻ specifications same as the grade to the left

ELECTRICAL CHARACTERISTICS: V_{SS} = −5V

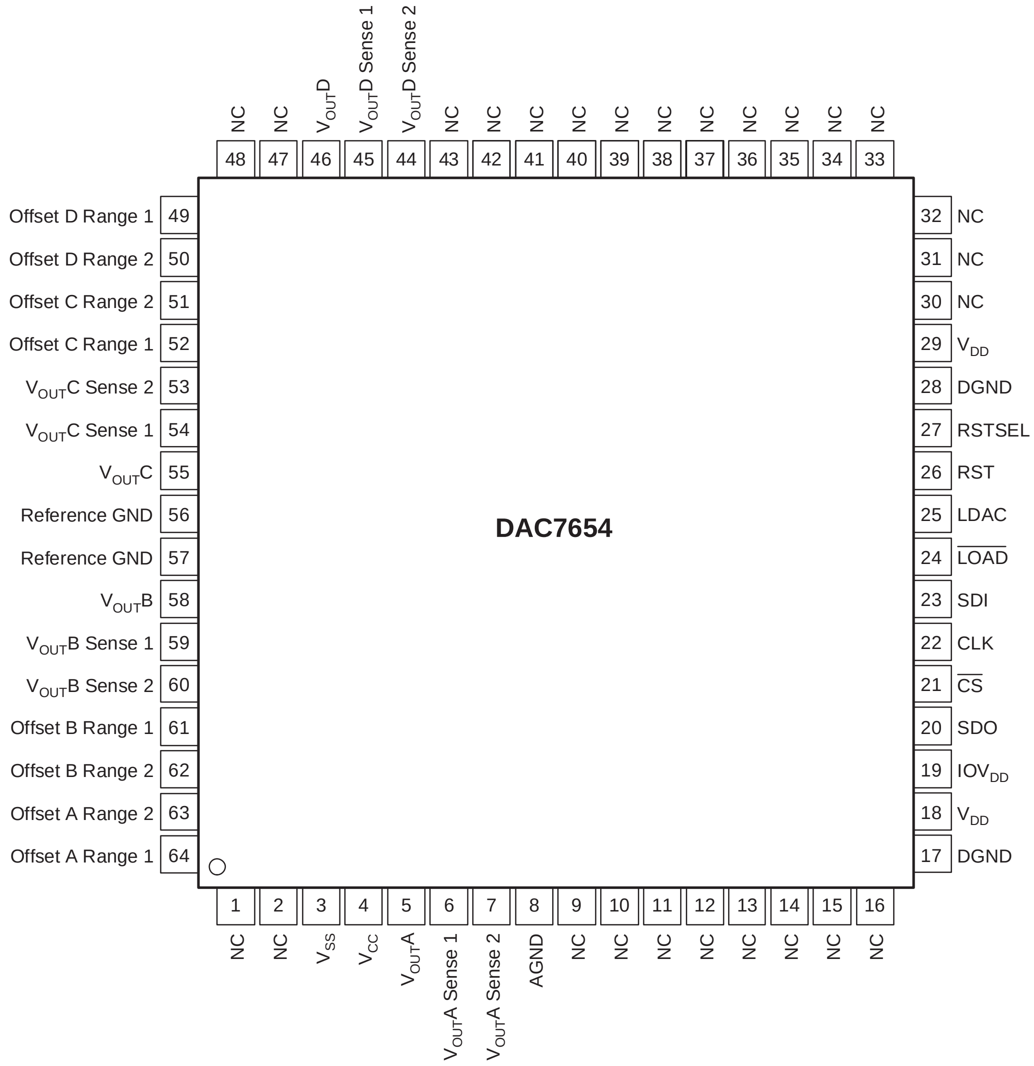
All specifications at T_A = T_{MIN} to T_{MAX}, IOV_{DD} = V_{DD} = V_{CC} = +5V, and V_{SS} = −5V, unless otherwise noted.

PARAMETER	TEST CONDITIONS	DAC7654Y			DAC7654YB			DAC7654YC			UNIT
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Accuracy											
Linearity error			±3	±4		±2	±3		✻	✻	LSB
Linearity match			±4			±2			✻		LSB
Differential linearity error			±2	±3		±1	±2	−1		+2	LSB
Monotonicity, T_{MIN} to T_{MAX}		14			15			16			Bit
Bipolar zero error			±1	±5		✻	✻		✻	✻	mV
Bipolar zero error drift			5	10		✻	✻		✻	✻	ppm/°C
Full-scale error			±6	±20		±4	±12.5		✻	✻	mV
Full-scale error drift			7	15		✻	✻		✻	✻	ppm/°C
Bipolar zero matching	Channel-to-channel matching		±3	±7		±2	±5		✻	✻	mV
Full-Scale matching	Channel-to-channel matching		±4	±10		±2	±8		✻	✻	mV
Power-supply rejection ratio (PSRR)	At full-scale		10	100		✻	✻		✻	✻	ppm/V
Analog Output											
Voltage output	R_L = 10kΩ	−2.5		+2.5	✻		✻	✻		✻	V
Output current		−1.25		+1.25	✻		✻	✻		✻	mA
Maximum load capacitance	No oscillation		500			✻			✻		pF
Short-circuit current			−15, +30			✻			✻		mA
Short-circuit duration	GND or V_{CC} or V_{SS}		Indefinite			✻			✻		
Dynamic Performance											
Settling time	To ±0.003%, 5V output step		12	15		✻	✻		✻	✻	µs
Channel-to-channel crosstalk			0.5			✻			✻		LSB
Digital feedthrough			2			✻			✻		nV-s
Output noise voltage	f = 10kHz		200			✻			✻		$nV/\sqrt{Hz}$
DAC glitch	7FFFh to 8000h or 8000h to 7FFFh		2	7		✻	✻		✻	✻	nV-s
Digital Input											
V_{IH}		$0.7 \times IOV_{DD}$			✻			✻			V
V_{IL}				$0.3 \times IOV_{DD}$			✻			✻	V
I_{IH}				±10			✻			✻	µA
I_{IL}				±10			✻			✻	µA
Digital Output											
V_{OH}	I_{OH} = −0.8mA, IOV_{DD} = 5V	3.6	4.5		✻	✻		✻	✻		V
V_{OL}	I_{OL} = 1.6mA, IOV_{DD} = 5V		0.3	0.4		✻	✻		✻	✻	V
V_{OH}	I_{OH} = −0.4mA, IOV_{DD} = 3V	2.4	2.6		✻	✻		✻	✻		V
V_{OL}	I_{OL} = 0.8mA, IOV_{DD} = 3V		0.3	0.4		✻	✻		✻	✻	V
Power Supply											
V_{DD}		+4.75	+5.0	+5.25	✻	✻	✻	✻	✻	✻	V
IOV_{DD}		+2.7	+5.0	+5.25	✻	✻	✻	✻	✻	✻	V
V_{CC}		+4.75	+5.0	+5.25	✻	✻	✻	✻	✻	✻	V
V_{SS}		−5.25	−5.0	−4.75	✻	✻	✻	✻	✻	✻	V
I_{CC}			4	5.5		✻	✻		✻	✻	mA
I_{DD}			50			✻			✻		µA
$I(IOV_{DD})$			50			✻			✻		µA
I_{SS}		−3.5	−2.0		✻	✻		✻	✻		mA
Power			30	45		✻	✻		✻		mW
Temperature Range											
Specified performance		−40		+85	✻		✻	✻		✻	°C

✻ specifications same as the grade to the left

PIN ASSIGNMENTS

LQFP PACKAGE
(TOP VIEW)



Terminal Functions

PIN	NAME	DESCRIPTION
1	NC	No Connection
2	NC	No Connection
3	V_{SS}	Analog –5V power supply or 0V single supply
4	V_{CC}	Analog +5V power supply
5	V_{OUT}A	DAC A output voltage
6	V_{OUT}A Sense 1	Connect to V_{OUT}A for unipolar mode
7	V_{OUT}A Sense 2	Connect to V_{OUT}A for bipolar mode
8	AGND	Analog ground
9	NC	No connection
10	NC	No connection
11	NC	No connection
12	NC	No connection
13	NC	No connection
14	NC	No connection
15	NC	No connection
16	NC	No connection
17	DGND	Digital ground
18	V_{DD}	Digital +5V power supply
19	IOV_{DD}	Interface power supply
20	SDO	Serial data output
21	CS	Chip select, active low
22	CLK	Data clock input
23	SDI	Serial data input
24	LOAD	DAC input register load control, active low
25	LDAC	DAC register load control, rising edge triggered
26	RST	Reset, rising edge triggered. Depending on the state of RSTSEL, the DAC registers are set to either mid-scale or zero.
27	RSTSEL	Reset select. Determines the action of RST. If high, an RST command sets the DAC registers to mid-scale (8000h). If low, an RST command sets the DAC registers to zero (0000h).
28	DGND	Digital ground
29	V_{DD}	Digital +5V power supply
30	NC	No connection
31	NC	No connection
32	NC	No connection
33	NC	No connection
34	NC	No connection
35	NC	No connection

PIN	NAME	DESCRIPTION
36	NC	No connection
37	NC	No connection
38	NC	No connection
39	NC	No connection
40	NC	No connection
41	NC	No connection
42	NC	No connection
43	NC	No connection
44	V_{OUT}D Sense 2	Connect to V_{OUT}D for bipolar mode
45	V_{OUT}D Sense 1	Connect to V_{OUT}D for unipolar mode
46	V_{OUT}D	DAC D output
47	NC	No connection
48	NC	No connection
49	Offset D Range 1	Connect to Offset D Range 2 for unipolar mode
50	Offset D Range 2	Connect to Offset D Range 1 for unipolar mode
51	Offset C Range 2	Connect to Offset C Range 1 for unipolar mode
52	Offset C Range 1	Connect to Offset C Range 2 for unipolar mode
53	V_{OUT}C Sense 2	Connect to V_{OUT}C for bipolar mode
54	V_{OUT}C Sense 1	Connect to V_{OUT}C for unipolar mode
55	V_{OUT}C	DAC C output
56	REF GND	Reference ground
57	REF GND	Reference ground
58	V_{OUT}B	DAC B output
59	V_{OUT}B Sense 1	Connect to V_{OUT}B for unipolar mode
60	V_{OUT}B Sense 2	Connect to V_{OUT}B for bipolar mode
61	Offset B Range 1	Connect to Offset B Range 2 for unipolar mode
62	Offset B Range 2	Connect to Offset B Range 1 for unipolar mode
63	Offset A Range 2	Connect to Offset A Range 1 for unipolar mode
64	Offset A Range 1	Connect to Offset A Range 2 for unipolar mode

TYPICAL CHARACTERISTICS: V_{SS} = 0V

All specifications at T_A = 25°C, $IOV_{DD} = V_{DD} = V_{CC}$ = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

+25°C

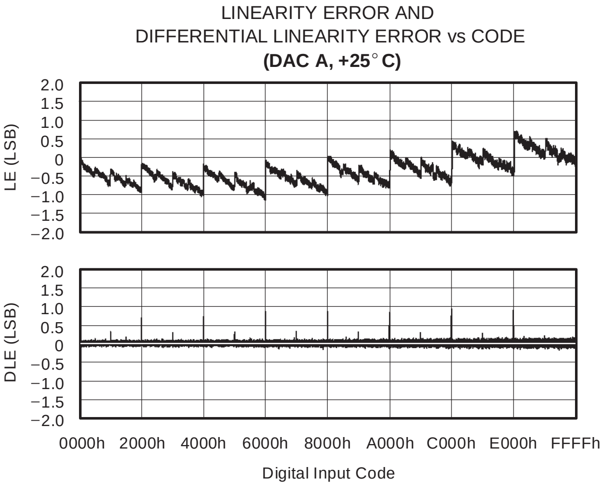


Figure 1

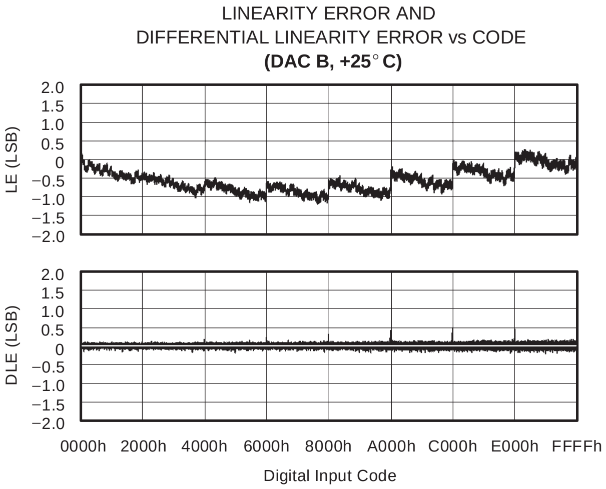


Figure 2

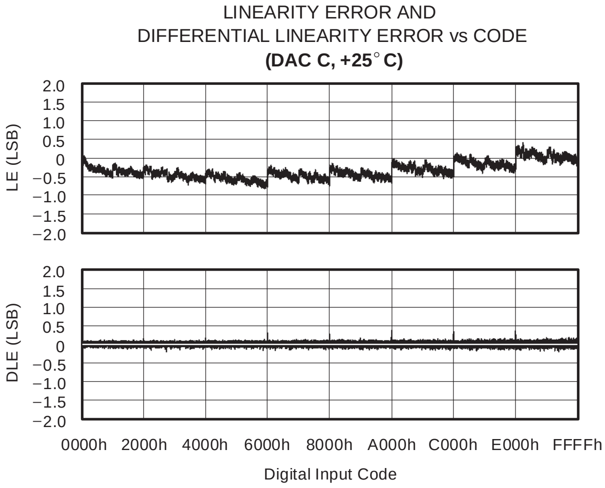


Figure 3

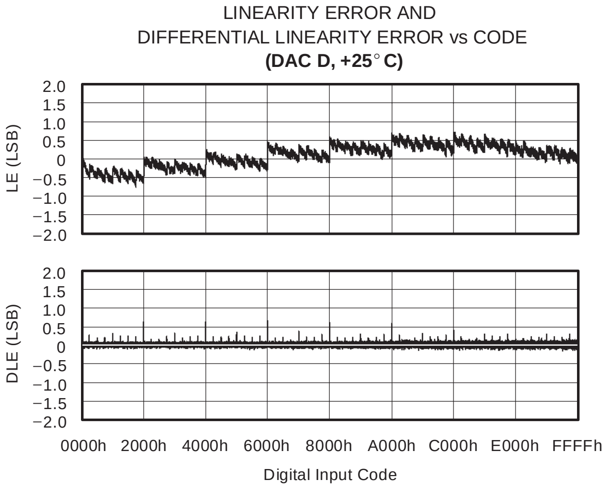


Figure 4

TYPICAL CHARACTERISTICS: V_{SS} = 0V (continued)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

+85°C

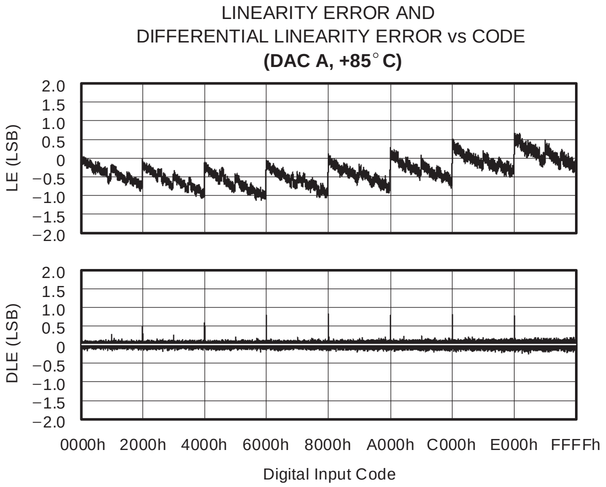


Figure 5

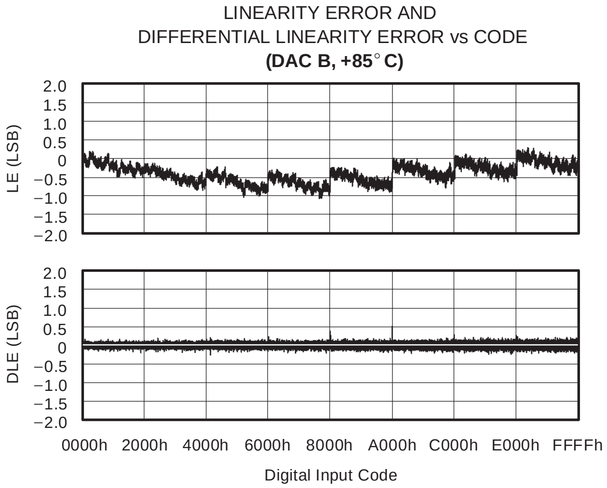
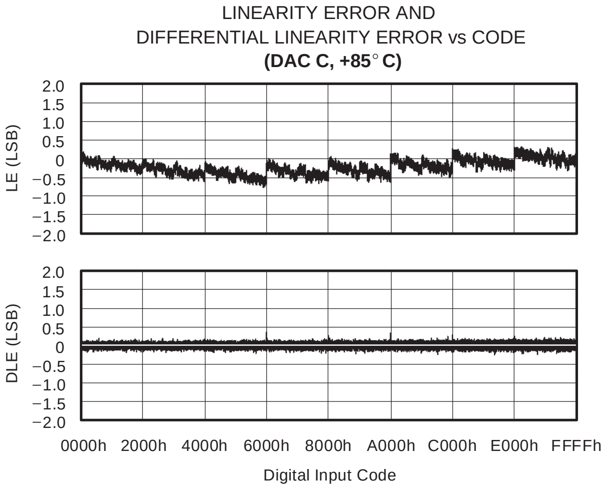


Figure 6



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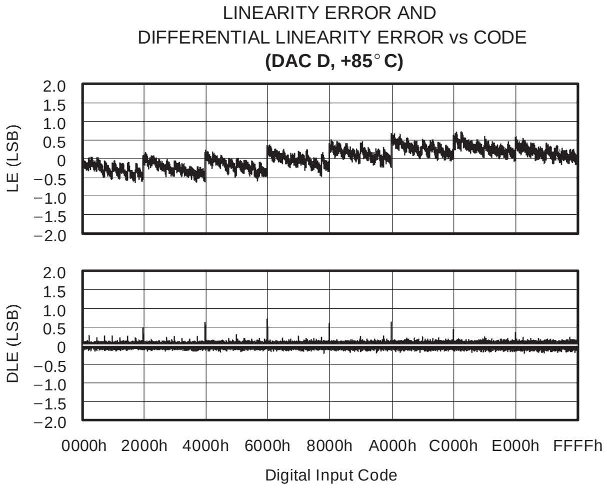

Figure 8

TYPICAL CHARACTERISTICS: V_{SS} = 0V (continued)

All specifications at T_A = 25°C, $IOV_{DD} = V_{DD} = V_{CC}$ = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

−40°C

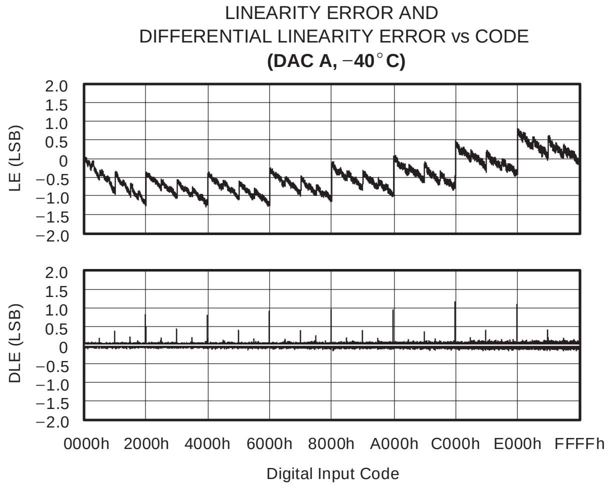

Figure 9

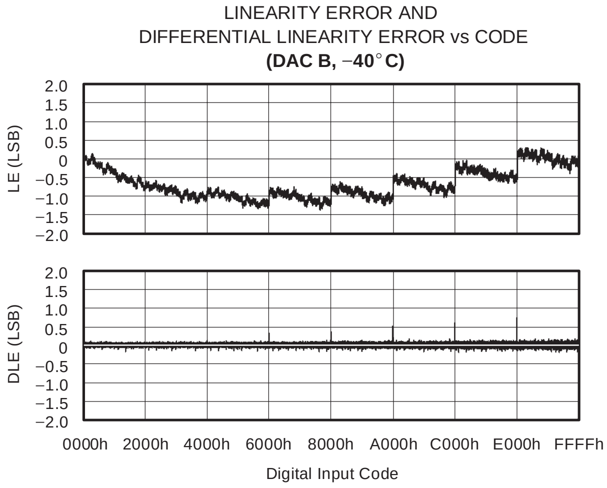

Figure 10

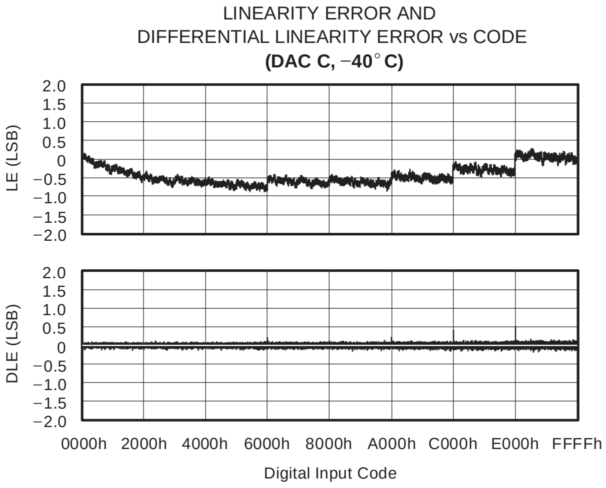

Figure 11

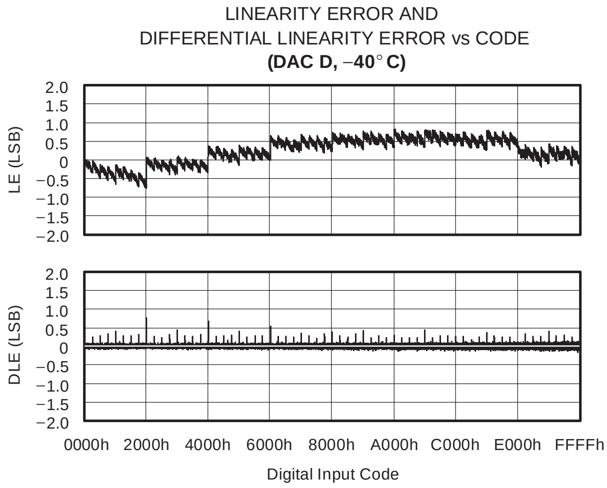

Figure 12

TYPICAL CHARACTERISTICS: V_{SS} = 0V (continued)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

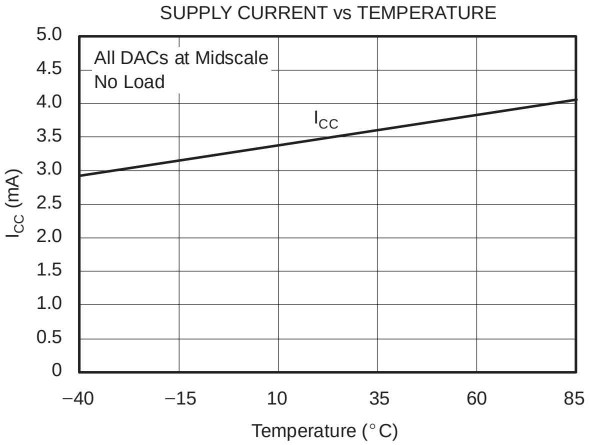

Figure 13

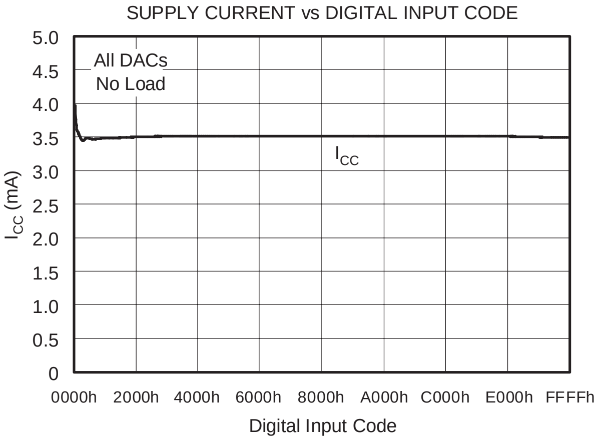

Figure 14

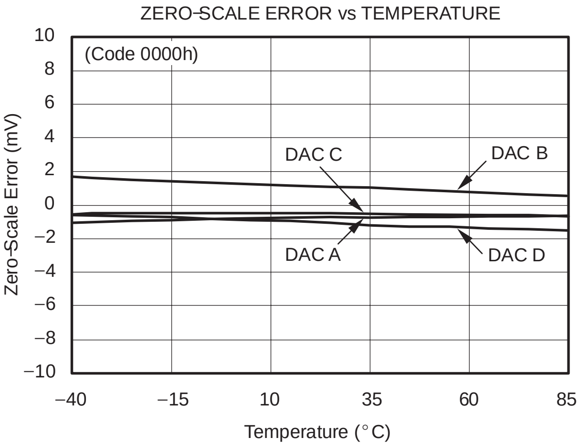

Figure 15

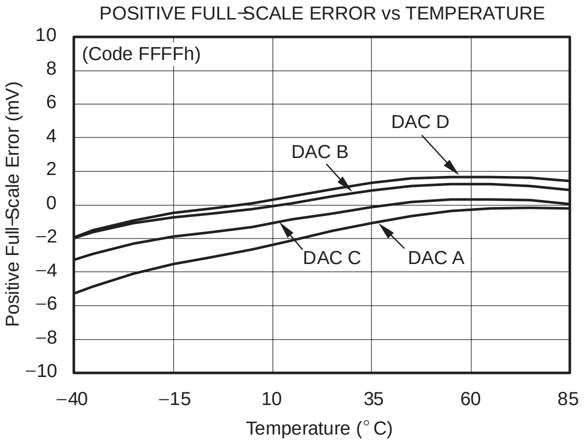

Figure 16

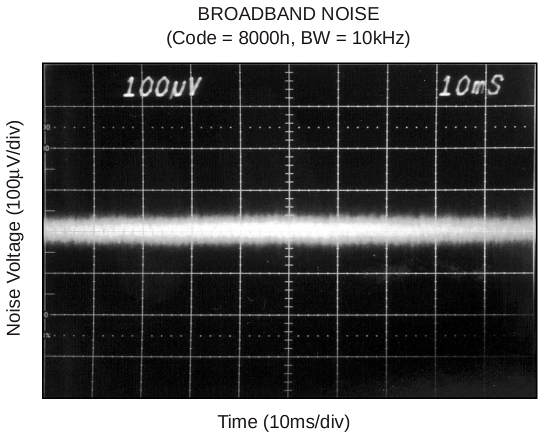

Figure 17

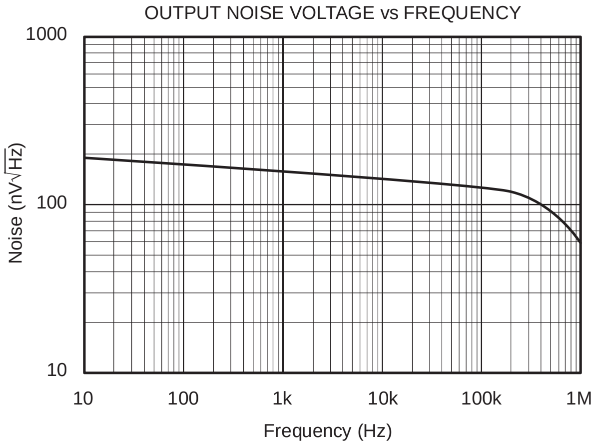

Figure 18

TYPICAL CHARACTERISTICS: V_{SS} = 0V (continued)

All specifications at T_A = 25°C, $IOV_{DD} = V_{DD} = V_{CC}$ = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

SETTLING TIME
(0V to +2.5V)

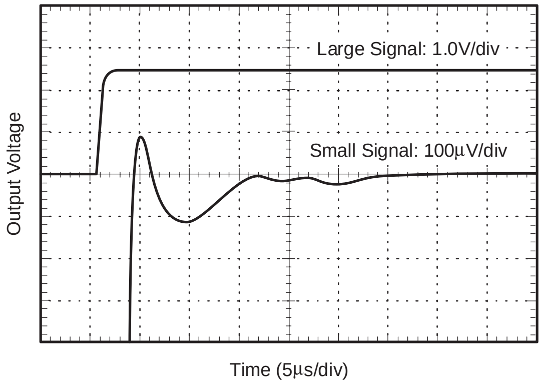

Figure 19

SETTLING TIME
(+2.5V to 39mV)

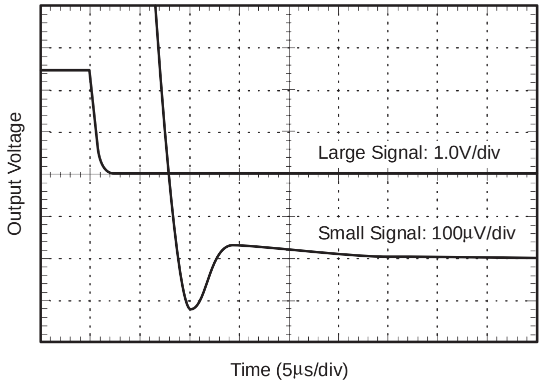

Figure 20

MIDSCALE GLITCH PERFORMANCE
CODE 7FFFh to 8000h

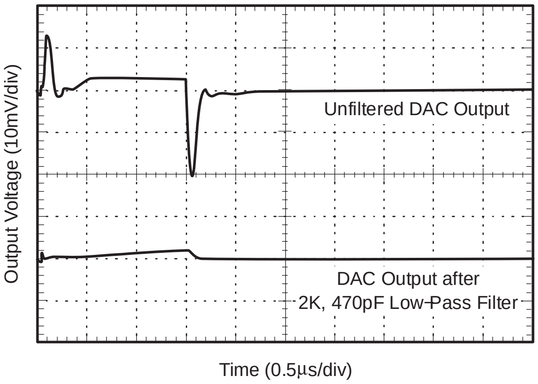

Figure 21

MIDSCALE GLITCH PERFORMANCE
CODE 8000h to 7FFFh

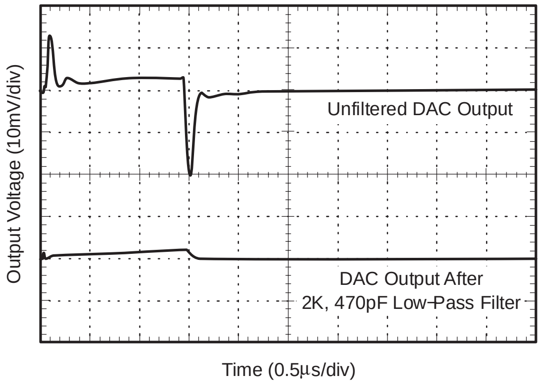

Figure 22

OVERSHOOT FOR TRANSITION OF 100 CODES
CODE 32750 to 32850

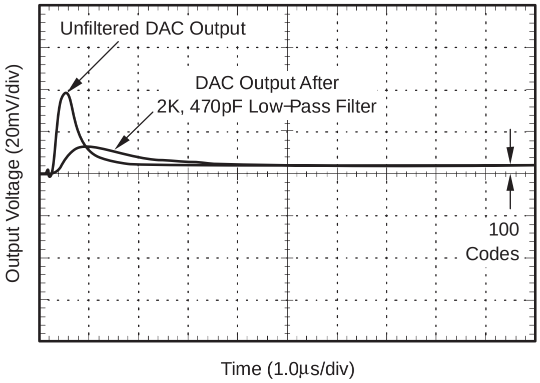

Figure 23

OVERSHOOT FOR TRANSITION OF 100 CODES
CODE 32850 to 32750

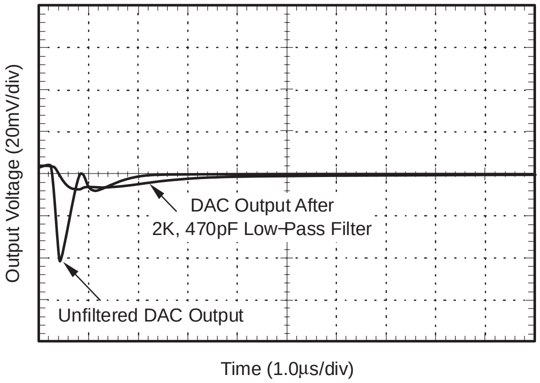

Figure 24

TYPICAL CHARACTERISTICS: V_{SS} = 0V (continued)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = 0V, representative unit, unless otherwise noted.

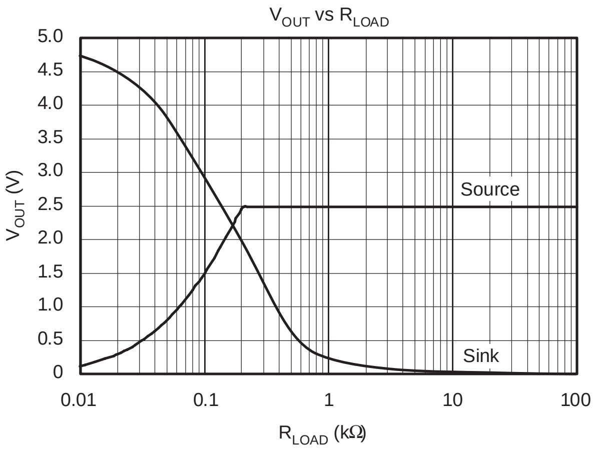

Figure 25

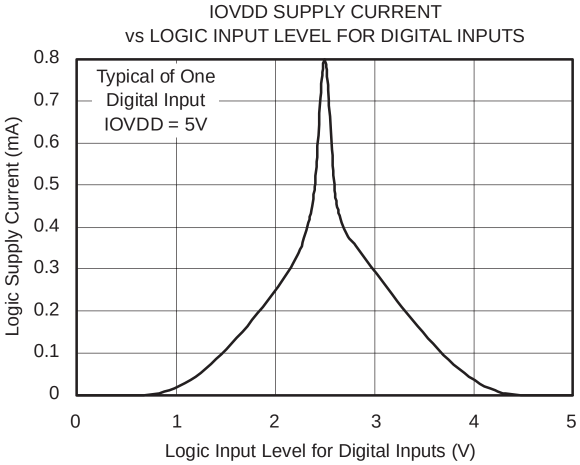

Figure 26

TYPICAL CHARACTERISTICS: V_{SS} = −5V

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

+25°C

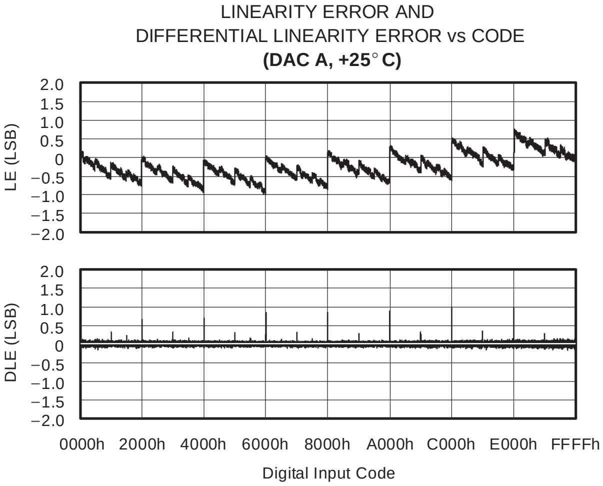

Figure 27

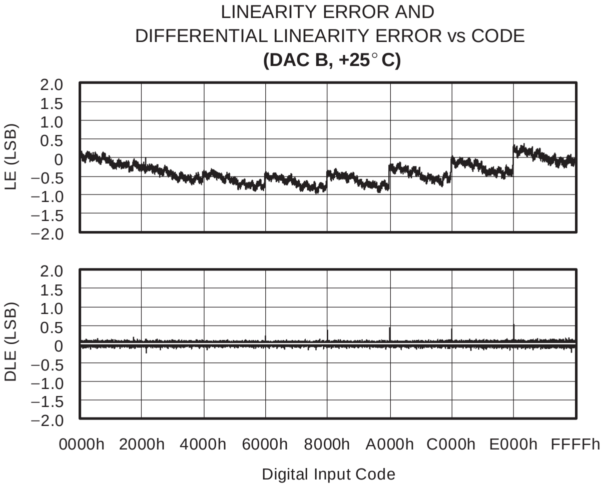

Figure 28

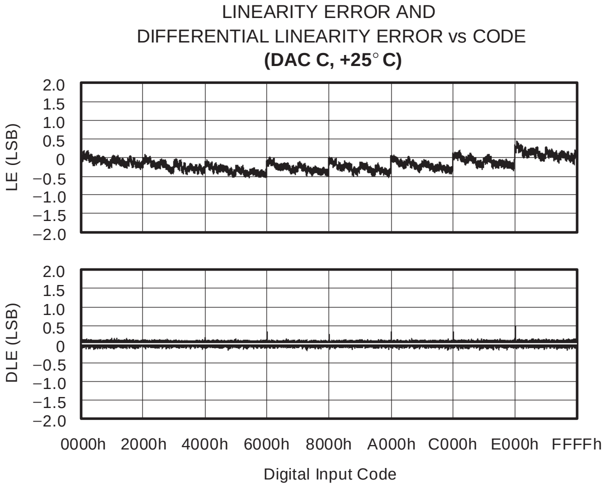

Figure 29

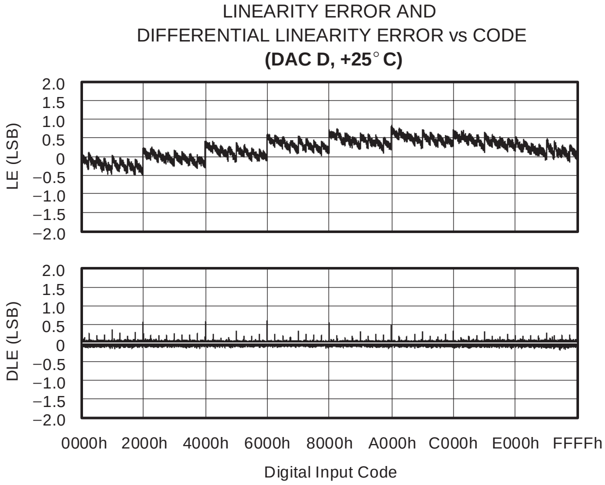

Figure 30

TYPICAL CHARACTERISTICS: V_{SS} = −5V (continued)

All specifications at T_A = 25°C, $IOV_{DD} = V_{DD} = V_{CC}$ = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

+85°C

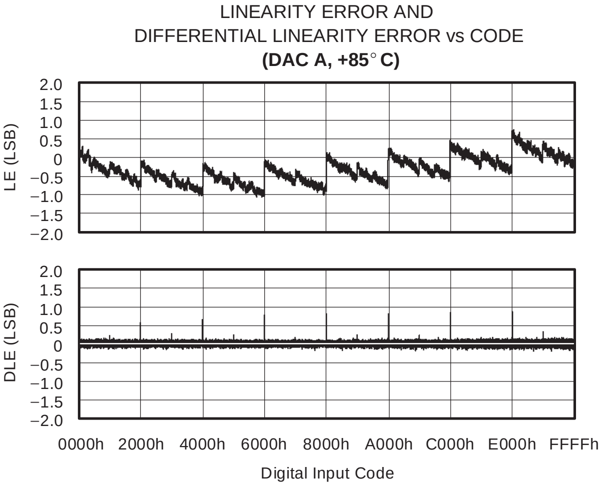

Figure 31

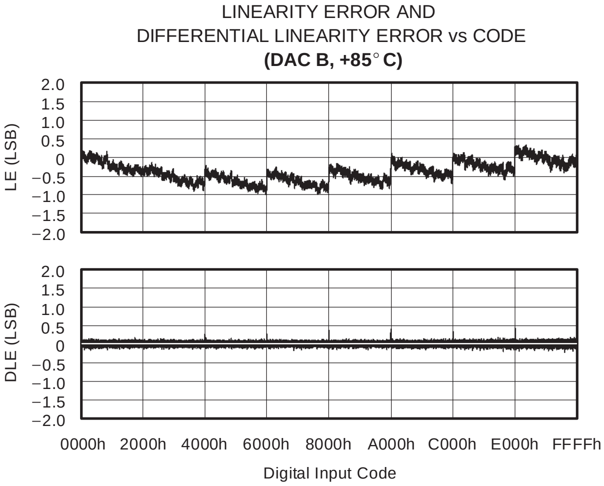

Figure 32

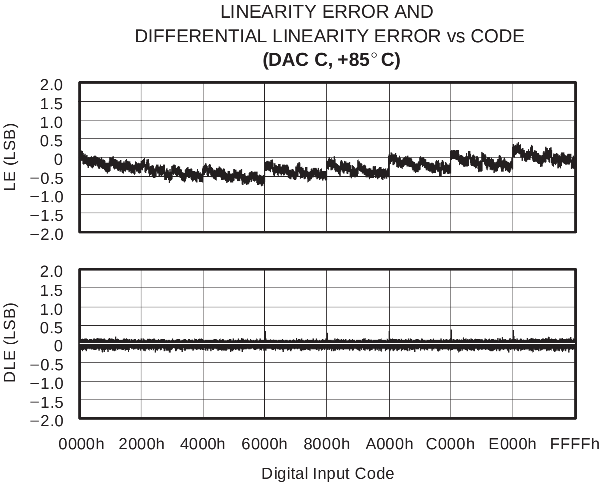

Figure 33

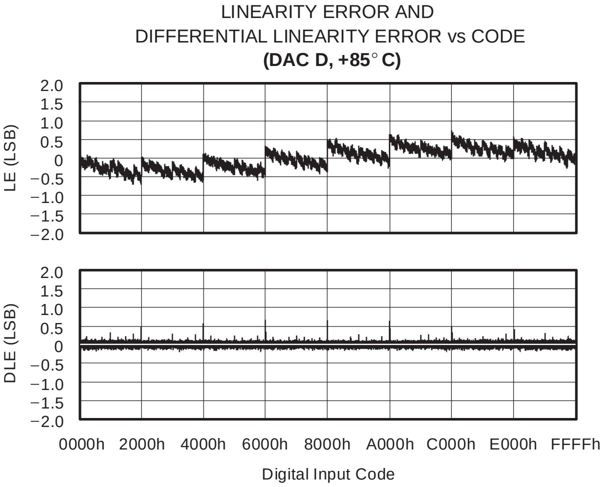

Figure 34

TYPICAL CHARACTERISTICS: V_{SS} = −5V (continued)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

−40°C

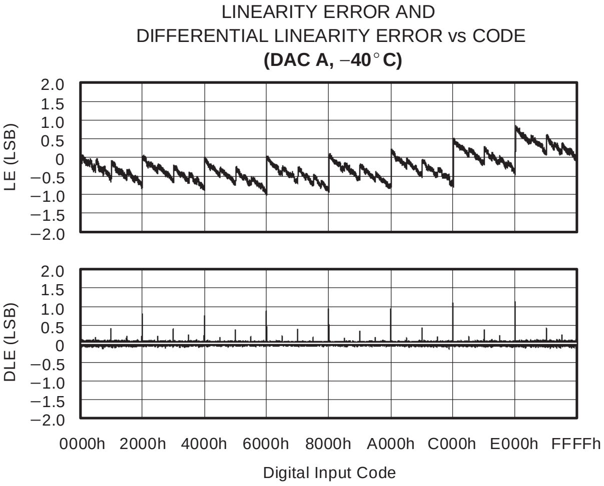

Figure 35

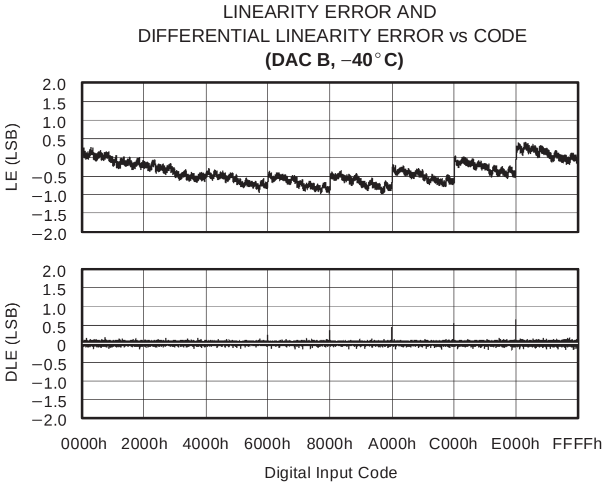

Figure 36

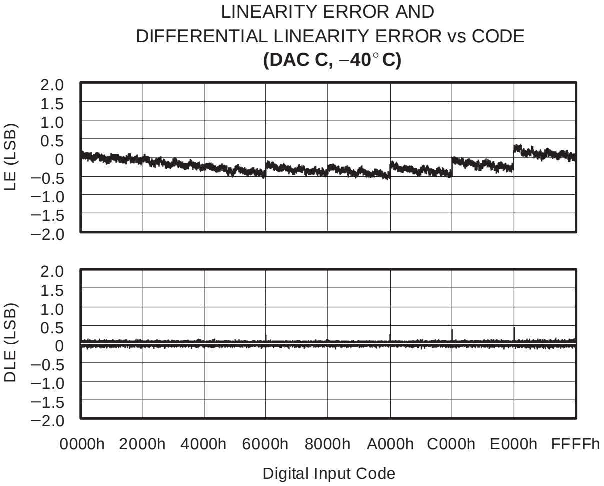

Figure 37

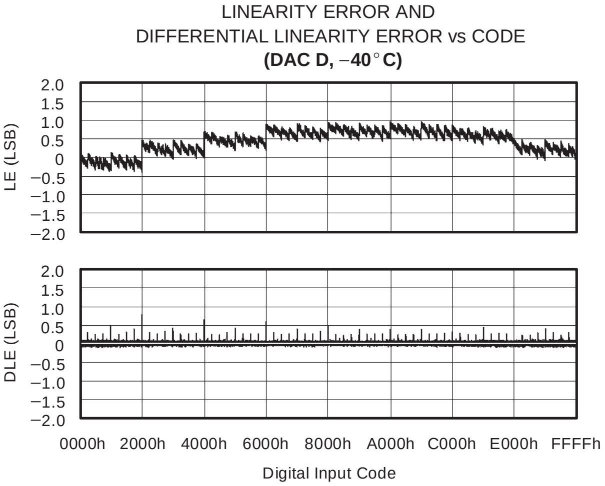

Figure 38

TYPICAL CHARACTERISTICS: V_{SS} = −5V (continued)

All specifications at T_A = 25°C, $IOV_{DD} = V_{DD} = V_{CC}$ = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

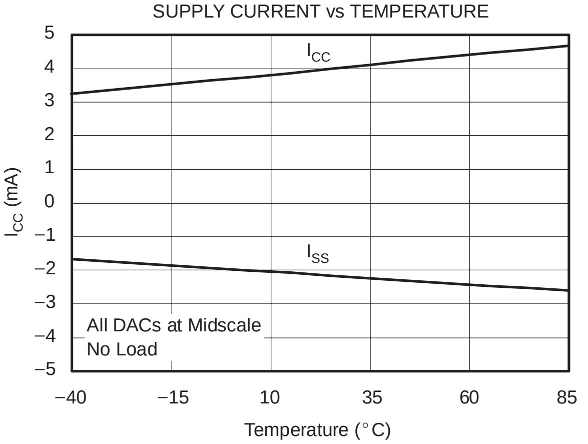

Figure 39

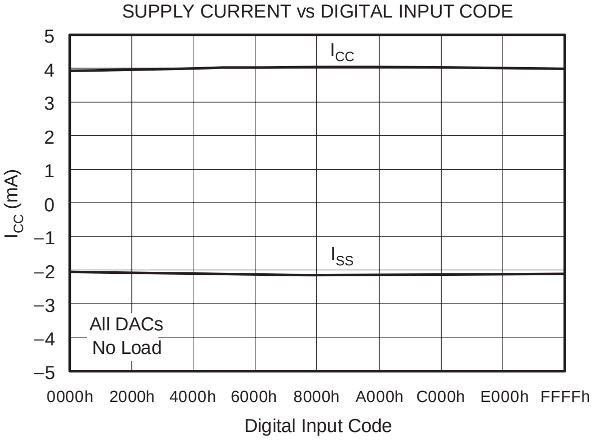

Figure 40

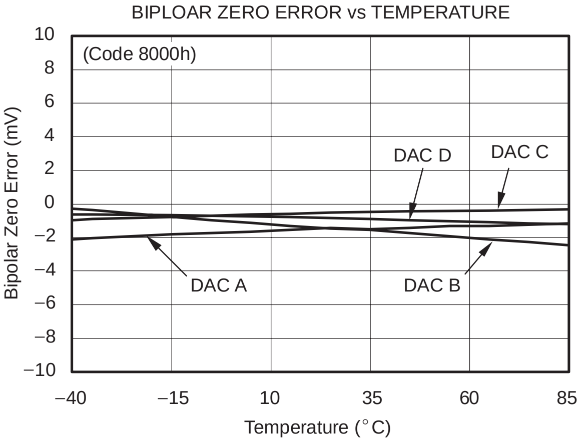

Figure 41

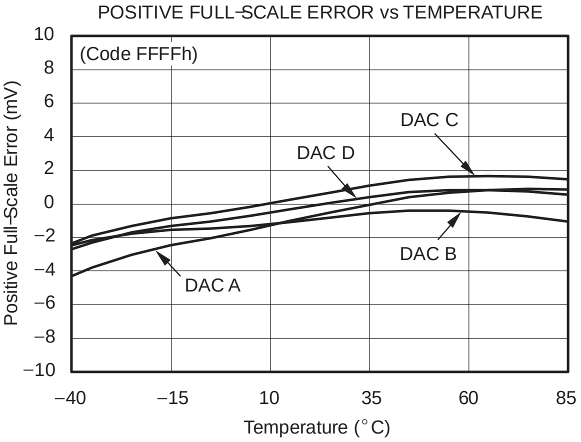

Figure 42

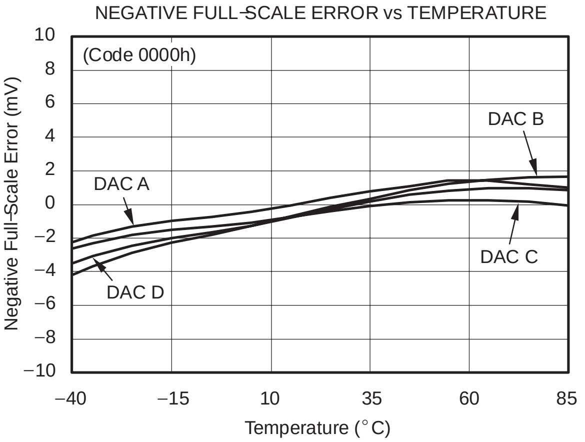

Figure 43

TYPICAL CHARACTERISTICS: V_{SS} = −5V (continued)

All specifications at T_A = 25°C, IOV_{DD} = V_{DD} = V_{CC} = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

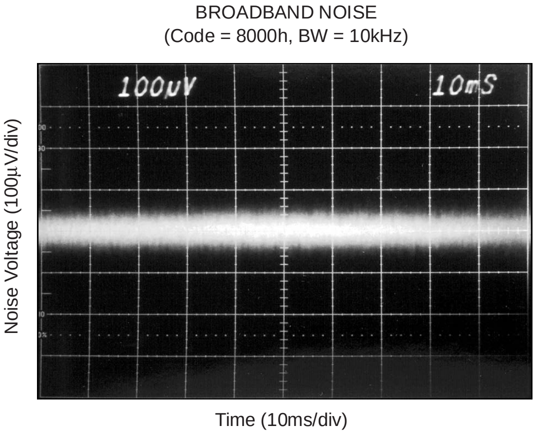

Figure 44

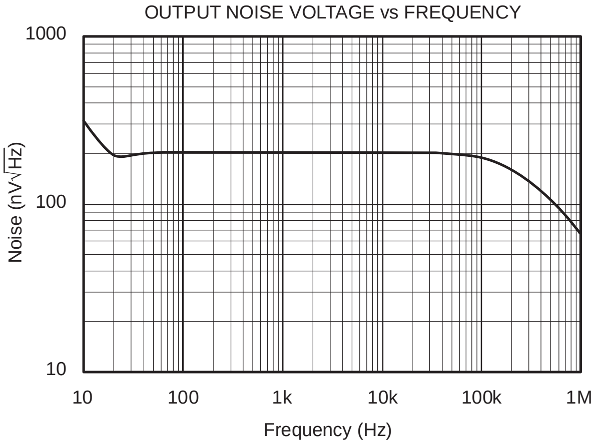

Figure 45

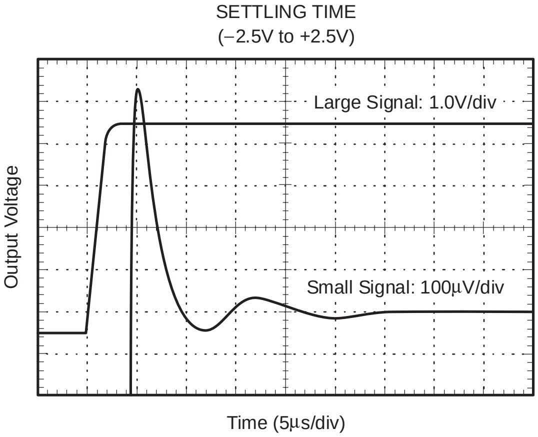

Figure 46

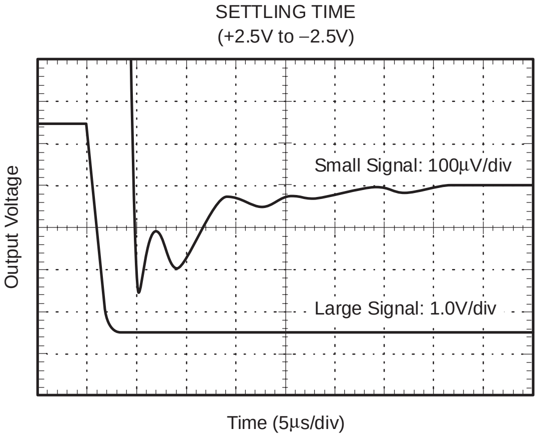

Figure 47

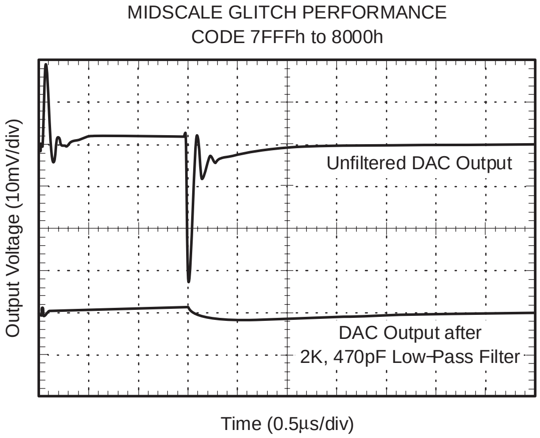

Figure 48

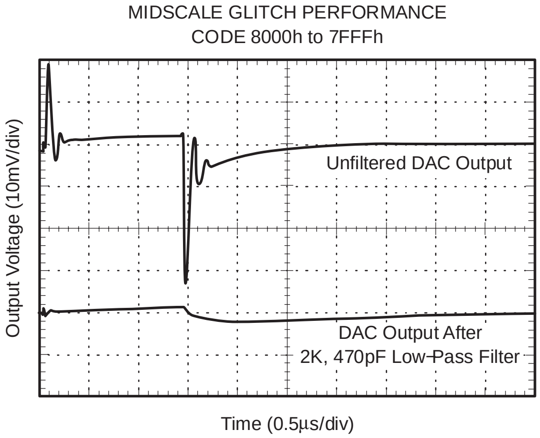

Figure 49

TYPICAL CHARACTERISTICS: V_{SS} = −5V (continued)

All specifications at T_A = 25°C, $IOV_{DD} = V_{DD} = V_{CC}$ = +5V, V_{SS} = −5V, representative unit, unless otherwise noted.

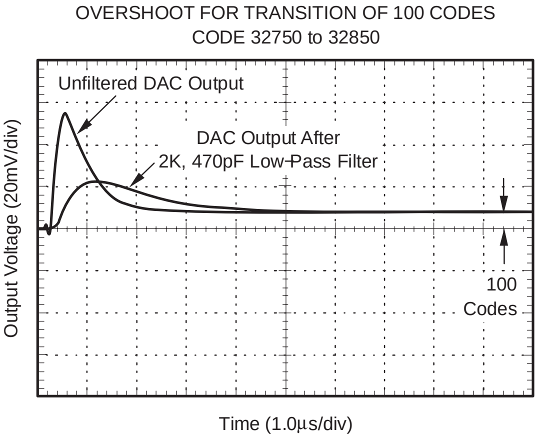

Figure 50

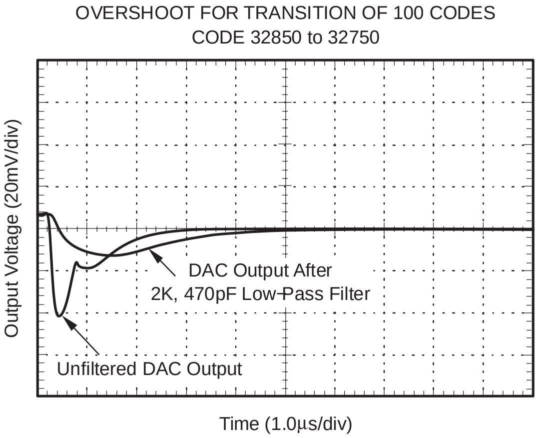

Figure 51

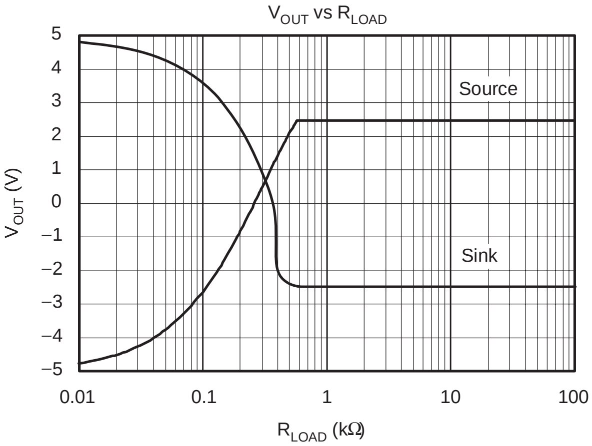

Figure 52

THEORY OF OPERATION

The DAC7654 is a quad voltage output, 16-bit DAC. The architecture is an R−2R ladder configuration with the three most significant bits (MSBs) segmented, followed by an operational amplifier that serves as a buffer. Each DAC has its own R−2R ladder network, segmented MSBs, and output op amp, as shown in Figure 53. The minimum voltage output (zero-scale) and maximum voltage output (full-scale) are set by the internal voltage references and the resistors associated with the output operational amplifier.

The digital input is a 24-bit serial word that contains a 2-bit address code for selecting one of four DACs, a quick load bit, five unused bits, and the 16-bit DAC code (MSB first). The converters can be powered from either a single +5V supply or a dual ±5V supply. The device offers a reset function that immediately sets all DAC output voltages and DAC registers to mid-scale (code 8000h) or to zero-scale (code 0000h). See Figure 54 and Figure 55 for basic single- and dual-supply operation of the DAC7654.

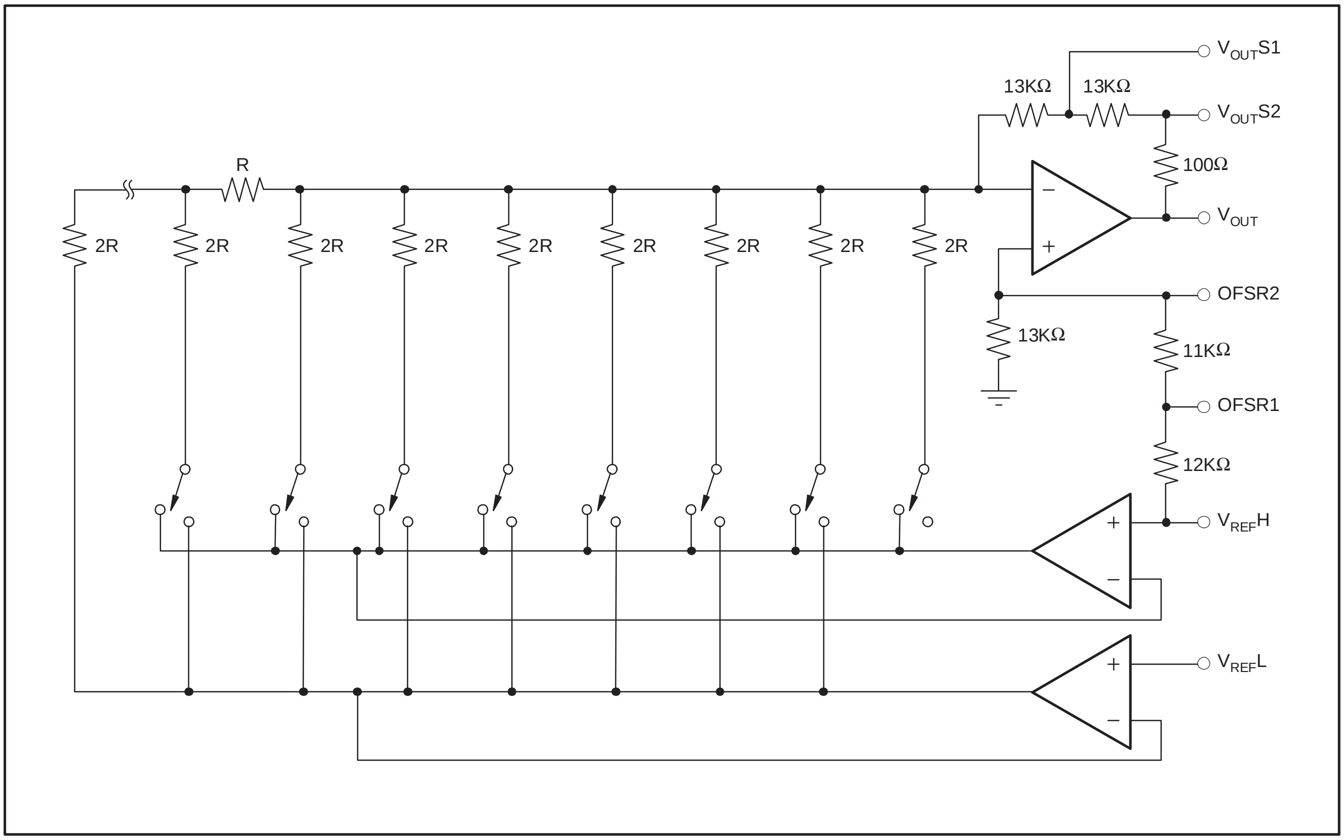

Figure 53. DAC7654 Architecture

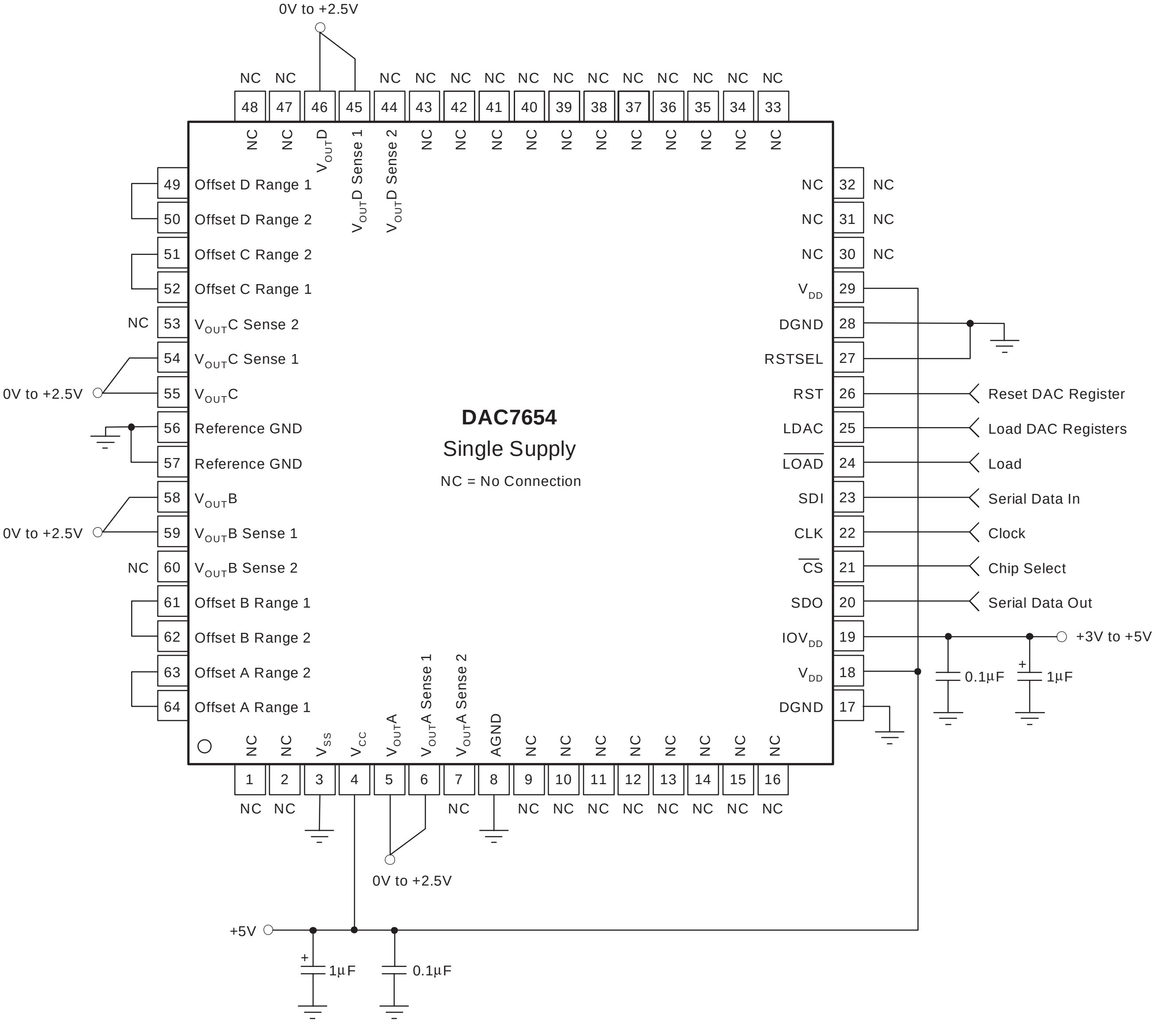

Figure 54. Basic Single-Supply Operation of the DAC7654

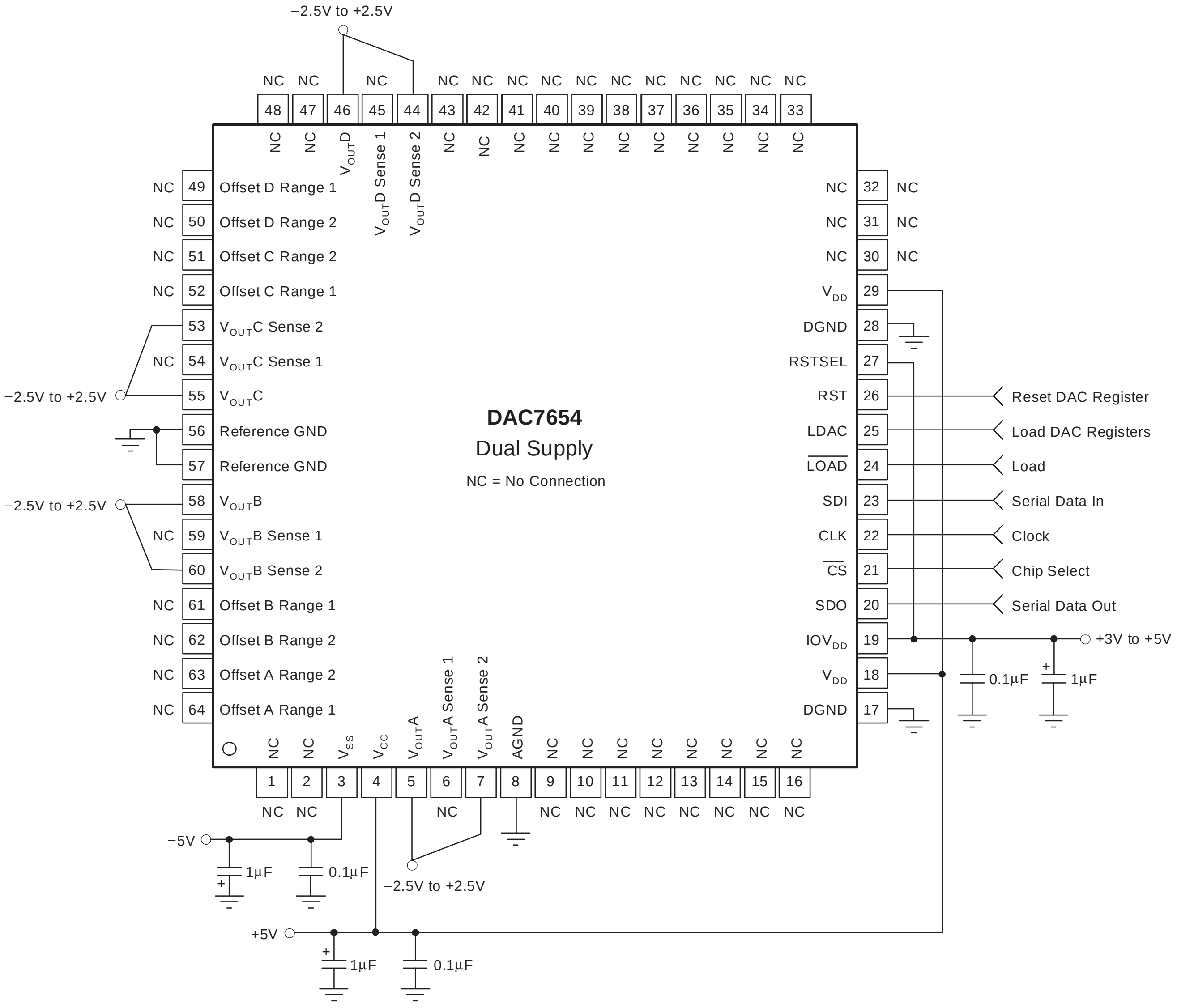

Figure 55. Basic Dual-Supply Operation of the DAC7654

ANALOG OUTPUTS

When V_{SS} = –5V (dual-supply operation), the output amplifier can swing to within 2.25V of the supply rails over a range of –40°C to +85°C. When V_{SS} = 0V (single-supply operation), and with R_{LOAD} also connected to ground, the output can swing to within 5mV of ground. Care must be taken when measuring the zero-scale error when V_{SS} = 0V. Since the output voltage cannot swing below ground, the output voltage may not change for the first few digital input codes (0000h, 0001h, 0002h, etc.) if the output amplifier has a negative offset.

Due to the high accuracy of these DACs, system design problems such as grounding and contact resistance are very important. A 16-bit converter with a 2.5V full-scale range has a 1LSB value of 38μV. With a load current of 1mA, series wiring and connector resistance of only 40mΩ (R_{W2}) will cause a voltage drop of 40μV, as shown in Figure 56. To understand what this means in terms of system layout, the resistivity of a typical 1-ounce copper-clad printed circuit board is 1/2 mΩ per square. For a 1mA load, a 0.01-inch-wide printed circuit conductor 0.6 inches long will result in a voltage drop of 30μV.

The DAC7654 offers a force and sense output configuration for the high open-loop gain output amplifier. This feature allows the loop around the output amplifier to be closed at the load (as shown in Figure 56), thus ensuring an accurate output voltage.

DIGITAL INTERFACE

Table 1 shows the basic control logic for the DAC7654. The interface consists of a signal data clock (CLK) input, serial data in (SDI), DAC input register load control signal ($\overline{\text{LOAD}}$), and DAC register load control signal (LDAC). In addition, a chip select ($\overline{\text{CS}}$) input is available to enable serial communication when there are multiple serial devices. An asynchronous reset (RST) input, by the rising edge, is provided to simplify startup conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select (RSTSEL) signal.

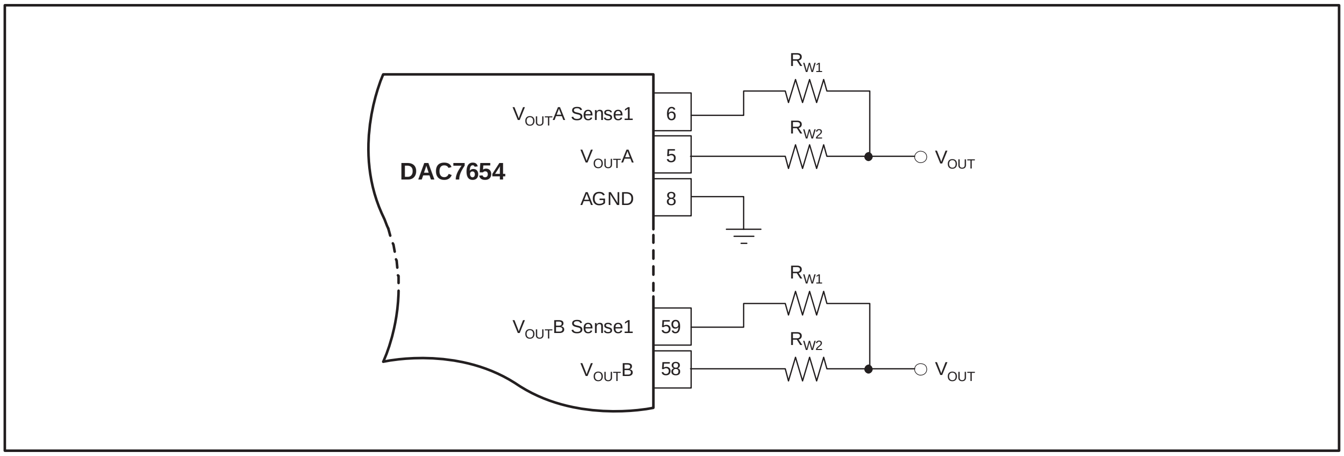

Figure 56. Analog Output Closed-Loop Configuration (1/2 DAC7654). R_W represents wiring resistances.

Table 1. DAC7654 Logic Truth Table

A1	A0	$\overline{\text{CS}}$	RST	RSTSEL	LDAC	$\overline{\text{LOAD}}$	INPUT REGISTER	DAC REGISTER	MODE	DAC
L	L	L	H	X	X	L	Write	Hold	Write input	A
L	H	L	H	X	X	L	Write	Hold	Write input	B
H	L	L	H	X	X	L	Write	Hold	Write input	C
H	H	L	H	X	X	L	Write	Hold	Write input	D
X	X	H	H	X	↑	H	Hold	Write	Update	All
X	X	H	H	X	H	H	Hold	Hold	Hold	All
X	X	X	↑	L	X	X	Reset to zero	Reset to zero	Reset to zero	All
X	X	X	↑	H	X	X	Reset to mid-scale	Reset to mid-scale	Reset to mid-scale	All

The DAC code, quick load control, and address are provided via a 24-bit serial interface (see Table 3; also see Figure 58, page 25). The first two bits select the input register that will be updated when $\overline{\text{LOAD}}$ goes low. The third bit is a Quick Load bit; if high, the code in the shift register is loaded into all of the DAC input registers when the $\overline{\text{LOAD}}$ signal goes low. If the Quick Load bit is low, the content of shift register is loaded only to the DAC input register that is addressed. The Quick Load bit is followed by five unused bits. The last 16 bits (MSB first) are the DAC code.

The internal DAC register is edge triggered and not level triggered. When the LDAC signal is transitioned from low to high, the digital word currently in the DAC input register is latched. The first set of registers (the DAC input registers) are level triggered via the $\overline{\text{LOAD}}$ signal. This double-buffered architecture has been designed so that new data can be entered for each DAC without disturbing the analog outputs. When the new data has been entered into the device, all of the DAC outputs can be updated simultaneously by the rising edge of LDAC. Additionally, it allows writing to the DAC input registers at any point, which permits the DAC output voltages to be synchronously changed via a trigger signal (LDAC).

3V TO 5V LOGIC INTERFACE

All of the digital input and output pins are compatible with any logic supply voltage between 3V and 5V. Connect the interface logic supply voltage to the IOV_{DD} pin. Note that the internal digital logic operates from 5V, so the VDD pin must connect to a 5V supply.

$\overline{\text{CS}}$ AND CLK INPUTS

Note that $\overline{\text{CS}}$ and CLK are combined with an OR gate, which controls the serial-to-parallel shift register. These two inputs are completely interchangeable. However, care must be taken with the state of CLK when $\overline{\text{CS}}$ rises at the end of a serial transfer. If CLK is low when $\overline{\text{CS}}$ rises, the OR gate will provide a rising edge to the shift register, shifting the internal data by one additional bit. The result will be incorrect data and the possible selection of the wrong input register(s). If both $\overline{\text{CS}}$ and CLK are used, $\overline{\text{CS}}$ should rise only when CLK is high. If not, then either $\overline{\text{CS}}$ or CLK can be used to operate the shift register. Table 2 shows more information.

Table 2. Serial Shift Register Truth Table

$\overline{\text{CS}}$(1)	CLK(1)	$\overline{\text{LOAD}}$	RST	SERIAL SHIFT REGISTER
H(2)	X(2)	H	H	No change
L(2)	L	H	H	No change
L	↑(2)	H	H	Advanced one bit
↑	L	H	H	Advanced one bit
H(3)	X	L(4)	H	No change
H(3)	X	H	↑(5)	No change

(1) $\overline{\text{CS}}$ and CLK are interchangeable.
(2) H = logic high. X = don't care. L = logic low. ↑ = positive logic transition.
(3) A high value is suggested in order to avoid a false clock from advancing and changing the shift register.
(4) If data are clocked into the serial register while $\overline{\text{LOAD}}$ is low, the selected DAC register will change as the shift register bits flow through A1 and A0. This will corrupt the data in each DAC register that has been erroneously selected.
(5) Rising edge of RST causes no change in the contents of the serial shift register.

GLITCH SUPPRESSION CIRCUIT

Figure 21, Figure 22, Figure 48, and Figure 49 show the typical DAC output when switching between codes 7FFFh and 8000h. For R-2R ladder DACs, this is potentially the worst-case glitch condition, since every switch in the DAC changes state. To minimize the glitch energy at this and other code pairs with possible high-glitch outputs, an internal track-and-hold circuit is used to maintain the DAC ouput voltage at a nearly constant level during the internal switching interval. This track-and-hold circuit is activated only when the transition is at, or close to, one of the code pairs with the high-glitch possibility.

It is advisable to avoid digital transitions within 1µs of the rising edge of the LDAC signal. These signals can affect the charge on the track-and-hold capacitor, thus increasing the glitch energy.

Table 3. 24-Bit Data and Command Word

B23	B22	B21	B20	B19	B18	B17	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
A1	A0	Quick Load	X	X	X	X	X	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

SERIAL DATA OUTPUT

The serial-data output (SDO) is the internal shift register output. For the DAC7654, the SDO is a driven output and does not require an external pull-up. Any number of DAC7654s can be daisy-chained by connecting the SDO pin of one device to the SDI pin of the following device in the chain, as shown in Figure 57.

DIGITAL TIMING

Figure 58 and Table 4 provide detailed timing for the digital interface of the DAC7654.

DIGITAL INPUT CODING

The DAC7654 input data is in straight binary format. The output voltage for single-supply operation is given by Equation 1:

$$V_{OUT} = \frac{2.5 \times N}{65,536} \tag{1}$$

where N is the digital input code.

This equation does not include the effects of offset (zero-scale) or gain (full-scale) errors.

The output for the dual supply operation is given by Equation 2:

$$V_{OUT} = \frac{5 \times N}{65,536} - 2.5 \tag{2}$$

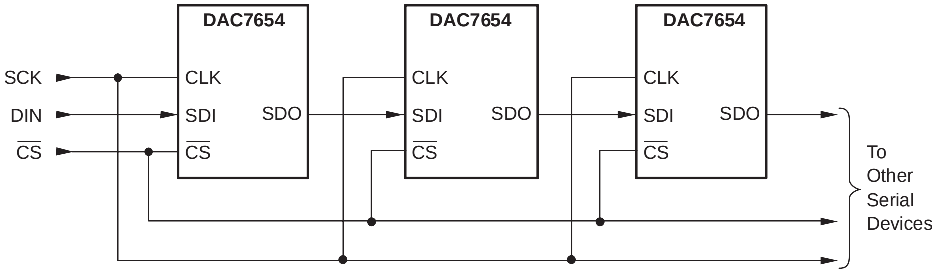

Figure 57. Daisy-Chaining the DAC7654

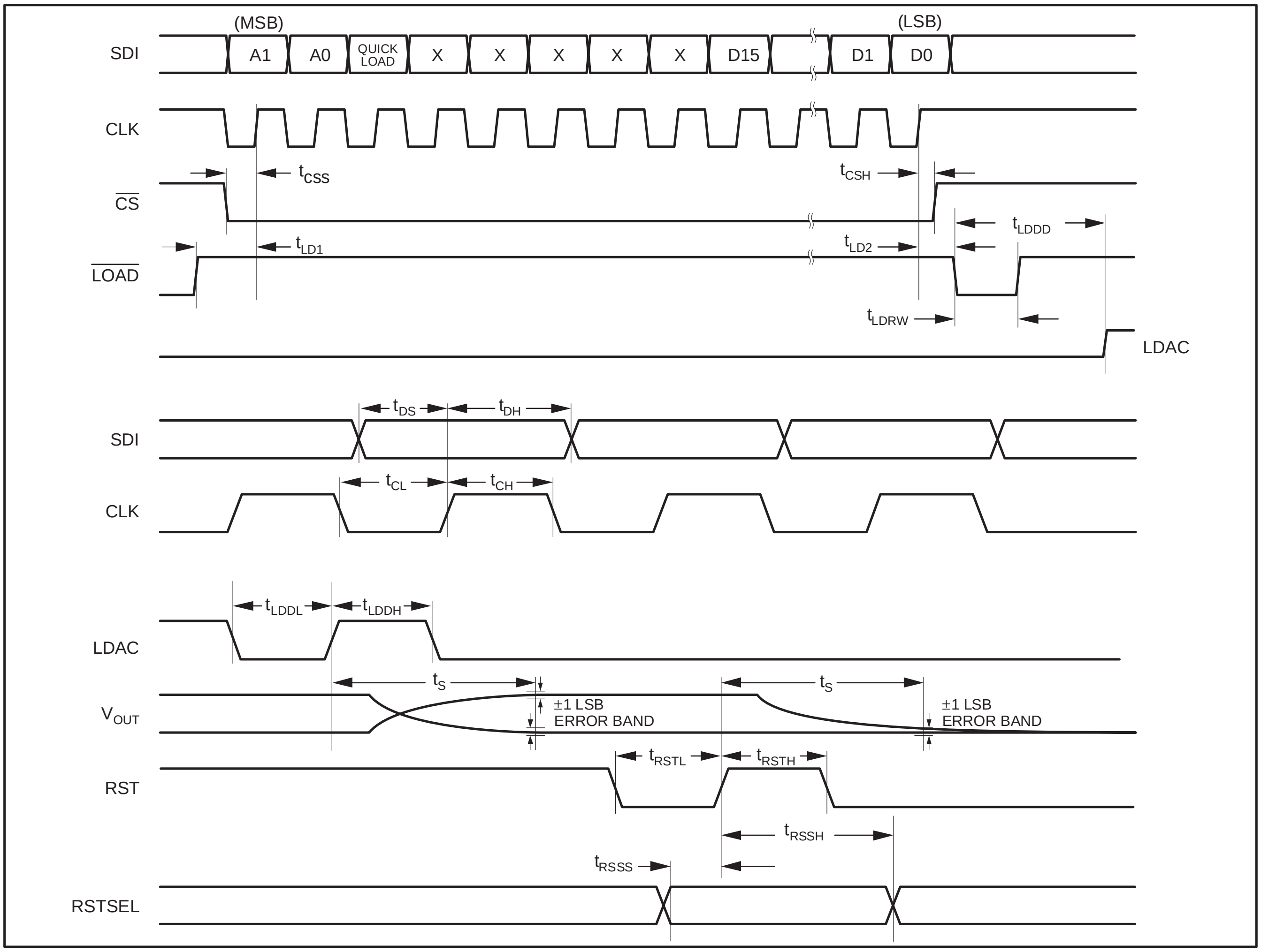

Figure 58. Digital Input and Output Timing

Table 4. Timing Specifications for Figure 58

SYMBOL	DESCRIPTION	MIN	UNITS
t_{DS}	Data valid to CLK rising	10	ns
t_{DH}	Data held valid after CLK rises	20	ns
t_{CH}	CLK high	25	ns
t_{CL}	CLK low	25	ns
t_{CSS}	$\overline{\text{CS}}$ low to CLK rising	15	ns
t_{CSH}	CLK high to $\overline{\text{CS}}$ rising	0	ns
t_{LD1}	$\overline{\text{LOAD}}$ high to CLK rising	10	ns
t_{LD2}	CLK rising to $\overline{\text{LOAD}}$ low	30	ns
t_{LDRW}	$\overline{\text{LOAD}}$ low time	30	ns
t_{LDDL}	LDAC low time	100	ns
t_{LDDH}	LDAC high time	150	ns
t_{LDDD}	LDAC rising from $\overline{\text{LOAD}}$ low	40	ns
t_{RSSS}	RSTSEL valid to RST high	0	ns
t_{RSSH}	RST high to RSTSEL not valid	100	ns
t_{RSTL}	RST low time	10	ns
t_{RSTH}	RST high time	10	ns
t_S	Settling time	10	µs

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7654YCT	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7654Y C	Samples
DAC7654YCTG4	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7654Y C	Samples
DAC7654YT	ACTIVE	LQFP	PM	64	250	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7654Y	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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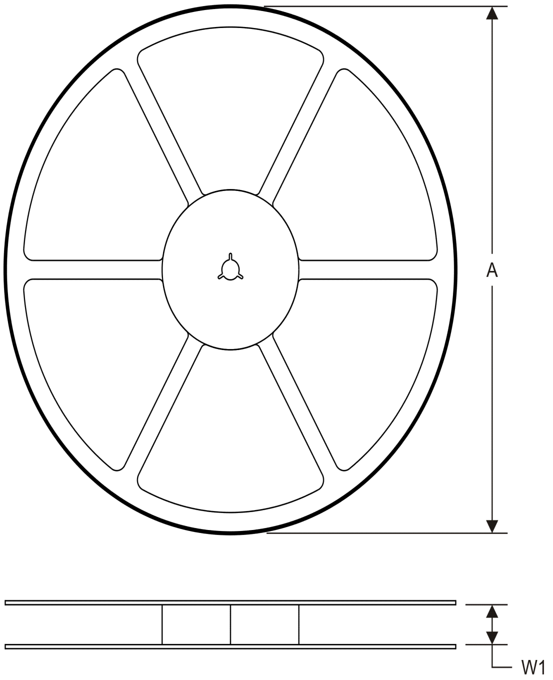
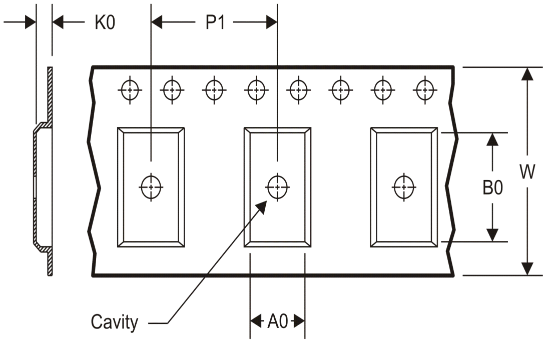
TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



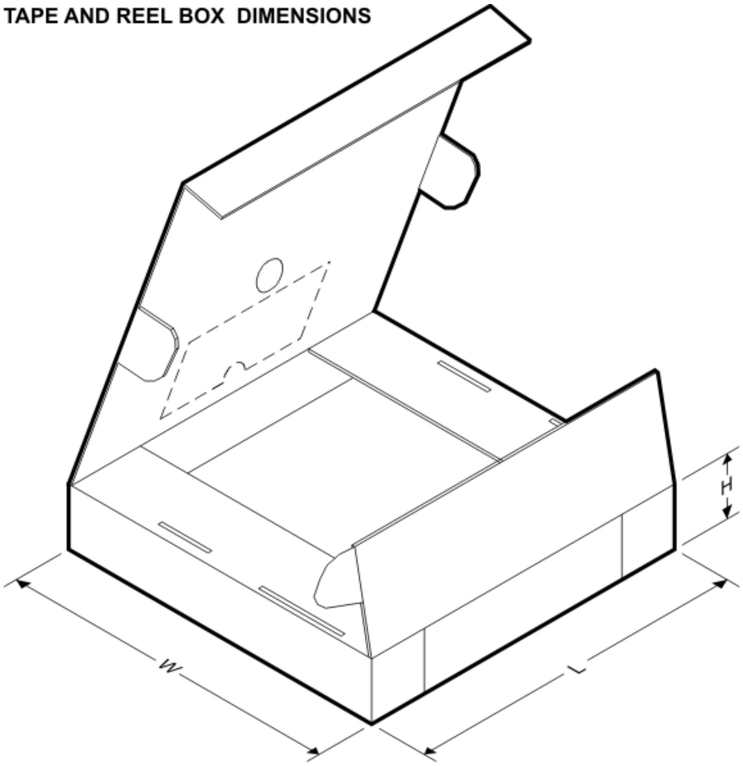
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7654YCT	LQFP	PM	64	250	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
DAC7654YT	LQFP	PM	64	250	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

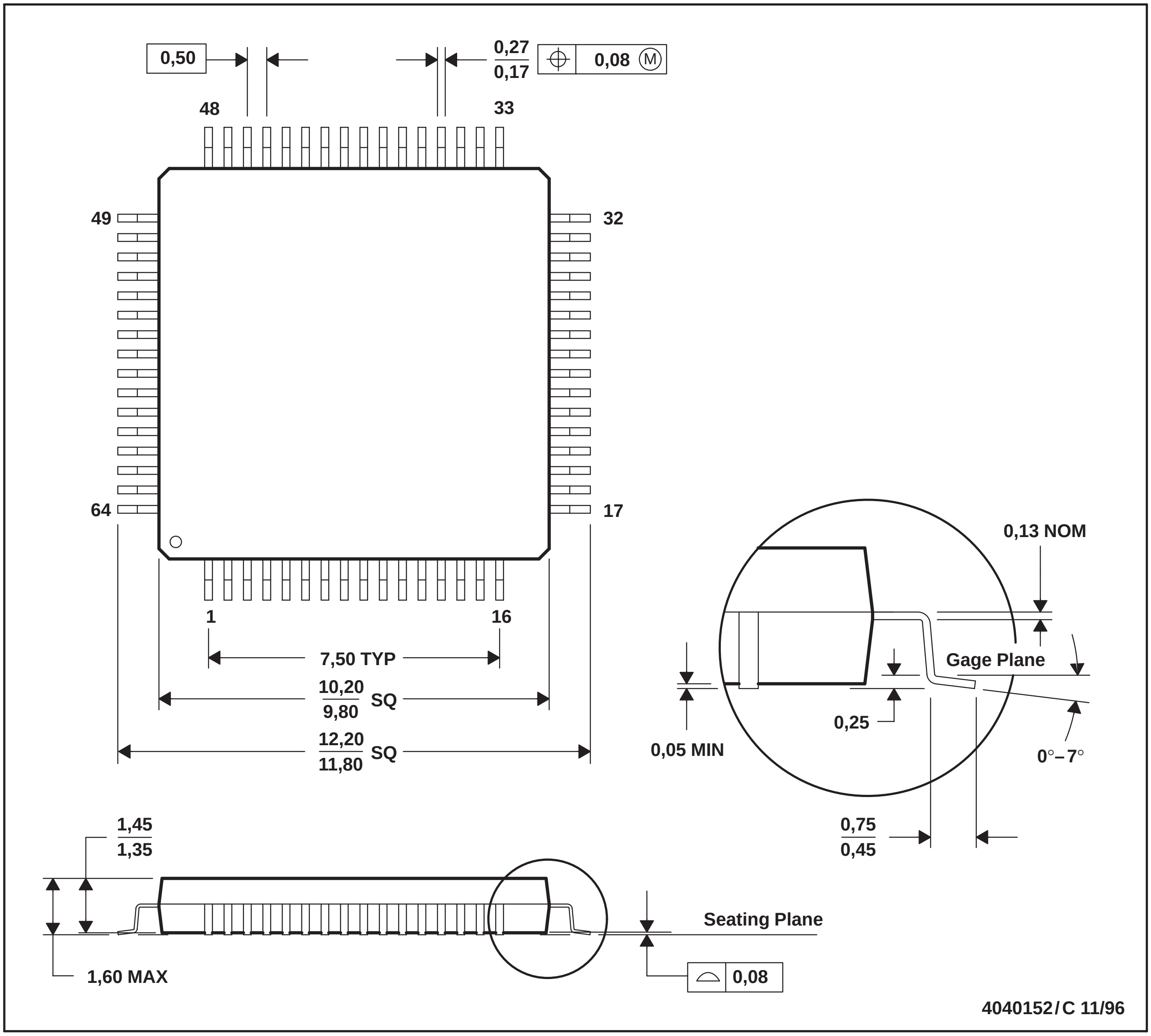
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

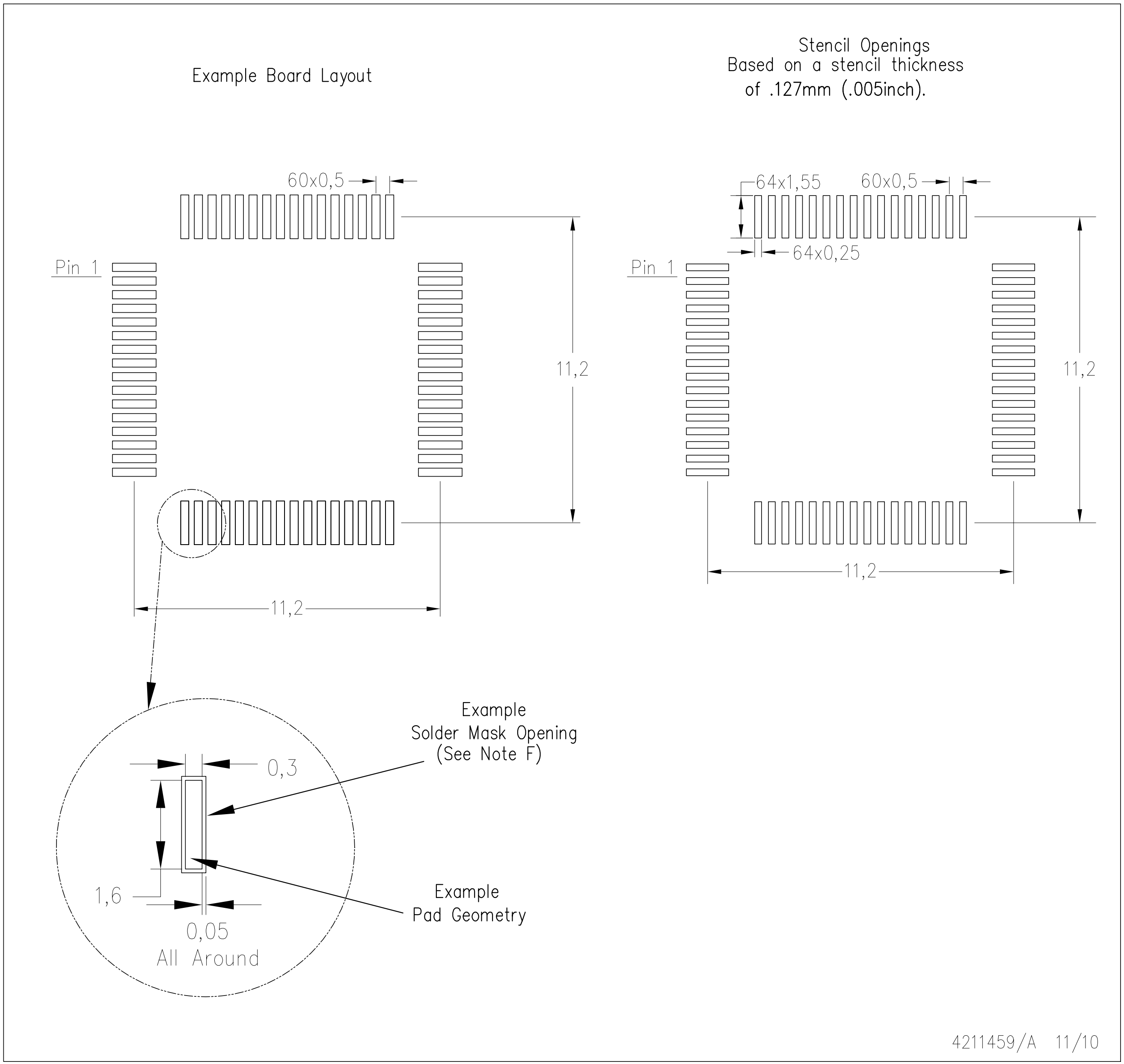
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7654YCT	LQFP	PM	64	250	367.0	367.0	45.0
DAC7654YT	LQFP	PM	64	250	367.0	367.0	45.0

PM (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Falls within JEDEC MS-026
- D. May also be thermally enhanced plastic with leads connected to the die pads.

PM (S-PQFP-G64) PLASTIC QUAD FLATPACK



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- D. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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