Unitrode Products from Texas Instruments

UCC5681
9-LINE LVD-ONLY SCSI TERMINATOR WITH INTEGRATED
SPI-3 DELAYS AND REVERSE DISCONNECT
SLUS441A – MARCH 1999 – REVISED AUGUST 2000

- **LVD-Only Active Termination**
- **2.7 V to 5.25 V Operation**
- **Differential Failsafe Bias**
- **Built-In SPI-3 Mode Change Filter/Delay**

- **Standards Supported: SPI-3, Ultra2 (Fast 40), Ultra3/Ultra160 (Fast 80)**
- **Reversed Disconnect Polarity**

description

The UCC5681 is an LVD-only Small Computer System Interface (SCSI) terminator that integrates the mode change delay function required by the SPI-3 specification. The device senses what types of SCSI drivers are present on the bus via the voltage on the DIFFSENS SCSI control line. Single-ended (SE) and high-voltage differential (HVD) SCSI drivers (EIA485) are not supported. If the chip detects the presence of an SE or HVD SCSI driver, it disconnects itself by switching all terminating resistors off the bus and enters a high-impedance state. The terminator can also be commanded to disconnect the terminating resistors with the $\overline{\text{DISCNCT}}$ input. Impedance is trimmed for accuracy and maximum effectiveness. Bus lines are biased to a failsafe state to ensure signal integrity.

The UCC5681 is offered in both 24-pin and 28-pin TSSOP (PW) packages for a temperature range of 0°C to 70°C.

functional block diagram
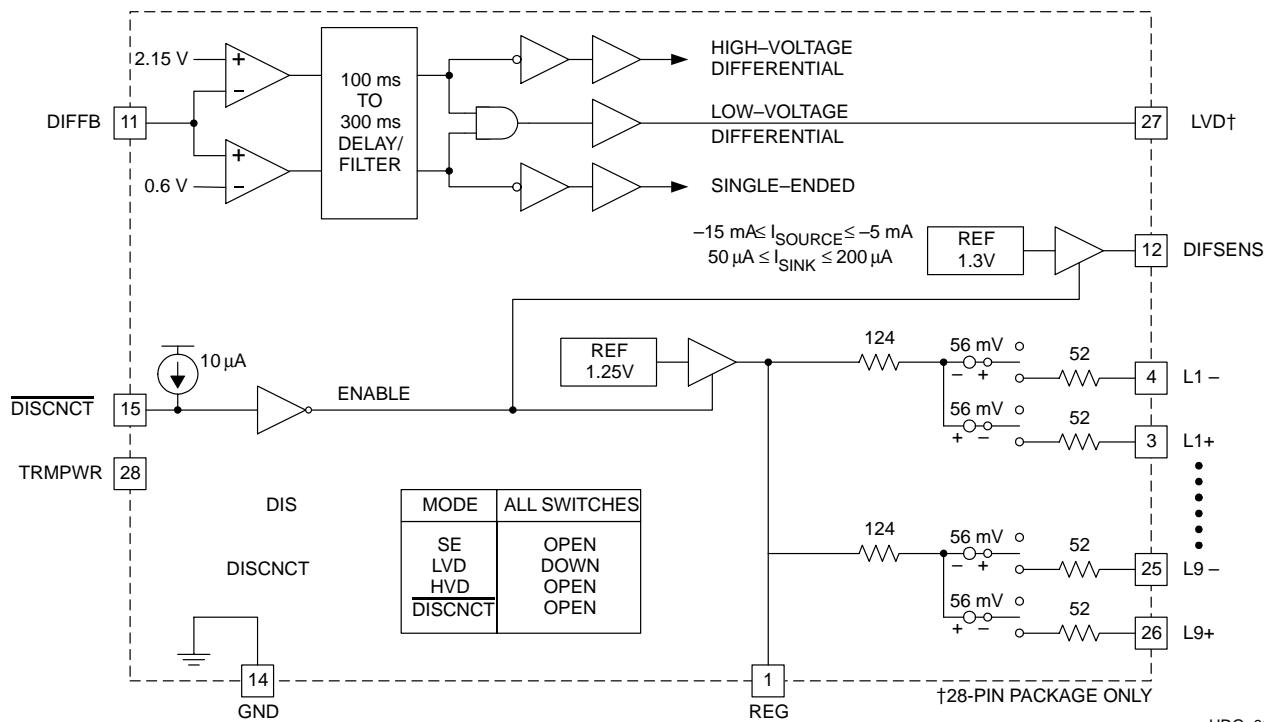
MODE	ALL SWITCHES
SE	OPEN
LVD	DOWN
HVD	OPEN
$\overline{\text{DISCNCT}}$	OPEN

†28-PIN PACKAGE ONLY

UDG–00126

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

UCC5681
9-LINE LVD-ONLY SCSI TERMINATOR WITH INTEGRATED SPI-3 DELAYS AND REVERSE DISCONNECT

SLUS441A – MARCH 1999 – REVISED AUGUST 2000

24-PIN PW PACKAGE
(TOP VIEW)

REG	1		24	TRMPWR
L1+	2		23	L9+
L1 –	3		22	L9 –
L2+	4		21	L8+
L2 –	5		20	L8 –
L3+	6		19	L7+
L3 –	7		18	L7 –
L4+	8		17	L6+
L4 –	9		16	L6 –
DIFFB	10		15	L5+
DIFSENS	11		14	L5 –
GND	12		13	DISCNCT

28-PIN PW PACKAGE
(TOP VIEW)

REG	1		28	TRMPWR
N/C	2		27	LVD
L1+	3		26	L9+
L1 –	4		25	L9 –
L2+	5		24	L8+
L2 –	6		23	L8 –
L3+	7		22	L7+
L3 –	8		21	L7 –
L4+	9		20	L6+
L4 –	10		19	L6 –
DIFFB	11		18	L5+
DIFSENS	12		17	L5 –
N/C	13		16	N/C
GND	14		15	DISCNCT
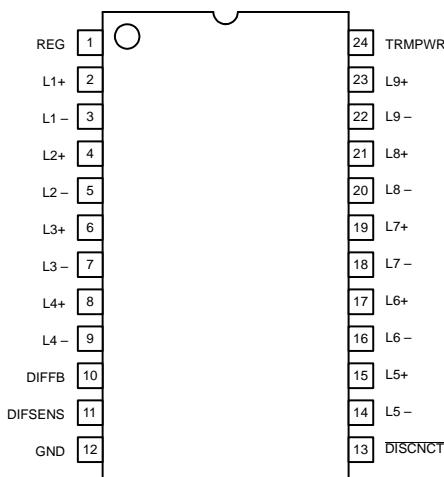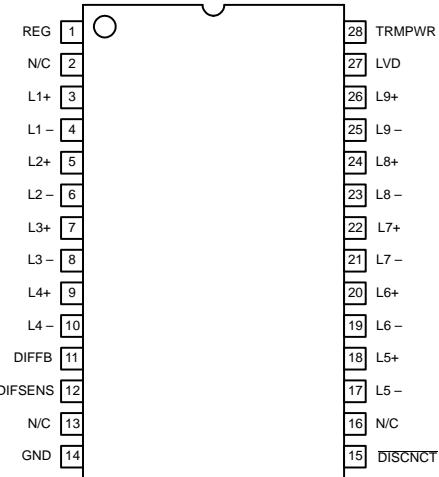
absolute maximum ratings over operating free-air temperature (unless otherwise noted)†

TERMPWR Voltage . . . . 6 V
Signal Line Voltage . . . . 0 V to 5 V
Package Dissipation . . . . 0.5 W
Storage Temperature . . . . –65°C to 150°C
Junction Temperature . . . . –55°C to 150°C
Lead Temperature (Soldering, 10 sec.) . . . . 300°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

TERMPWR Voltage . . . . 2.7 V to 5.25 V
Operating Temperature Range . . . . 0°C to 70°C

electrical characteristics over recommended operating free-air temperature range, $T_A = T_J = 0°C$ to $70°C$, TRMPWR = 2.7 V to 5.25 V

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
TRMPWR Supply Current Section					
TRMPWR supply current	LVD Mode (No Load)			35	mA
	Disabled Mode			500	µA
Regulator Section					
Regulator output voltage	0.5 V $\leq V_{CM} \leq$ 2.0, See Note 1	1.15	1.25	1.35	V
Regulator short-circuit source current	V_{REG} = 0 V		-100	-80	mA
Regulator short-circuit sink current	V_{REG} = 3.0 V	80	100		mA
DIFSENS Output Section					
Output voltage	–5 mA $\leq I_{DIFSENS} \leq$ 50 µA	1.2	1.3	1.4	V
Short-circuit source current	$V_{DIFSENS}$ = 0 V	-15		-5	mA
Short-circuit sink current	$V_{DIFSENS}$ = 2.75 V	50		200	µA
Differential Termination Section (Applies to each line pair , 1-9, in LVD mode)					
Differential impedance		100	105	110	Ω
Common-mode impedance	L+ and L- shorted together, See Note 2	110	150	165	Ω
Differential bias voltage		100		125	mV
Common-mode bias voltage	L+ and L- shorted together	1.15	1.25	1.35	V
Disconnected Termination Section (Applies to each line pair , 1-9, in DISCNCT, SE or HVD mode)					
Output leakage				400	nA
Output capacitance	Single-ended measurement to ground, See Note 3			3	pF
DISCNCT and DIFFB Input Section					
$\overline{DISCNCT}$ threshold		0.8		2.0	V
$\overline{DISCNCT}$ input current	$V_{\overline{DISCNCT}}$ = 0 V and 2.0 V	-30	-10		µA
DIFFB SE to LVD threshold		0.5		0.7	V
DIFFB LVD to HVD threshold		1.9		2.4	V
DIFFB input current	0 V $\leq V_{DIFFB} \leq$ 2.75 V	-10		10	µA
Low Voltage Differential (LVD) Status Bit Section (See Note 4)					
I_{SOURCE}	V_{LOAD} = 2.4 V		-6	-4	mA
I_{SINK}	V_{LOAD} = 0.4 V	2	5		mA
Time Delay/Filter Section					
Mode change delay	A new mode change can start any time after a previous mode change has been detected	100	190	300	ms
Thermal Shutdown Section					
Themal shutdown threshold	For increasing temperature	140	155	170	°C
Themal shutdown hysteresis			10		°C

NOTES: 1. V_{CM} is applied to all L+ and L- lines simultaneously.

2. $Z_{CM} = \dfrac{(2.0V - 0.5V)}{\left[I_{VCM(max)} - I_{VCM(min)} \right]}$ @ $V_{CM(max)}$ = 2.0, $V_{CM(min)}$ = 0.5 V

3. Ensured by design, not production tested.

4. This applies to the 28-pin package only.

pin descriptions

DIFFB: DIFFSENS input pin. Connect through a 20-kΩ resistor to DIFSENS and through a 0.1-µF capacitor to ground. Input to comparators that detect what types of drivers are connected to the SCSI bus.

DIFSENS: SCSI bus DIFSENS line driver.

$\overline{\text{DISCNCT}}$: Disconnect pin. Shuts down the terminator (switches terminating resistors off the bus) when tied to GND. The disconnect pin high (or OPEN) enables the terminator.

GND: Power supply return.

LINE*n*-: Line termination pins. Negative line in differential pair.

LINE*n*+: Line termination pins. Positive line in differential pair.

LVD: (28-pin package only) Indicates that the bus is in LVD mode.

REG: Regulator bypass pin. Bypass near the terminator with a 4.7-µF and a high-frequency, low-ESR 0.01-µF capacitor to ground.

TRMPWR: V_{IN} 2.75 V to 5.25 V supply. Bypass near the terminator with a 4.7-µF and a high-frequency, low-ESR 0.01-µF capacitor to ground.

APPLICATION INFORMATION

All SCSI buses require a termination network at each end to function properly. Specific termination requirements differ, depending on which types of SCSI driver devices are present on the bus. The UCC5681 is a low-voltage differential (LVD)-only device. It senses which types of drivers are present on the bus. If it detects the presence of a single-ended (SE) or high-voltage differential (HVD) driver, the UCC5681 will place itself in a high-impedance input state, effectively disconnecting the chip from the bus.

The UCC5681 senses what kinds of drivers are present on the bus by the voltage on SCSI bus control line DIFFSENS, which is monitored by the DIFFB input pin. The DIFSENS output pin on the UCC5681 attempts to drive a DIFFSENS control line to 1.3 V. If only LVD devices are present, the DIFFSENS line will be successfully driven to that voltage. If HVD drivers are present, they will pull the DIFFSENS line high. If any single-ended drivers are present, they pull the DIFSENS line to ground (even if HVD drivers are also present on the bus). If the voltage on the DIFFB is below 0.5 V or above 2.4 V, the UCC5681 enters the high-impedance SE/HVD state. If it is between 0.7 V and 1.9 V, the UCC5681 enters the LVD mode. These thresholds accommodate differences in ground potential that can occur between the ends of long bus lines.

Three UCC5681 ICs are required at each end of the SCSI bus to terminate 27 lines (18 data, 9 control). Every UCC5681 contains a DIFSENS driver, but only one should be used to drive the line at each end. The DIFSENS pin on the other devices should be left unconnected.

On power up (the voltage on the TRMPWR pin rising above 2.7 V), the UCC5681 assumes the SE/HVD mode. If the voltage on the DIFFB input indicates LVD mode, the chip waits 100 ms to 300 ms before changing the mode of the bus. If the voltage at the DIFFB input later crosses one of the thresholds, the UCC5681 again waits 100 ms to 300 ms before changing the mode of the bus. The magnitude of the delay is the same when changing in or out of either bus mode. A new mode change can start anytime after a previous mode change has been detected.

The DIFFB inputs on all three chips at each end of the bus should be connected together. Properly filtered, noise on DIFFB will not cause a false mode change. There should be a shared 50-Hz noise filter implemented on DIFFB at each end of the bus as close as possible to the DIFFB pins. This is implemented with a 20-kΩ resistor between the DIFFB and DIFSENS pins, and a 0.1-µF capacitor from DIFFB to ground. See the *Typical Application* diagram at the end of this datasheet.

TEXAS
INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

APPLICATION INFORMATION (continued)

In LVD mode, the regulated voltage is switched to 1.25 V and a resistor network is presented to each line pair that provides common-mode impedance of 150 Ω and differential impedance of 105 Ω. The lines in each differential pair are biased so that when not driven, Line(n)+ and Line(n)– are driven 56 mV below and above the common-mode bias voltage (1.25 V) respectively.

In SE/HVD mode, all the terminating resistors are switched off the bus. The 1.25-V and 1.3-V (DIFSENS) regulators are left on.

When the disconnect input ($\overline{\text{DISCNCT}}$) is low, the terminating resistors are switched off the bus and both voltage regulators are turned off to save power. The mode change filter/delay function is still active and the LVD pin (in the 28-pin package) continues to indicate the correct bus mode.

The UCC5681 operates down to a TRMPWR voltage of 2.7 V. This accommodates a 3.3-V system with allowance for supply tolerance ($\pm$10%), a unidirectional fusing device, and cable drop. The UCC3916 is recommended in place of a fuse and diode implementation, as its lower voltage drop provides additional voltage margin for the system.

Layout is important in all SCSI implementations and critical in SPI-3 systems, which have stringent requirements on both the absolute value of capacitance on differential signal lines and the balancing of capacitance between paired lines and from pair to pair.

Feedthroughs, through-hole connections, and etch lengths need to be carefully balanced. Standard multilayer power and ground plane spacing adds about 1 pF to each plane. Each feed-through will add 2.5 pF to 3.5 pF. Enlarging the clearance holes on both power and ground planes reduces capacitance. Opening up the power and ground planes under a through-hole connector reduces added capacitance in those applications. Capacitance is also affected by components in close proximity on both sides of the board.

maximum capacitance

SCSI Class	Trace to GND: REQ, ACK, DATA, Parity, P_CRCA	Trace to Trace: REQ, ACK, DATA, Parity, P_CRCA	Trace to GND: Other signals	Trace to Trace: Other Signals
Ultra1	25 pF	N/A	25 pF	N/A
Ultra2	20 pF	10 pF	25 pF	13 pF
Ultra3/Ultra160	15 pF	8 pF	25 pF	13 pF
Ultra320	13 pF	6.5 pF	21 pF (est.)	10 pF (est.)

TI terminators are designed with very tightly controlled capacitance on their signal lines. Between the positive and negative lines in a differential pair the difference is typically no more than 0.1 pF, and only 0.3 pF between pairs.

Multi-layer boards need to adhere to the 120-Ω impedance standard, including the connector and feedthroughs. Bus traces are normally run on the outer layers of the board with 4-mil etch and 4-mil spacing between the two lines in each differential pair, and a minimum of 8-mil spacing to adjacent pairs to minimize crosstalk. Microstrip technology is too low in impedance and should not be used—it is designed for 50 Ω rather than 120-Ω differential systems.

Decoupling capacitors should be installed as close as possible to the following input pins of the UCC5681:

TRMPWR: 4.7-μF capacitor to ground, 0.01-μF capacitor to ground (high-frequency, low ESR)

REG: 4.7-μF capacitor to ground, 0.01-μF capacitor to ground (high-frequency, low ESR)

TYPICAL APPLICATION

UDG-00125

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

TEXAS INSTRUMENTS
www.ti.com
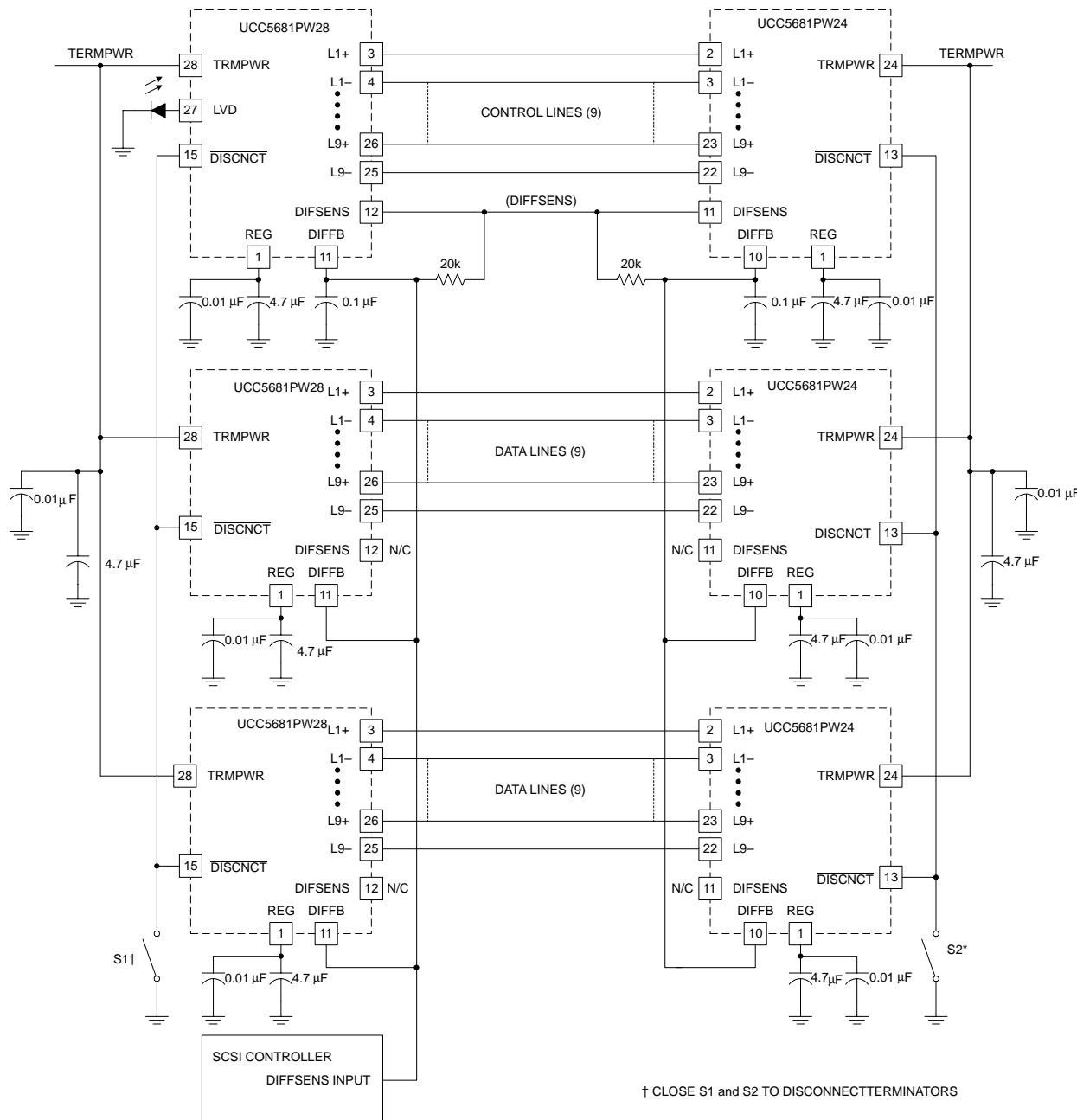
PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
UCC5681PW24	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
UCC5681PW24G4	ACTIVE	TSSOP	PW	24	60	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

[1] The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN

0,65

0,30
0,19

⊕ 0,10 Ⓜ

14   8

4,50
4,30

6,60
6,20

1   7

A

0,15 NOM

Gage Plane

0°–8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌒ 0,10

DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F 01/97
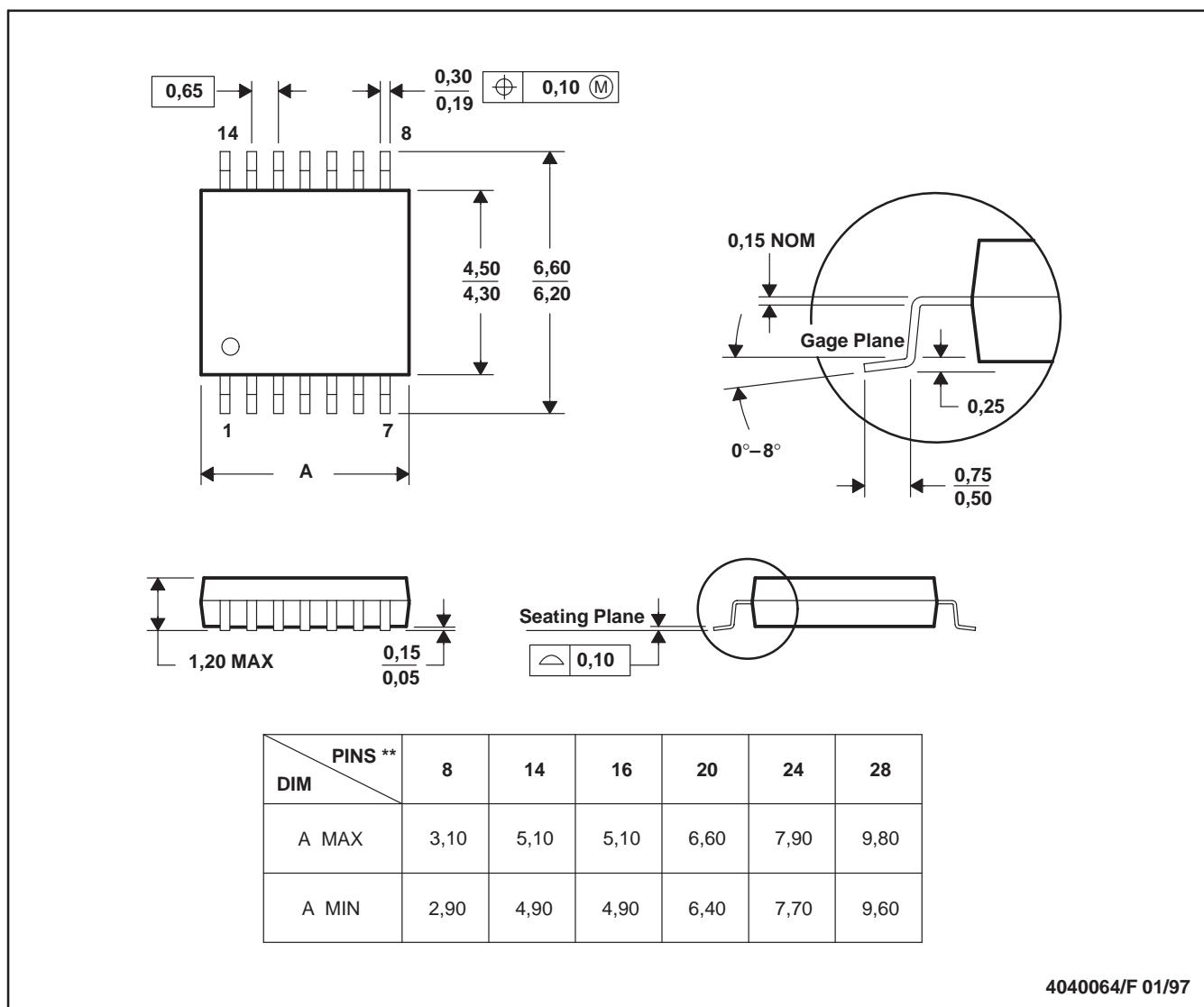
NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

![Texas Instruments logo] **TEXAS INSTRUMENTS**

POST OFFICE BOX 655303 ● DALLAS, TEXAS 75265

IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

Products		**Applications**	
Amplifiers	amplifier.ti.com	Audio	www.ti.com/audio
Data Converters	dataconverter.ti.com	Automotive	www.ti.com/automotive
DSP	dsp.ti.com	Broadband	www.ti.com/broadband
Interface	interface.ti.com	Digital Control	www.ti.com/digitalcontrol
Logic	logic.ti.com	Military	www.ti.com/military
Power Mgmt	power.ti.com	Optical Networking	www.ti.com/opticalnetwork
Microcontrollers	microcontroller.ti.com	Security	www.ti.com/security
Low Power Wireless	www.ti.com/lpw	Telephony	www.ti.com/telephony
		Video & Imaging	www.ti.com/video
		Wireless	www.ti.com/wireless

Mailing Address: Texas Instruments
                     Post Office Box 655303 Dallas, Texas 75265