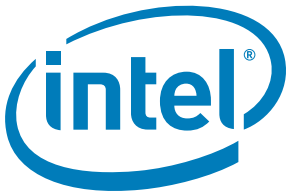

Intel® Atom™ Processor 200$^{\Delta}$ Series

Datasheet

June 2008

Document Number: 319977-001

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Revision History

Revision Number	Description	Date
-001	• Initial Release	June 2008

Intel® Atom™ Processor 200 Series Features

- Available at 1.6 GHz,
- On die, primary 32-kB instructions cache and 24-KB write-back data cache
- 533-MHz Source-Synchronous front side bus (FSB)
- Threading enabled
- On-die 512-KB, 8-way L2 cache
- Support for IA 32-bit and Intel® 64 architecture
- Streaming SIMD Extensions 2 and 3 (SSE2 and SSE3) support
- Micro-FCBGA packaging technologies
- Thermal management support via TM1
- FSB Lane Reversal for flexible routing
- Supports C0 and C1 states only
- L2 Dynamic Cache Sizing
- Execute Disable Bit support for enhanced security

The Intel® Atom™ processor 200 series represents a new family of processors designed from the ground-up on a ground-breaking new low-power microarchitecture. It is manufactured on industry-leading 45 nm process with Hi-K Metal Gate technology.

The Intel® Atom™ processor 200 series enables a new class of simple and affordable internet-centric computers called “nettops” that is best suited for applications focused on internet usage models—communicate, listen, watch, play, share, and learn.

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1 Introduction

The Intel® Atom™ processor 200 series is a single-core processor built on 45-nanometer process technology. In nettop 2008 platforms, the Intel® Atom™ processor 200 series supports SiS as well as Intel chipsets. The processor use a Flip-Chip Ball Grid Array (FCBGA) package technology. This document contains electrical, mechanical, and thermal specifications for the processor.

Note: In this document, the Intel® Atom™ Single Core processor 200 series will be referred to as the "processor". SiS and Intel chipsets are referred to as GMCH and ICH respectively.

Note: In this document, the Intel® Atom™ processor 200 series refers to the Intel® Atom™ processor 230.

1.1 Terminology

Term	Definition
#	A "#" symbol after a signal name refers to an active low signal, indicating a signal is in the active state when driven to a low level. For example, when RESET# is low, a reset has been requested. Conversely, when NMI is high, a nonmaskable interrupt has occurred. In the case of signals where the name does not imply an active state but describes part of a binary sequence (such as *address* or *data*), the "#" symbol implies that the signal is inverted. For example, D[3:0] = "HLHL" refers to a hex 'A', and D[3:0]# = "LHLH" also refers to a hex "A" (H= High logic level, L= Low logic level).
Front Side Bus (FSB)	Refers to the interface between the processor and system core logic (also known as the GMCH chipset components).
AGTL+	Advanced Gunning Transceiver Logic. Used to refer to Assisted GTL+ signaling technology on some Intel processors.
CMOS	Complementary metal-Oxide semiconductor.
Storage Conditions	Refers to a non-operational state. The processor may be installed in a platform, in a tray, or loose. Processors may be sealed in packaging or exposed to free air. Under these conditions, processor landings should not be connected to any supply voltages, have any I/Os biased or receive any clocks. Upon exposure to "free air" (i.e., unsealed packaging or a device removed from packaging material) the processor must be handled in accordance with moisture sensitivity labeling (MSL) as indicated on the packaging material.
Enhanced Intel SpeedStep® Technology	Technology that provides power management capabilities to low power devices.
Processor Core	Processor core die with integrated L1 and L2 cache. All AC timing and signal integrity specifications are at the pads of the processor core.
Intel® 64 Technology	64-bit memory extensions to the IA-32 architecture.
Intel® Virtualization Technology	Processor virtualization which when used in conjunction with Virtual Machine Monitor software enables multiple, robust independent software environments inside a single platform.

Term	Definition
TDP	Thermal Design Power
V_{CC}	The processor core power supply
V_{TT}	FSB AGTL+ termination voltage with respect to V_{SS}
VR	Voltage Regulator
V_{SS}	The processor ground

1.2 References

Material and concepts available in the following documents may be beneficial when reading this document.

Table 1. References

Document	Document Number
Intel® Atom™ Processors 200 Series Specification Update	www.intel.com/design/processor/specupdt/319978.pdf
Intel® Atom™ Processors 200 Series Thermal and Mechanical Design Guidelines	www.intel.com/design/processor/designex/319979.pdf
AP-485, Intel® Processor Identification and CPUID Instruction Application Note	http://www.intel.com/design/processor/applnots/241618.htm
Voltage Regulator-Down (VRD) 11.0 - Processor POwer Delivery Design Guidelines	http://www.intel.com/design/processor/applnots/313214.htm
Intel® 64 and IA-32 Architectures Software Developer's Manuals Volume 1: Basic Architecture Volume 2A: Instruction Set Reference, A-M Volume 2B: Instruction Set Reference, N-Z Volume 3A: System Programming Guide Volume 3B: System Programming Guide	http://www.intel.com/products/processor/manuals/index.htm

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2 Low Power Features

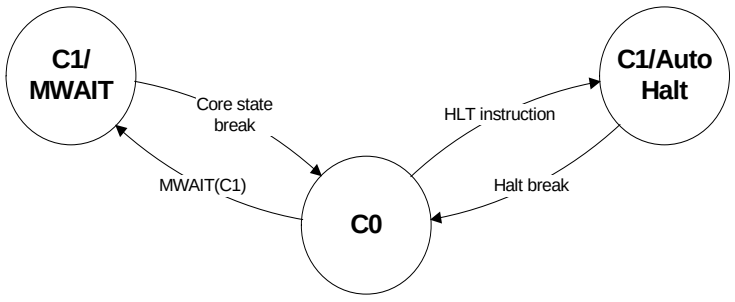
2.1 Clock Control and Low-power States

The processor supports low power states at the thread level and the package level. A thread may independently enter the C1/AutoHALT and C1/MWAIT low power states. When both threads are in a common low-power state, the central power management logic ensures the entire processor enters the respective package low power state by initiating a P_LVLx I/O read to the chipset.

The processor implements two software interfaces for requesting low power states, MWAIT instruction extensions with sub-state hints and P_LVLx reads to the ACPI P_BLK register block mapped in the processor's I/O address space. The P_LVLx I/O reads are converted to equivalent MWAIT C-state requests inside the processor and do not directly result in I/O reads on the processor FSB. The monitor address does not need to be setup before using the P_LVLx I/O read interface. The sub-state hints used for each P_LVLx read can be configured in a software programmable MSR.

Figure 1 shows the thread low-power states. Table 2 provides a mapping of thread low-power states to package low power states.

Figure 1. Thread Low-power States



halt break = A20M# transition, INIT#, INTR, NMI, PREQ#, RESET#, SMI#, or APIC interrupt
core state break = (halt break OR Monitor event)

Table 2. Coordination of Thread Low-power States at the Package Level

Thread State	Package State[2]	
	C0	C1[1]
C0	Normal	Normal
C1[1]	Normal	AutoHalt

NOTES:
1. AutoHALT or MWAIT/C1.
2. To enter a package state, both threads must be in a common low power state. If the threads are not in a common low power state, the package state will resolve to the highest power C state.

2.1.1 Thread Low-power State Descriptions

2.1.1.1 Thread C0 State

This is the normal operating state for threads in the processor.

2.1.1.2 Thread C1/AutoHALT Powerdown State

C1/AutoHALT is a low-power state entered when a thread executes the HALT instruction. The processor thread will transition to the C0 state upon occurrence of SMI#, INIT#, LINT[1:0] (NMI, INTR), or FSB interrupt messages. RESET# will cause the processor to immediately initialize itself.

A System Management Interrupt (SMI) handler will return execution to either Normal state or the AutoHALT Powerdown state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 3A/3B: System Programmer's Guide* for more information.

While in AutoHALT Powerdown state, the processor threads will process bus snoops and snoops from the other thread. The processor will enter a snoopable sub-state (not shown in Figure 1) to process the snoop and then return to the AutoHALT Powerdown state.

2.1.1.3 Thread C1/MWAIT Powerdown State

C1/MWAIT is a low-power state entered when the processor thread executes the MWAIT(C1) instruction. Processor behavior in the MWAIT state is identical to the AutoHALT state except that Monitor events can cause the processor to return to the C0 state. See the *Intel® 64 and IA-32 Architectures Software Developer's Manuals, Volume 2A: Instruction Set Reference, A-M* and *Volume 2B: Instruction Set Reference, N-Z*, for more information.

2.1.2 Package Low-power State Descriptions

Note: The following state descriptions assume that both threads are in the a common low power state. For cases when only one thread is in a low power state, see Section 2.1.1.

2.1.2.1 Normal State

This is the normal operating state for the processor. The processor remains in the Normal state when the threads are in the C0, C1/AutoHALT, or C1/MWAIT state.

2.1.3 Front Side Bus

The processor has only one signaling mode, where the data and address busses and the strobe signals are operating in GTL mode. The reason to use GTL is to improve signal integrity.

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3 Electrical Specifications

This chapter contains signal group descriptions, absolute maximum ratings, voltage identification, and power sequencing. The chapter also includes DC specifications.

3.1 FSB and GTLREF

The processor supports two kinds of signalling protocol: Complementary Metal Oxide Semiconductor (CMOS), and Advanced Gunning Transceiver Logic (AGTL+). For FSB data and address bus, only AGTL+ is used.

The termination voltage level for the processor CMOS and AGTL+ signals is V_{TT} = 1.10 V (nominal). Due to speed improvements to data and address bus, signal integrity and platform design methods have become more critical than with previous processor families.

The CMOS sideband signals are listed in Table 6.

The AGTL+ inputs, including the sideband signals listed in Table 6, require a reference voltage (GTLREF) that is used by the receivers to determine if a signal is a logical 0 or a logical 1. GTLREF must be generated on the system board. Termination resistors are provided on the processor silicon and are terminated to its I/O voltage (V_{TT}). The appropriate chipset will also provide on-die termination; thus, eliminating the need to terminate the bus on the system board for most AGTL+ signals.

The AGTL+ bus depends on incident wave switching. Timing calculations for AGTL+ signals are based on flight time as opposed to capacitive deratings. Analog signal simulation of the FSB, including trace lengths, is highly recommended when designing a system.

3.2 Power and Ground Pins

For clean, on-chip power distribution, the processor will have a large number of VTT (FSB AGTL+ reference voltage), VCCP (power) and VSS (ground) inputs. All power pins must be connected to V_{CCP} power planes while all VSS pins must be connected to system ground planes. Use of multiple power and ground planes is recommended to reduce I*R drop. The processor VCCP pins must be supplied the voltage stated in Table 8

3.3 Decoupling Guidelines

Due to its large number of transistors and high internal clock speeds, the processor is capable of generating large average current swings between low and full power states. This may cause voltages on power planes to sag below their minimum values if bulk decoupling is not adequate. Larger bulk storage, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition. Care must be taken in the board design to ensure that the voltage provided to the processor remains within the specifications listed in Table 8. Failure to do so can result in timing violations or reduced lifetime of the component. For further information and design guidelines, refer to the *Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines.*

3.3.1 V_{CCP} Decoupling

V_{CCP} regulator solutions need to provide bulk capacitance with a low Effective Series Resistance (ESR) and keep a low interconnect resistance from the regulator to the socket. Bulk decoupling for the large current swings when the part is powering on, or entering/exiting low-power states, must be provided by the voltage regulator solution For more details on decoupling recommendations, refer to the *Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines.*

3.3.2 FSB AGTL+ Decoupling

The processor integrates signal termination on the die. Decoupling must also be provided by the system motherboard for proper AGTL+ bus operation.

3.4 Voltage Identification and Power Sequencing

Table 3. Voltage Identification Definition

VID 6	VID 5	VID 4	VID 3	VID 2	VID 1	VID 0	VCC (V)
0	1	0	0	0	0	1	1.2000
0	1	0	0	0	1	0	1.1875
0	1	0	0	0	1	1	1.1750
0	1	0	0	1	0	0	1.1625
0	1	0	0	1	0	1	1.1500
0	1	0	0	1	1	0	1.1375
0	1	0	0	1	1	1	1.1250
0	1	0	1	0	0	0	1.1125
0	1	0	1	0	0	1	1.1000
0	1	0	1	0	1	0	1.0875
0	1	0	1	0	1	1	1.0750
0	1	0	1	1	0	0	1.0625
0	1	0	1	1	0	1	1.0500
0	1	0	1	1	1	0	1.0375
0	1	0	1	1	1	1	1.0250
0	1	1	0	0	0	0	1.0125
0	1	1	0	0	0	1	1.0000
0	1	1	0	0	1	0	0.9875
0	1	1	0	0	1	1	0.9750
0	1	1	0	1	0	0	0.9625
0	1	1	0	1	0	1	0.9500
0	1	1	0	1	1	0	0.9375
0	1	1	0	1	1	1	0.9250
0	1	1	1	0	0	0	0.9125
0	1	1	1	0	0	1	0.9000
0	1	1	1	0	1	0	0.8875
0	1	1	1	0	1	1	0.8750
0	1	1	1	1	0	0	0.8625
0	1	1	1	1	0	1	0.8500
0	1	1	1	1	1	0	0.8375
0	1	1	1	1	1	1	0.8250
1	0	0	0	0	0	0	0.8125
1	0	0	0	0	0	1	0.8000
1	0	0	0	0	1	0	0.7875
1	0	0	0	0	1	1	0.7750
1	0	0	0	1	0	0	0.7625
1	0	0	0	1	0	1	0.7500
1	0	0	0	1	1	0	0.7375
1	0	0	0	1	1	1	0.7250
1	0	0	1	0	0	0	0.7125
1	0	0	1	0	0	1	0.7000

The VID specification for the processor is defined by the *Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines*.

The processor uses seven voltage identification pins, VID[6:0], to support automatic selection of power supply voltages. The VID pins for the processor are CMOS outputs driven by the processor VID circuitry. Table 3 specifies the voltage level corresponding

to the state of VID[6:0]. A 1 in this refers to a high-voltage level and a 0 refers to low-voltage level. For more details about VR design to support the processor power supply requirements, refer to the *Voltage Regulator-Down (VRD) 11.0 Processor Power Delivery Design Guidelines.*

VRD11 has 8 VID pins (VID[7:0]) compared to 7 VID pins for the processor. VRD11 VID[n] should be connected to processor VID[n-1]. VRD11 VID[0] should be connected to V_{SS}.

Table 4. Processor VID Pin to VRD11 VID Pin Mapping

Processor VID Pin	Map to VRD11 VID Pin
6	7
5	6
4	5
3	4
2	3
1	2
0	1
	0 (tie to ground)

Power source characteristics must be stable whenever the supply to the voltage regulator is stable.

3.5 Catastrophic Thermal Protection

The processor supports the THERMTRIP# signal for catastrophic thermal protection. An external thermal sensor should also be used to protect the processor and the system against excessive temperature. Even with the activation of THERMTRIP#, which halts all processor internal clocks and activities, leakage current can be high enough such that the processor cannot be protected in all conditions without the removal of power to the processor. If the external thermal sensor detects a catastrophic processor temperature of 125 °C (maximum), or if the THERMTRIP# signal is asserted, the V_{CC} supply to the processor must be turned off within 500 ms to prevent permanent silicon damage due to thermal runaway of the processor. THERMTRIP functionality is not ensured if the PWRGOOD signal is not asserted.

3.6 Reserved and Unused Pins

All RESERVED (RSVD) pins must remain unconnected. Connection of these pins to V_{CCP}, V_{SS}, or to any other signal (including each other) can result in component malfunction or incompatibility with future processors. See section Section 4.2 for a pin listing of the processor and the location of all RSVD pins.

For reliable operation, always connect unused inputs or bidirectional signals to an appropriate signal level. Unused active low AGTL+ inputs may be left as no connects if AGTL+ termination is provided on the processor silicon. Unused active high inputs should be connected through a resistor to ground (V_{SS}). Unused outputs can be left unconnected.

3.7 FSB Frequency Select Signals (BSEL[2:0])

Only 133 MHz is supported by the processor. The BSEL[2:0] signals need to be set accordingly to select the frequency of the processor input clock (BCLK[1:0]). These signals should be connected to the clock chip and the appropriate chipset on the platform. The BSEL encoding for BCLK[1:0] is shown in Table 5.

Table 5. BSEL[2:0] Encoding for BCLK Frequency

BSEL[2]	BSEL[1]	BSEL[0]	BCLK Frequency
L	L	H	133 MHz

NOTE: All other bus selections are reserved.

3.8 FSB Signal Groups

To simplify the following discussion, the FSB signals have been combined into groups by buffer type. AGTL+ input signals have differential input buffers, which use GTLREF as a reference level. In this document, the term “AGTL+ Input” refers to the AGTL+ input group as well as the AGTL+ I/O group when receiving. Similarly, “AGTL+ Output” refers to the AGTL+ output group as well as the AGTL+ I/O group when driving.

With the implementation of a source synchronous data bus comes the need to specify two sets of timing parameters. One set is for common clock signals, which are dependent upon the rising edge of BCLK0 (ADS#, HIT#, HITM#, etc.) and the second set is for the source synchronous signals which are relative to their respective strobe lines (data and address) as well as the rising edge of BCLK0. Asychronous signals are still present (A20M#, IGNNE#, etc.) and can become active at any time during the clock cycle. Table 6 identifies which signals are common clock, source synchronous, and asynchronous.

Table 6. FSB Pin Groups

Signal Group	Type	Signals[1]	
AGTL+ Common Clock Input	Synchronous to BCLK[1:0]	BPRI#, DEFER#, PREQ#, RESET#, RS[2:0]#, TRDY#, DPWR#	
AGTL+ Common Clock I/O	Synchronous to BCLK[1:0]	ADS#, BNR#, BPM[3:0]#, BR0#, DBSY#, DRDY#, HIT#, HITM#, LOCK#, PRDY#	
AGTL+ Source Synchronous I/O	Synchronous to assoc. strobe	**Signals**	**Associated Strobe**
		REQ[4:0]#, A[16:3]#	ADSTB[0]#
		A[35:17]#	ADSTB[1]#
		D[15:0]#, DBI[0]#, DINV[0]#	DSTBP[0]#, DSTBN[0]#
		D[31:16]#, DBI[1]#, DINV[0]#	DSTBP[1]#, DSTBN[1]#
		D[47:32]#, DBI[2]#, DINV[0]#	DSTBP[2]#, DSTBN[2]#
		D[63:48]#, DBI[3]#, DINV[0]#	DSTBP[3]#, DSTBN[3]#
AGTL+ Strobes	Synchronous to BCLK[1:0]	ADSTB[1:0]#, DSTBP[3:0]#, DSTBN[3:0]#	
CMOS Input	Asynchronous	IGNNE#, INIT#, LINT0/INTR, LINT1/NMI, PWRGOOD, SMI#	
Open Drain Output	Asynchronous	FERR#, IERR#, THERMTRIP#	

Table 6. FSB Pin Groups

Signal Group	Type	Signals[1]
Open Drain I/O	Asynchronous	PROCHOT#[2]
CMOS Output	Asynchronous	VID[6:0], BSEL[2:0]
CMOS Input	Synchronous to TCK	TCK, TDI, TMS, TRST#
Open Drain Output	Synchronous to TCK	TDO
FSB Clock	Clock	BCLK[1:0]
Power/Other		COMP[3:0], GTLREF, THRMDA, THRMDC, VCCA, VCCP, VTT, VCC_SENSE, VSS, VSS_SENSE, VCCQ[1:0]

NOTES:
1. In processor systems where there is no debug port implemented on the system board, these signals are used to support a debug port interposer. In systems with the debug port implemented on the system board, these signals are no connects.
2. PROCHOT# signal type is open drain output and CMOS input.
3. On die termination differs from other AGTL+ signals.

3.9 CMOS Asynchronous Signals

CMOS input signals are shown in Table 6. Legacy output FERR#, IERR#, and other non-AGTL+ signals (THERMTRIP# and PROCHOT#) use Open Drain output buffers. These signals do not have setup or hold time specifications in relation to BCLK[1:0]. However, all of the CMOS signals are required to be asserted for more than 4 BCLKs for the processor to recognize them. See Section 3.11 for the DC specifications for the CMOS signal groups.

3.10 Maximum Ratings

Table 7 specifies absolute maximum and minimum ratings. Within functional operation limits, functionality and long-term reliability can be expected.

At conditions outside functional operation condition limits, but within absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. If a device is returned to conditions within functional operation limits after having been subjected to conditions outside these limits, but within the absolute maximum and minimum ratings, the device may be functional, but with its lifetime degraded depending on exposure to conditions exceeding the functional operation condition limits.

At conditions exceeding absolute maximum and minimum ratings, neither functionality nor long term reliability can be expected. Moreover, if a device is subjected to these conditions for any length of time then, when returned to conditions within the functional operating condition limits, it will either not function or its reliability will be severely degraded.

Although the processor contains protective circuitry to resist damage from static electric discharge, precautions should always be taken to avoid high static voltages or electric fields.

Table 7. Processor Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Unit	Notes[1]
$T_{STORAGE}$	Processor Storage Temperature	-40	85	°C	2,3,4
V_{CC}	Any Processor Supply Voltage with Respect to V_{SS}	-0.3	1.55	V	5
VinAGTL+	AGTL+ Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.55	V	
VinAsynch_CMOS	CMOS Buffer DC Input Voltage with Respect to V_{SS}	-0.1	1.55	V	

NOTES:
1. For functional operation, all processor electrical, signal quality, mechanical and thermal specifications must be satisfied.
2. Storage temperature is applicable to storage conditions only. In this scenario, the processor must not receive a clock, and no lands can be connected to a voltage bias. Storage within these limits will not affect the long term reliability of the device. For functional operation, refer to the processor case temperature specifications.
3. This rating applies to the processor and does not include any tray or packaging.
4. Failure to adhere to this specification can affect the long term reliability of the processor.
5. The V_{CC} max supported by the process is 1.2 V but the parameter can change (burnin voltage is higher).

3.11 Processor DC Specifications

The processor DC specifications in this section are defined at the processor core (pads) unless noted otherwise. See Chapter 4 for the pin signal definitions and signal pin assignments. Most of the signals on the FSB are in the AGTL+ signal group. The DC specifications for these signals are listed in Table 10. DC specifications for the CMOS group are listed in Table 11.

Table 10 through Table 12 list the DC specifications for the processor and are valid only while meeting specifications for junction temperature, clock frequency, and input voltages. Unless specified otherwise, all specifications for the processor are at T_J = 90 °C. Care should be taken to read all notes associated with each parameter.

Table 8. Voltage and Current Specifications

Symbol	Parameter		Min	Typ	Max	Unit	Notes[6]
FSB Frequency	BCLK Frequency		132.6	133.33	133.5	MHz	
V_{TT}	FSB AGTL+ termination voltage with respect to V_{SS}		1.05	1.10	1.15	V	
V_{CCP}	Vcc Core voltage with respect to V_{SS}		0.7	—	1.2	V	7,8
V_{CCA}	PLL Supply voltage		1.425	1.5	1.575	V	
$V_{CC\ BOOT}$	Default V_{CCP} voltage for initial power up		—	1.10		V	
I_{TT}	$I_{CC\ for}$ V_{TT} supply after V_{CCP} stable $I_{CC\ for}$ V_{TT} supply at startup		— —	— —	1.5 2.5	A	3
I_{CCDES}	I_{CC} for Processors Recommended Design Target (Estimated)		—	—	4	A	3
I_{CC}	I_{CC} for processors		—	—			
	Processor Number	Core Frequency					
	230	1.6 GHz @ V_{CCP} (AVID controlled)	—	—	4	A	1, 2
I_{AH}	I_{CC} Auto-Halt		—	—	2.0	A	1, 2
dI_{CC}/dt	V_{CCP} Power Supply Current Slew Rate at Processor Package Pin (Estimated)		—	—	2.5	A/µs	4, 5
I_{CCA}	I_{CC} for V_{CCA} Supply		—	—	130	mA	

NOTES:

1. Specified at 90 °C T_J.
2. Specified at the nominal V_{CCP}.
3. Refer to the *Voltage Regulator-Down (VRD) 11.0 - Processor Power Delivery Design Guidelines* for design target capability.
4. Measured at the bulk capacitors on the motherboard.
5. Based on simulations and averaged over the duration of any change in current. Specified by design/ characterization at nominal V_{CCP}. Not 100% tested.
6. Unless otherwise noted, all specifications in this table are based on estimates and simulations or empirical data. These specifications will be updated with characterized data from silicon measurements at a later date.
7. V_{CCP} is determined by processor VID[6:0] pins. Each processor is programmed with a maximum valid voltage identification value (VID), which is set at manufacturing and can not be altered. Individual maximum VID values are calibrated during manufacturing such that two processors at the same frequency may have different settings within VID range. Refer to VID Table 3 for the specific voltages corresponding to VID[6:0] codes.
8. This is the V_{CCP} range, not the absolute voltage set for the core. The V_{CCP} tolerance should be ±50 mV, inclusive of ripple, VR tolerance and transient (droop and overshoot).
9. Since the processor is soldered down with no loadline and no dynamic VID, there is no “socket load line slope (SKT_LL)”; “socket load line tolerance band” but only “Tolerance Band (TOB)” of 50 mV; no “maximum overshoot above VID (OS_AMP)”; no “maximum overshoot time duration above VID (OS_TIME)”; no “peak to peak ripple amplitude (RIPPLE)”; no “thermal compensation voltage drift (THERMAL_DRIF)”; no “maximum DC test (Current I_DC_MAX)”; no “minimum DC test (Current I_DC_MIN)”; “Voltage Regulator Thermal Design Current (VR_TDC_)” of 3.64 A; “current step rise time (I_RISE) of 2.5 A/us”.

Table 9. FSB Differential BCLK Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{IH}	Input High Voltage	—	—	1.15	V	7, 8
V_{IL}	Input Low Voltage	—	—	-0.3	V	7, 8
V_{CROSS}	Crossing Voltage	0.3	—	0.55	V	2, 7, 9
ΔV_{CROSS}	Range of Crossing Points	—	—	140	mV	2, 7, 5
V_{SWING}	Differential Output Swing	300	—	—	mV	6
I_{LI}	Input Leakage Current	-5	—	+5	µA	3
Cpad	Pad Capacitance	1.2	1.45	2.0	pF	4

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Crossing Voltage is defined as absolute voltage where rising edge of BCLK0 is equal to the falling edge of BCLK1.
3. For Vin between 0 V and V_{IH}.
4. Cpad includes die capacitance only. No package parasitics are included.
5. ΔV_{CROSS} is defined as the total variation of all crossing voltages as defined in note 2.
6. Measurement taken from differential waveform.
7. Measurement taken from single-ended waveform.
8. “Steady state” voltage, not including Overshoots or Undershoots.
9. Only applies to the differential rising edge (clock rising and clock# falling).

Table 10. AGTL+ /CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{TT}	I/O Voltage	1.05	1.10	1.15	V	11
GTLREF	GTL Reference Voltage	—	2/3 V_{TT}	—	V	5
R_{COMP}	Compensation Resistor COMP[0] & COMP[2] COMP[1] & COMP[3]	 24.75 49.5	 25 50	 25.25 50.5	Ω	9, 11
R_{ODT}	Termination Resistor	—	50	—	Ω	10
V_{IH}	Input High Voltage	GTLREF+0.10	V_{TT}	V_{TT}+0.10	V	3,5
V_{IL}	Input Low Voltage	-0.10	0	GTLREF-0.10	V	2,4
V_{OH}	Output High Voltage	V_{TT}-0.10	V_{TT}	V_{TT}	V	5
R_{TT}	Termination Resistance	45	50	55	Ω	6
R_{ON} (GTL mode)	GTL Buffer on Resistance	—	8	—	Ω	
I_{LI}	Input Leakage Current	—	—	±100	µA	7
Cpad	Pad Capacitance	1.6	2.1	2.55	pF	8

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. V_{IL} is defined as the maximum voltage level at a receiving agent that will be interpreted as a logical low value.
3. V_{IH} is defined as the minimum voltage level at a receiving agent that will be interpreted as a logical high value.
4. V_{IH} and V_{OH} may experience excursions above V_{TT}. However, input signal drivers must comply with the signal quality specifications.
5. GTLREF should be generated from V_{TT} with a 1% tolerance resistor divider. The V_{TT} referred to in these specifications is the instantaneous V_{TT}.

6. R_{TT} is the on-die termination resistance measured at V_{OL} of the AGTL+ output driver. Measured at $0.31*V_{TT}$. R_{TT} is connected to V_{TT} on die.
7. Specified with on-die R_{TT} and R_{ON} are turned off. Vin between 0 and V_{TT}.
8. Cpad includes die capacitance only. No package parasitics are included.
9. This is the external resistor on the comp pins.
10. On-die termination resistance, measured at $0.33*V_{TT}$.
11. R_{COMP} resistance must be provided on the system board with 1% resistors.

Table 11. Legacy CMOS Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{TT}	I/O Voltage	1.05	1.10	1.15	V	
V_{IH}	Input High Voltage	$0.7*V_{TT}$	V_{TT}	V_{TT} + 0.1	V	2
V_{IL}	Input Low Voltage CMOS	-0.10	0.00	$0.3*V_{TT}$	V	2
V_{OH}	Output High Voltage	$0.9*V_{TT}$	V_{TT}	V_{TT} + 0.1	V	2
V_{OL}	Output Low Voltage	-0.10	0	$0.1*V_{TT}$	V	2
I_{OH}	Output High Current	1.5	—	4.1	mA	4
I_{OL}	Output Low Current	1.5	—	4.1	mA	3
I_{LI}	Input Leakage Current		—	± 100	µA	5
Cpad1	Pad Capacitance	1.6	2.1	2.55	pF	6
Cpad2	Pad Capacitance for CMOS Input	0.95	1.2	1.45		7

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. The V_{TT} referred to in these specifications refers to instantaneous V_{TT}.
3. Measured at $0.1*V_{TT}$.
4. Measured at $0.9*V_{TT}$.
5. For Vin between 0 V and V_{TT}. Measured when the driver is tri-stated.
6. Cpad1 includes die capacitance only for DPRSTP#, DPSLP#, PWRGOOD. No package parasitics are included.
7. Cpad2 includes die capacitance for all other CMOS input signals. No package parasitics are included.

Table 12. Open Drain Signal Group DC Specifications

Symbol	Parameter	Min	Typ	Max	Unit	Notes[1]
V_{OH}	Output High Voltage	V_{TT} – 5%	V_{TT}	V_{TT} + 5%	V	3
V_{OL}	Output Low Voltage	0	—	0.20	V	
I_{OL}	Output Low Current	16	—	50	mA	2
I_{LO}	Output Leakage Current	—	—	±200	µA	4
Cpad	Pad Capacitance	1.9	2.2	2.45	pF	5

NOTES:
1. Unless otherwise noted, all specifications in this table apply to all processor frequencies.
2. Measured at 0.2 V.
3. V_{OH} is determined by value of the external pull-up resistor to V_{TT}.
4. For Vin between 0 V and V_{OH}.
5. Cpad includes die capacitance only. No package parasitics are included.

3.12 AGTL+ FSB Specifications

Termination resistors are not required for most AGTL+ signals, as these are integrated into the processor silicon.

Valid high and low levels are determined by the input buffers, which compare a signal's voltage with a reference voltage called GTLREF (known as V_{REF} in previous documentation).

Table 10 lists the GTLREF specifications. The AGTL+ reference voltage (GTLREF) should be generated on the system board using high precision voltage divider circuits. It is important that the system board impedance is held to the specified tolerance, and that the intrinsic trace capacitance for the AGTL+ signal group traces is known and well-controlled.

§ §

4 Package Mechanical Specifications and Ball Information

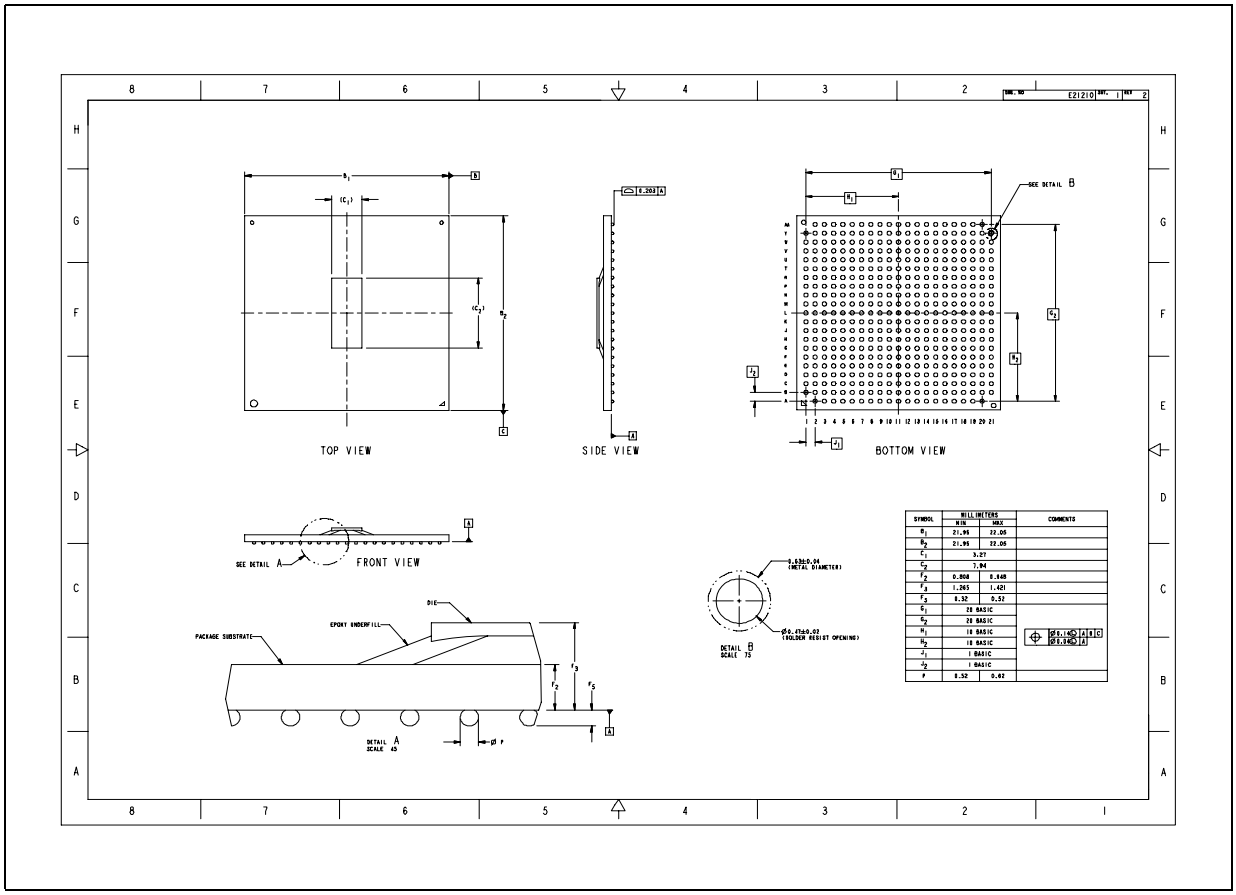
This chapter provides the package specifications, pinout assignments, and signal description.

4.1 Package Mechanical Specifications

The processor is available in 512 kB, 437 pins in FCBGA package.

4.1.1 Package Mechanical Drawings

Figure 2. Package Mechanical Drawing



4.1.2 Package Loading Specifications

The package loading is 5 lb max static compressive.

4.1.3 Processor Mass Specifications

The processor mass is 1.4 g.

4.2 Processor Ball Assignment

Figure 3 and Figure 4 are graphic representations of the processor ball assignments. Table 13 lists the ballout by signal name.

Figure 3. Ballout Diagram (Top View, Left Side)

	1	2	3	4	5	6	7	8	9	10	11	
A		VSS	RSVD	VSS	D[54]#	D[56]#	GTLREF	VSS	VCCQ0	VCCP	VCCP	A
B	VSS	VSS	D[60]#	D[52]#	VSS	D[59]#	CMREF	VSS	VCCQ0	VCCP	VCCP	B
C	RSVD	D[48]#	D[55]#	D[61]#	DINV[3]	D[58]#	D[62]#	VSS	VTT	VCCP	VCCP	C
D	VSS	D[63]#	D[51]#	RSVD	VSS	NC	VCCA	VSS	VTT	VCCP	VCCP	D
E	D[53]#	DSTBN[3]	VSS	THRMDA	THRMDC	VSS	VSS	VSS	VTT	VCCP	VCCP	E
F	D[50]#	D[57]#	DSTBP[3]	VSS	VSS	VSS	VSS	VTT	VTT	VCCP	VCCP	F
G	VSS	D[49]#	D[40]#	VSS	BSEL[2]	NC	VSS	VTT	VSS	VCCP	VCCP	G
H	D[46]#	D[41]#	VSS	VSS	BSEL[1]	NC	VSS	VTT	VSS	VCCP	VCCP	H
J	D[47]#	D[45]#	D[38]#	IGNNE#	VSS	BSEL[0]	VSS	VTT	VSS	VCCP	VCCP	J
K	VSS	DSTBN[2]	DSTBP[2]	NC	NC	VSS	VSS	VTT	VSS	VCCP	VCCP	K
L	DINV[2]	D[43]#	VSS	VSS	VSS	VSS	VSS	VTT	VSS	VCCP	VCCP	L
M	VSS	D[36]#	D[44]#	RSVD	VSS	EXTBGREF	VSS	VTT	VSS	VCCP	VCCP	M
N	D[35]#	D[42]#	D[39]#	VSS	VSS	RSVD	VSS	VTT	VSS	VCCP	VCCP	N
P	D[34]#	D[37]#	VSS	VSS	VSS	VSS	VSS	VTT	VSS	VCCP	VCCP	P
R	VSS	D[33]#	D[32]#	RSVD	VSS	RSVD	VSS	VTT	VSS	VCCP	VCCP	R
T	COMP[0]	COMP[1]	D[28]#	VSS	VSS	RSVD	VSS	VTT	VSS	VSS	VSS	T
U	D[19]#	D[27]#	VSS	DPWR#	RSVD	VSS	VSS	VTT	VTT	VTT	VTT	U
V	VSS	D[30]#	D[26]#	VSS	RSVD	VSS	VSS	VSS	RSVD	VTT	BCLK[0]	V
W	VSS	D[25]#	D[18]#	D[31]#	VSS	D[21]#	D[20]#	VSS	D[15]#	D[1]#	VSS	W
Y	VSS	VSS	D24[]#	DSTBN[1]	DSTBP[1]	DINV[1]	D[22]#	D[17]#	D[8]#	D[7]#	D[0]#	Y
AA		VSS	VSS	VSS	D[16]#	D[23]#	VSS	D[29]#	D[14]#	VSS	D[4]#	AA
	1	2	3	4	5	6	7	8	9	10	11	

Figure 4. Ballout Diagram (Top View, Right Side)

	12	13	14	15	16	17	18	19	20	21	
A	VCCP	RSVD	A[35]#	VSS	A[20]#	A[32]#	VSS	VSS	VSS		A
B	VCCP	VSS	A[33]#	A[34]#	A[29]#	A[30]#	A[27]#	ADSTB[1]#	VSS	VSS	B
C	VCCP	VCCSENSE	A[22]#	A[28]#	A[31]#	VSS	A[23]#	A[17]#	A[24]#	RSVD	C
D	VCCP	VSSSENSE	VSS	RESET#	VID[1]	RSVD	VSS	A[21]#	A[26]#	VSS	D
E	VCCP	VTT	VTT	VSS	VSS	VID[5]	VID[2]	VSS	A[25]#	A[19]#	E
F	VCCP	VTT	VTT	VID[0]	IERR#	VSS	VSS	A[18]#	COMP[2]	COMP[3]	F
G	VCCP	VSS	VTT	VID[3]	VID[4]	PROCHOT#	VID[6]	REQ[2]#	A[9]#	VSS	G
H	VCCP	VSS	VTT	BPM[2]#	VSS	RSVD	VSS	VSS	A[4]#	A[11]#	H
J	VCCP	VSS	VTT	BPM[3]#	PREQ#	VSS	BPM[1]#	A[7]#	A[15]#	REQ[1]#	J
K	VCCP	VSS	VTT	VSS	TRST#	BPM[0]#	PRDY#	A[14]#	ADSTB[0]#	VSS	K
L	VCCP	VSS	VTT	VSS	NC	TMS	VSS	VSS	A[12]#	A[16]#	L
M	VCCP	VSS	VTT	NC	TDO	TCK	RSVD	A[10]#	A[13]#	VSS	M
N	VCCP	VSS	VTT	FORCEPR#	TDI	VSS	SLP#	A[8]#	A[5]#	REQ[0]#	N
P	VCCP	VSS	VTT	VSS	VSS	RSVD	VSS	VSS	REQ[3]#	A[3]#	P
R	VCCP	VSS	VTT	LINT1	STPCLK#	DPSLP#	DPRSTP#	REQ[4]#	A[6]#	VSS	R
T	VSS	VSS	VTT	LINT0	FERR#	RSVD	VSS	DRDY#	BR0#	DEFER#	T
U	VTT	VTT	VTT	VSS	VSS	SMI#	A20M	VSS	RS[2]#	BPRI#	U
V	BCLK[1]	VSS	VSS	BR1#	INIT#	PWRGOOD	VSS	ADS	HITM#	VSS	V
W	D[5]#	D[13]#	VSS	D[10]#	DINV[0]	VSS	RS[0]#	TRDY#	LOCK#	VSS	W
Y	D[2]#	D[9]#	DSTBN[0]	DSTBP[0]	D[12]#	RS[1]#	DBSY#	BNR#	VSS	VSS	Y
AA	VSS	D[11]#	D[3]#	VSS	D[6]#	HIT#	VSS	VSS	VSS		AA
	12	13	14	15	16	17	18	19	20	21	

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
A[3]#	P21
A[4]#	H20
A[5]#	N20
A[6]#	R20
A[7]#	J19
A[8]#	N19
A[9]#	G20
A[10]#	M19
A[11]#	H21
A[12]#	L20
A[13]#	M20
A[14]#	K19
A[15]#	J20
A[16]#	L21
A[17]#	C19
A[18]#	F19
A[19]#	E21
A[20]#	A16
A[21]#	D19
A[22]#	C14
A[23]#	C18
A[24]#	C20
A[25]#	E20
A[26]#	D20
A[27]#	B18
A[28]#	C15
A[29]#	B16
A[30]#	B17
A[31]#	C16
A[32]#	A17
A[33]#	B14
A[34]#	B15
A[35]#	A14
A20M#	U18
ADS#	V19
ADSTB[0]#	K20
ADSTB[1]#	B19

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
BCLK[0]	V11
BCLK[1]	V12
BNR#	Y19
BPM[0]#	K17
BPM[1]#	J18
BPM[2]#	H15
BPM[3]#	J15
BPRI#	U21
BR0#	T20
BR1#	V15
BSEL[0]	J6
BSEL[1]	H5
BSEL[2]	G5
CMREF	B7
COMP[0]	T1
COMP[1]	T2
COMP[2]	F20
COMP[3]	F21
D[0]#	Y11
D[1]#	W10
D[2]#	Y12
D[3]#	AA14
D[4]#	AA11
D[5]#	W12
D[6]#	AA16
D[7]#	Y10
D[8]#	Y9
D[9]#	Y13
D[10]#	W15
D[11]#	AA13
D[12]#	Y16
D[13]#	W13
D[14]#	AA9
D[15]#	W9
D[16]#	AA5
D[17]#	Y8
D[18]#	W3

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
D[19]#	U1
D[20]#	W7
D[21]#	W6
D[22]#	Y7
D[23]#	AA6
D[24]#	Y3
D[25]#	W2
D[26]#	V3
D[27]#	U2
D[28]#	T3
D[29]#	AA8
D[30]#	V2
D[31]#	W4
D[32]#	R3
D[33]#	R2
D[34]#	P1
D[35]#	N1
D[36]#	M2
D[37]#	P2
D[38]#	J3
D[39]#	N3
D[40]#	G3
D[41]#	H2
D[42]#	N2
D[43]#	L2
D[44]#	M3
D[45]#	J2
D[46]#	H1
D[47]#	J1
D[48]#	C2
D[49]#	G2
D[50]#	F1
D[51]#	D3
D[52]#	B4
D[53]#	E1
D[54]#	A5
D[55]#	C3

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
D[56]#	A6
D[57]#	F2
D[58]#	C6
D[59]#	B6
D[60]#	B3
D[61]#	C4
D[62]#	C7
D[63]#	D2
DBSY#	Y18
DEFER#	T21
DINV[0]#	W16
DINV[1]#	Y6
DINV[2]#	L1
DINV[3]#	C5
DPRSTP#	R18
DPSLP#	R17
DPWR#	U4
DRDY#	T19
DSTBN[0]#	Y14
DSTBN[1]#	Y4
DSTBN[2]#	K2
DSTBN[3]#	E2
DSTBP[0]#	Y15
DSTBP[1]#	Y5
DSTBP[2]#	K3
DSTBP[3]#	F3
FERR#	T16
FORCEPR#	N15
GTLREF	A7
HIT#	AA17
HITM#	V20
IERR#	F16
IGNNE#	J4
INIT#	V16
LINT0	T15
LINT1	R15
LOCK#	W20

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
NC	D6
NC	G6
NC	H6
NC	K4
NC	K5
NC	M15
NC	L16
PRDY#	K18
PREQ#	J16
PROCHOT#	G17
PWRGOOD	V17
REQ[0]#	N21
REQ[1]#	J21
REQ[2]#	G19
REQ[3]#	P20
REQ[4]#	R19
RESET#	D15
RS[0]#	W18
RS[1]#	Y17
RS[2]#	U20
RSVD	U5
RSVD	V5
RSVD	P17
RSVD	D17
RSVD	M18
RSVD	T17
RSVD	A13
RSVD	R6
RSVD	N6
RSVD	T6
RSVD	A3
RSVD	C1
RSVD	C21
RSVD	V9
RSVD	R4
RSVD	M4
RSVD	D4

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
VTT	E13
VTT	E14
VTT	F13
VTT	F14
SLP#	N18
SMI#	U17
STPCLK#	R16
TCK	M17
TDI	N16
TDO	M16
EXTBGREF	M6
THERMTRIP#	H17
THRMDA	E4
THRMDC	E5
TMS	L17
TRDY#	W19
TRST#	K16
VCC	A10
VCC	A11
VCC	A12
VCC	B10
VCC	B11
VCC	B12
VCC	C10
VCC	C11
VCC	C12
VCC	D10
VCC	D11
VCC	D12
VCC	E10
VCC	E11
VCC	E12
VCC	F10
VCC	F11
VCC	F12
VCC	G10
VCC	G11

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
VCC	G12
VCC	H10
VCC	H11
VCC	H12
VCC	J10
VCC	J11
VCC	J12
VCC	K10
VCC	K11
VCC	K12
VCC	L10
VCC	L11
VCC	L12
VCC	M10
VCC	M11
VCC	M12
VCC	N10
VCC	N11
VCC	N12
VCC	P10
VCC	P11
VCC	P12
VCC	R10
VCC	R11
VCC	R12
VCCA	D7
VTT	V10
VCCQ0	A9
VCCQ0	B9
VCC_SENSE	C13
VID[0]	F15
VID[1]	D16
VID[2]	E18
VID[3]	G15
VID[4]	G16
VID[5]	E17
VID[6]	G18

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
VSS	A2
VSS	A4
VSS	A8
VSS	A15
VSS	A18
VSS	A19
VSS	A20
VSS	B1
VSS	B2
VSS	B5
VSS	B8
VSS	B13
VSS	B20
VSS	B21
VSS	C8
VSS	C17
VSS	D1
VSS	D5
VSS	D8
VSS	D14
VSS	D18
VSS	D21
VSS	E3
VSS	E6
VSS	E7
VSS	E8
VSS	E15
VSS	E16
VSS	E19
VSS	F4
VSS	F5
VSS	F6
VSS	F7
VSS	F17
VSS	F18
VSS	G1
VSS	G4

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
VSS	G7
VSS	G9
VSS	G13
VSS	G21
VSS	H3
VSS	H4
VSS	H7
VSS	H9
VSS	H13
VSS	H16
VSS	H18
VSS	H19
VSS	J5
VSS	J7
VSS	J9
VSS	J13
VSS	J17
VSS	K1
VSS	K6
VSS	K7
VSS	K9
VSS	K13
VSS	K15
VSS	K21
VSS	L3
VSS	L4
VSS	L5
VSS	L6
VSS	L7
VSS	L9
VSS	L13
VSS	L15
VSS	L18
VSS	L19
VSS	M1
VSS	M5
VSS	M7

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
VSS	M9
VSS	M13
VSS	M21
VSS	N4
VSS	N5
VSS	N7
VSS	N9
VSS	N13
VSS	N17
VSS	P3
VSS	P4
VSS	P5
VSS	P6
VSS	P7
VSS	P9
VSS	P13
VSS	P15
VSS	P16
VSS	P18
VSS	P19
VSS	R1
VSS	R5
VSS	R7
VSS	R9
VSS	R13
VSS	R21
VSS	T4
VSS	T5
VSS	T7
VSS	T9
VSS	T10
VSS	T11
VSS	T12
VSS	T13
VSS	T18
VSS	U3
VSS	U6

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
VSS	U7
VSS	U15
VSS	U16
VSS	U19
VSS	V1
VSS	V4
VSS	V6
VSS	V7
VSS	V8
VSS	V13
VSS	V14
VSS	V18
VSS	V21
VSS	W1
VSS	W5
VSS	W8
VSS	W11
VSS	W14
VSS	W17
VSS	W21
VSS	Y1
VSS	Y2
VSS	Y20
VSS	Y21
VSS	AA2
VSS	AA3
VSS	AA4
VSS	AA7
VSS	AA10
VSS	AA12
VSS	AA15
VSS	AA18
VSS	AA19
VSS	AA20
VSS_SENSE	D13
VTT	C9
VTT	D9

Table 13.Ballout Arranged By Signal Name

Signal Name	Ball #
VTT	E9
VTT	F8
VTT	F9
VTT	G8
VTT	G14
VTT	H8
VTT	H14
VTT	J8
VTT	J14
VTT	K8
VTT	K14
VTT	L8
VTT	L14
VTT	M8
VTT	M14
VTT	N8
VTT	N14
VTT	P8
VTT	P14
VTT	R8
VTT	R14
VTT	T8
VTT	T14
VTT	U8
VTT	U9
VTT	U10
VTT	U11
VTT	U12
VTT	U13
VTT	U14

4.3 Signal Description

Table 14. Signal Description (Sheet 1 of 7)

Signal Name	Type	Description
A[35:3]#	I/O	A[35:3]# (Address) defines a 2^{36}-byte physical memory address space. In subphase 1 of the address phase, these pins transmit the address of a transaction. In sub-phase 2, these pins transmit transaction type information. These signals must connect the appropriate pins of both agents on the processor FSB. A[35:3]# are source synchronous signals and are latched into the receiving buffers by ADSTB[1:0]#. Address signals are used as straps, which are sampled before RESET# is de-asserted.
A20M#	I	If A20M# (Address-20 Mask) is asserted, the processor masks physical address bit 20 (A20#) before looking up a line in any internal cache and before driving a read/write transaction on the bus. Asserting A20M# emulates the 8086 processor's address wrap-around at the 1-MB boundary. Assertion of A20M# is only supported in real mode. A20M# is an asynchronous signal. However, to ensure recognition of this signal following an input/output write instruction, it must be valid along with the TRDY# assertion of the corresponding input/output Write bus transaction.
ADS#	I/O	ADS# (Address Strobe) is asserted to indicate the validity of the transaction address on the A[35:3]# and REQ[4:0]# pins. All bus agents observe the ADS# activation to begin parity checking, protocol checking, address decode, internal loop, or deferred reply ID match operations associated with the new transaction.
ADSTB[1:0]#	I/O	Address strobes are used to latch A[35:3]# and REQ[4:0]# on their rising and falling edges. Strobes are associated with signals as shown below. **Signals** — **Associated Strobe** REQ[4:0]#, A[16:3]# — ADSTB[0]# A[35:17]# — ADSTB[1]#
BCLK[1:0]	I	The differential pair BCLK (Bus Clock) determines the FSB frequency. All FSB agents must receive these signals to drive their outputs and latch their inputs. All external timing parameters are specified with respect to the rising edge of BCLK0 crossing VCROSS.
BNR#	I/O	BNR# (Block Next Request) is used to assert a bus stall by any bus agent who is unable to accept new bus transactions. During a bus stall, the current bus owner cannot issue any new transactions.
BPM[0]#	O	BPM[3:0]# (Breakpoint Monitor) are breakpoint and performance monitor signals. They are outputs from the processor which indicate the status of breakpoints and programmable counters used for monitoring processor performance. BPM[3:0]# should connect the appropriate pins of all FSB agents.This includes debug or performance monitoring tools.
BPM[1]#	I/O	
BPM[2]#	O	
BPM[3]#	I/O	

Table 14. Signal Description (Sheet 2 of 7)

Signal Name	Type	Description
BPRI#	I	BPRI# (Bus Priority Request) is used to arbitrate for ownership of the FSB. It must connect the appropriate pins of both FSB agents. Observing BPRI# active (as asserted by the priority agent) causes the other agent to stop issuing new requests, unless such requests are part of an ongoing locked operation. The priority agent keeps BPRI# asserted until all of its requests are completed; then, releases the bus by de-asserting BPRI#.
BR[1:0]#	I/O	BR0# is used by the processor to request the bus.
BSEL[2:0]	O	BSEL[2:0] (Bus Select) are used to select the processor input clock frequency. For the Intel® Atom™ processor 200 series, BSEL is fixed to operate at 133-MHz BCLK frequency.
COMP[3:0]	PWR	COMP[3:0] must be terminated on the system board using precision (1% tolerance) resistors.
D[63:0]#	I/O	D[63:0]# (Data) are the data signals. These signals provide a 64-bit data path between the FSB agents, and must connect the appropriate pins on both agents.The data driver asserts DRDY# to indicate a valid data transfer. D[63:0]# are quad-pumped signals and will thus be driven four times in a common clock period. D[63:0]# are latched off the falling edge of both DSTBP[3:0]# and DSTBN[3:0]#. Each group of 16 data signals correspond to a pair of one DSTBP# and one DSTBN#. The following table shows the grouping of data signals to data strobes and DINV#. **Quad-Pumped Signal Groups** **Data Group — DSTBN#/DSTBP# — DINV#** D[15:0]# — 0 — 0 D[31:16]# — 1 — 1 D[47:32]# — 2 — 2 D[63:48]# — 3 — 3 Furthermore, the DINV# pins determine the polarity of the data signals. Each group of 16 data signals corresponds to one DINV# signal. When the DINV# signal is active, the corresponding data group is inverted and therefore, sampled active high.
DBSY#	I/O	DBSY# (Data Bus Busy) is asserted by the agent responsible for driving data on the FSB to indicate that the data bus is in use. The data bus is released after DBSY# is de-asserted. This signal must connect the appropriate pins on both FSB agents.
DEFER#	I	DEFER# is asserted by an agent to indicate that a transaction cannot be guaranteed in-order completion. Assertion of DEFER# is normally the responsibility of the addressed memory or Input/Output agent. This signal must connect the appropriate pins of both FSB agents.

Table 14. Signal Description (Sheet 3 of 7)

Signal Name	Type	Description
DINV[3:0]#	I	DINV[3:0]# (Data Bus Inversion) are source synchronous and indicate the polarity of the D[63:0]# signals. The DINV[3:0]# signals are activated when the data on the data bus is inverted. The bus agent will invert the data bus signals if more than half the bits, within the covered group, would change level in the next cycle. DINV[3:0]# Assignment To Data Bus is provided below: **Bus Signal** **Data Bus Signals** DINV[3]# D[63:48]# DINV[2]# D[47:32]# DINV[1]# D[31:16]# DINV[0]# D[15:0]#
DPSLP#	I	DPSLP#, when asserted on the platform, causes the processor to transition from the Sleep State to the Deep Sleep state. To return to the Sleep State, DPSLP# must be de-asserted. DPSLP# is driven by the chipset. This signal is not used for nettop 2008 platforms and is tied to V_{TT}.
DPRSTP#	I	DPRSTP#, when asserted on the platform, causes the processor to transition from the Deep Sleep State to the Deeper Sleep state. To return to the Deep Sleep State, DPRSTP# must be de-asserted. DPRSTP# is driven by the chipset. This signal is not used for nettop 2008 platforms and is tied to V_{TT}.
DPWR#	I	DPWR# is a control signal from the chipset used to reduce power on the processor data bus input buffers. This signal is not used for nettop 2008 platforms and is tied to V_{TT}.
DRDY#	I/O	DRDY# (Data Ready) is asserted by the data driver on each data transfer, indicating valid data on the data bus. In a multi-common clock data transfer, DRDY# may be de-asserted to insert idle clocks. This signal must connect the appropriate pins of both FSB agents.
DSTBN[3:0]#	I/O	Data strobe used to latch in D[63:0]#. **Signals** **Associated Strobe** D[15:0]# DINV[0]#, DSTBN[0]# D[31:16]# DINV[1]#, DSTBN[1]# D[47:32]# DINV[2]#, DSTBN[2]# D[63:48]# DINV[3]#, DSTBN[3]#
DSTBP[3:0]#	I/O	Data strobe used to latch in D[63:0]#. **Signals** **Associated Strobe** D[15:0]# DINV[0]#, DSTBP[0]# D[31:16]# DINV[1]#, DSTBP[1]# D[47:32]# DINV[2]#, DSTBP[2]# D[63:48]# DINV[3]#, DSTBP[3]#

Table 14. Signal Description (Sheet 4 of 7)

Signal Name	Type	Description
FERR#/PBE#	O	FERR# (Floating-point Error)/PBE# (Pending Break Event) is a multiplexed signal and its meaning is qualified with STPCLK#. When STPCLK# is not asserted, FERR#/PBE# indicates a floating point when the processor detects an unmasked floating-point error. FERR# is similar to the ERROR# signal on the Intel 387 coprocessor, and is included for compatibility with systems using MSDOS*- type floating-point error reporting. When STPCLK# is asserted, an assertion of FERR#/PBE# indicates that the processor has a pending break event waiting for service. The assertion of FERR#/PBE# indicates that the processor should be returned to the Normal state. When FERR#/PBE# is asserted, indicating a break event, it will remain asserted until STPCLK# is de-asserted. Assertion of PREQ# when STPCLK# is active will also cause an FERR# break event. For additional information on the pending break event functionality, including identification of support of the feature and enable/disable information, refer to Volume 3 of the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* and the *Intel® Processor Identification and CPUID Instruction Application Note*.
GTLREF	PWR	GTLREF determines the signal reference level for AGTL+ input pins. GTLREF should be set at 2/3 V_{TT}. GTLREF is used by the AGTL+ receivers to determine if a signal is a logical 0 or logical 1.
CMREF	PWR	CMOS signal reference voltage for data and address pin. Since CMOS signalling is not used, this is a no connect. Tie this to GTLREF as defensive design.
EXTBGREF	PWR	Follow exactly GTLREF connection method.
HIT# HITM#	I/O	HIT# (Snoop Hit) and HITM# (Hit Modified) convey transaction snoop operation results. Either FSB agent may assert both HIT# and HITM# together to indicate that it requires a snoop stall, which can be continued by reasserting HIT# and HITM# together.
IERR#	O	IERR# (Internal Error) is asserted by a processor as the result of an internal error. Assertion of IERR# is usually accompanied by a SHUTDOWN transaction on the FSB. This transaction may optionally be converted to an external error signal (e.g., NMI) by system core logic. The processor will keep IERR# asserted until the assertion of RESET#, BINIT#, or INIT#.
IGNNE#	I	IGNNE# (Ignore Numeric Error) is asserted to force the processor to ignore a numeric error and continue to execute non-control floating-point instructions. If IGNNE# is deasserted, the processor generates an exception on a non-control floating-point instruction if a previous floating-point instruction caused an error. IGNNE# has no effect when the NE bit in control register 0 (CR0) is set. IGNNE# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/ Output Write bus transaction.

Table 14. Signal Description (Sheet 5 of 7)

Signal Name	Type	Description
INIT#	I	INIT# (Initialization), when asserted, resets integer registers inside the processor without affecting its internal caches or floating-point registers. The processor then begins execution at the power-on Reset vector configured during power-on configuration. The processor continues to handle snoop requests during INIT# assertion. INIT# is an asynchronous signal. However, to ensure recognition of this signal following an Input/Output Write instruction, it must be valid along with the TRDY# assertion of the corresponding Input/Output Write bus transaction. INIT# must connect the appropriate pins of both FSB agents. If INIT# is sampled active on the active to inactive transition of RESET#, the processor reverses its FSB data and address signals internally to ease mother board layout for systems where the chipset is on the other side of the mother board. D[63:0] => D[0:63] A[35:3] => A[3:35] DINV[3:0]# is also reversed.
LINT[1:0]	I	LINT[1:0] (Local APIC Interrupt) must connect the appropriate pins of all APIC Bus agents. When the APIC is disabled, the LINT0 signal becomes INTR, a maskable interrupt request signal, and LINT1 becomes NMI, a non-maskable interrupt. INTR and NMI are backward compatible with the signals of those names on the Pentium processor. Both signals are asynchronous. Both of these signals must be software configured via BIOS programming of the APIC register space to be used either as NMI/INTR or LINT[1:0]. Because the APIC is enabled by default after Reset, operation of these pins as LINT[1:0] is the default configuration.
LOCK#	I/O	Probe Ready signal used by debug tools to determine processor debug readiness.
PRDY#	O	Probe Request signal used by debug tools to request debug operation of the processor.
PREQ#	I	Probe Request signal used by debug tools to request debug operation of the processor.
PROCHOT#	I/O, O (DP)	As an output, PROCHOT# (Processor Hot) will go active when the processor temperature monitoring sensor detects that the processor has reached its maximum safe operating temperature. This indicates that the processor Thermal Control Circuit (TCC) has been activated, if enabled. As an input, assertion of PROCHOT# by the system will activate the TCC, if enabled. The TCC will remain active until the system de-asserts PROCHOT#. This signal may require voltage translation on the motherboard.

Table 14. Signal Description (Sheet 6 of 7)

Signal Name	Type	Description
PWRGOOD	I	PWRGOOD (Power Good) is a processor input. The processor requires this signal to be a clean indication that the clocks and power supplies are stable and within their specifications. 'Clean' implies that the signal will remain low (capable of sinking leakage current), without glitches, from the time that the power supplies are turned on until they come within specification. The signal must then transition monotonically to a high state. PWRGOOD can be driven inactive at any time, but clocks and power must again be stable before a subsequent rising edge of PWRGOOD. The PWRGOOD signal must be supplied to the processor; it is used to protect internal circuits against voltage sequencing issues. It should be driven high throughout boundary scan operation.
REQ[4:0]#	I/O	REQ[4:0]# (Request Command) must connect the appropriate pins of both FSB agents. They are asserted by the current bus owner to define the currently active transaction type. These signals are source synchronous to ADSTB[0]#.
RESET#	I	Asserting the RESET# signal resets the processor to a known state and invalidates its internal caches without writing back any of their contents. For a power-on Reset, RESET# must stay active for at least two milliseconds after V_{CC} and BCLK have reached their proper specifications. On observing active RESET#, both FSB agents will de-assert their outputs within two clocks. All processor straps must be valid within the specified setup time before RESET# is de-asserted.
RS[2:0]#	I	RS[2:0]# (Response Status) are driven by the response agent (the agent responsible for completion of the current transaction), and must connect the appropriate pins of both FSB agents.
RSVD	Reserved/ No Connect	These pins are Reserved and must be left unconnected on the board. However, it is recommended that routing channels to these pins on the board be kept open for possible future use.
SLP#	I	SLP# (Sleep), when asserted in Stop-Grant state, causes the processor to enter the Sleep state. During Sleep state, the processor stops providing internal clock signals to all units, leaving only the Phase-Locked Loop (PLL) still operating. Processors in this state will not recognize snoops or interrupts. The processor will recognize only assertion of the RESET# signal, de-assertion of SLP#, and removal of the BCLK input while in Sleep state. If SLP# is de-asserted, the processor exits Sleep state and returns to Stop-Grant state, restarting its internal clock signals to the bus and processor core units. If DPSLP# is asserted while in the Sleep state, the processor will exit the Sleep state and transition to the Deep Sleep state. This signal is not used for nettop 2008 platforms and tied to V_{TT}.
SMI#	I	SMI# (System Management Interrupt) is asserted asynchronously by system logic. On accepting a System Management Interrupt, the processor saves the current state and enter System Management Mode (SMM). An SMI Acknowledge transaction is issued, and the processor begins program execution from the SMM handler. If SMI# is asserted during the de-assertion of RESET#, the processor will tri-state its outputs.
STPCLK#	I	STOP-GRANT state is not supported; therefore, this pin is not used.

Table 14. Signal Description (Sheet 7 of 7)

Signal Name	Type	Description
TCK	I	TCK (Test Clock) provides the clock input for the processor Test Bus (also known as the Test Access Port).
TDI	I	TDI (Test Data In) transfers serial test data into the processor. TDI provides the serial input needed for JTAG specification support.
TDO	O	TDO (Test Data Out) transfers serial test data out of the processor. TDO provides the serial output needed for JTAG specification support.
THERMTRIP	O	The processor protects itself from catastrophic overheating by use of an internal thermal sensor. This sensor is set well above the normal operating temperature to ensure that there are no false trips. The processor will stop all execution when junction temperature exceeds approximately 125 °C. This is signalled to the system by the THERMTRIP# (Thermal Trip) pin.
THRMDA	PWR	Thermal Diode - Anode
THRMDC	PWR	Thermal Diode - Cathode
TMS	I	TMS (Test Mode Select) is a JTAG specification support signal used by debug tools.
TRDY#	I	TRDY# (Target Ready) is asserted by the target to indicate that it is ready to receive a write or implicit writeback data transfer. TRDY# must connect the appropriate pins of both FSB agents.
TRST#	I	TRST# (Test Reset) resets the Test Access Port (TAP) logic. TRST# must be driven low during power on Reset.
VCCA	PWR	V_{CCA} provides isolated power for the internal processor core PLLs.
VCCP	PWR	Processor core power supply.
VSS	GND	Processor core ground node.
VTT	PWR	FSB AGTL+ termination voltage with respect to V_{SS}.
VID[6:0]	O	VID[6:0] (Voltage ID) pins are used to support automatic selection of power supply voltages (V_{CC}). However, these pins are not used in the nettop 2008 platform as the VID is fixed at 1.1 V.
VCC_SENSE	O	VCC_SENSE is an isolated low impedance connection to the processor core power (V_{CC}). It can be used to sense or measure voltage near the silicon with little noise.
VSS_SENSE	O	VSS_SENSE is an isolated low impedance connection to processor core V_{SS}. It can be used to sense or measure ground near the silicon with little noise.

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5 Thermal Specifications and Design Considerations

The processor requires a thermal solution to maintain temperatures within operating limits as set forth in Section 5.1. Any attempt to operate the processor outside these operating limits may result in permanent damage to the processor and potentially other components in the system. As processor technology changes, thermal management becomes increasingly crucial when building computer systems. Maintaining the proper thermal environment is key to reliable, long-term system operation.

A complete thermal solution includes both component and system level thermal management features. Component level thermal solutions include active or passive heatsink attached to the exposed processor die. The solution should make firm contact to the die while maintaining processor mechanical specifications (such as pressure). A typical system level thermal solution may consist of a system fan used to evacuate or pull air through the system. For more information on designing a component level thermal solution, refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2). Alternatively, the processor may be in a fan-less system, but would likely still use a multi-component heat spreader. Note that trading of thermal solutions also involves trading performance.

5.1 Thermal Specifications

To allow for the optimal operation and long-term reliability of Intel processor-based systems, the system/processor thermal solution should be designed such that the processor remains within the minimum and maximum case temperature (T_C) specifications at the corresponding thermal design power (TDP) value listed in Table 15. Thermal solutions not designed to provide this level of thermal capability may affect the long-term reliability of the processor and system. For more details on thermal solution design, refer to the appropriate Thermal and Mechanical Design Guidelines (see Section 1.2).

The case temperature is defined at the geometric top center of the processor. Analysis indicates that real applications are unlikely to cause the processor to consume the theoretical maximum power dissipation for sustained time periods. Intel recommends that complete thermal solution designs target the TDP indicated in Table 15, instead of the maximum processor power consumption. The Intel Thermal Monitor feature is designed to help protect the processor in the unlikely event that an application exceeds the TDP recommendation for a sustained period of time. For more details on the usage of this feature, refer to Section Section 5.1.2. In all cases the Intel Thermal Monitor feature must be enabled for the processor to remain within specification.

Table 15. Power Specifications for the Processor

Symbol	Processor Number	Core Frequency and Voltage	Thermal Design Power			Unit	Tc min (°C)	Tc max (°C)	Notes
TDP	230	1.6 GHz & V_{CC}	4.0			W	0	85.2	1, 3, 4
Symbol	**Parameter**		**Min**	**Typ**	**Max**	**Unit**			
P_{AH}	Auto Halt		—	—	1.0	W	—	—	2

NOTES:
1. The TDP specification should be used to design the processor thermal solution. The TDP is not the maximum theoretical power the processor can generate.
2. Not 100% tested. These power specifications are determined by characterization of the processor currents at higher temperatures and extrapolating the values for the temperature indicated.
3. The Intel Thermal Monitor automatic mode must be enabled for the processor to operate within specifications.
4. V_{CC} is determined by processor VID[6:0].

The processor incorporates three methods of monitoring die temperature: the Digital Thermal Sensor, Intel Thermal Monitor, and the Thermal Diode. The Intel Thermal Monitor (detailed in Section Section 5.1.2) must be used to determine when the maximum specified processor junction temperature has been reached.

5.1.1 Thermal Diode

The processor incorporates an on-die PNP transistor whose base emitter junction is used as a thermal “diode”, with its collector shorted to ground. The thermal diode can be read by an off-die analog/digital converter (a thermal sensor) located on the motherboard or a stand-alone measurement kit. The thermal diode may be used to monitor the die temperature of the processor for thermal management or instrumentation purposes but is not a reliable indication that the maximum operating temperature of the processor has been reached. When using the thermal diode, a temperature offset value must be read from a processor MSR and applied. See Section 5.1.2 for more details. See Section Section 5.1.2 for thermal diode usage recommendation when the PROCHOT# signal is not asserted.

The reading of the external thermal sensor (on the motherboard) connected to the processor thermal diode signals will not necessarily reflect the temperature of the hottest location on the die. This is due to inaccuracies in the external thermal sensor, on-die temperature gradients between the location of the thermal diode and the hottest location on the die, and time-based variations in the die temperature measurement. Time-based variations can occur when the sampling rate of the thermal diode (by the thermal sensor) is slower than the rate at which the T_J temperature can change.

Offset between the thermal diode based temperature reading and the Intel Thermal Monitor reading may be characterized using the Intel Thermal Monitor’s Automatic mode activation of the thermal control circuit. This temperature offset must be taken into account when using the processor thermal diode to implement power management events. This offset is different than the diode T_{offset} value programmed into the processor Model Specific Register (MSR).

Table 16 and Table 17 provide the diode interface and specifications. Transistor model parameters shown in Table 17 providing more accurate temperature measurements when the diode ideality factor is closer to the maximum or minimum limits. Contact

your external sensor supplier for their recommendation. The thermal diode is separate from the Thermal Monitor's thermal sensor and cannot be used to predict the behavior of the Thermal Monitor.

Table 16. Thermal Diode Interface

Signal Name	Pin/Ball Number	Signal Description
THERMDA	E4	Thermal diode anode
THERMDC	E5	Thermal diode cathode

Table 17. Thermal Diode Parameters using Transistor Model

Symbol	Parameter	Min	Typ	Max	Unit	Notes
IFW	Forward Bias Current	5	—	200	μA	1
IE	Emitter Current	5	—	200	μA	1
nQ	Transistor Ideality	0.997	1.001	1.015		2,3,4
Beta		0.25	—	0.65		2,3
RT	Series Resistance	2.79	4.52	6.24	Ω	2,5

NOTES:

1. Intel does not support or recommend operation of the thermal diode under reverse bias.
2. Characterized across a temperature range of 50–100 °C.
3. Not 100% tested. Specified by design characterization.
4. The ideality factor, nQ, represents the deviation from ideal transistor model behavior as exemplified by the equation for the collector current:

$$I_C = I_S * (e^{qV_{BE}/n_Q kT} - 1)$$

   where I_S = saturation current, q = electronic charge, V_{BE} = voltage across the transistor base emitter junction (same nodes as VD), k = Boltzmann Constant, and T = absolute temperature (Kelvin).

5. The series resistance, R_T, provided in the Diode Model Table (Table 17) can be used for more accurate readings as needed.

When calculating a temperature based on the thermal diode measurements, a number of parameters must be either measured or assumed. Most devices measure the diode ideality and assume a series resistance and ideality trim value, although are capable of also measuring the series resistance. Calculating the temperature is then accomplished using the equations listed under Table 17. In most sensing devices, an expected value for the diode ideality is designed-in to the temperature calculation equation. If the designer of the temperature sensing device assumes a perfect diode, the ideality value (also called n_{trim}) will be 1.000. Given that most diodes are not perfect, the designers usually select an n_{trim} value that more closely matches the behavior of the diodes in the processor. If the processor diode ideality deviates from that of the n_{trim}, each calculated temperature will be offset by a fixed amount. This temperature offset can be calculated with the equation:

$$T_{error(nf)} = T_{measured} * (1 - n_{actual}/n_{trim})$$

where $T_{error(nf)}$ is the offset in degrees C, $T_{measured}$ is in Kelvin, n_{actual} is the measured ideality of the diode, and n_{trim} is the diode ideality assumed by the temperature sensing device.

5.1.2 Intel® Thermal Monitor

The Intel Thermal Monitor helps control the processor temperature by activating the TCC (Thermal Control Circuit) when the processor silicon reaches its maximum operating temperature. The temperature at which the Intel Thermal Monitor activates the TCC is not user configurable. Bus traffic is snooped in the normal manner and interrupt requests are latched (and serviced during the time that the clocks are on) while the TCC is active.

With a properly designed and characterized thermal solution, it is anticipated that the TCC would only be activated for very short periods of time when running the most power intensive applications. The processor performance impact due to these brief periods of TCC activation is expected to be minor and hence not detectable. An under-designed thermal solution that is not able to prevent excessive activation of the TCC in the anticipated ambient environment may cause a noticeable performance loss and may affect the long-term reliability of the processor. In addition, a thermal solution that is significantly under designed may not be capable of cooling the processor even when the TCC is active continuously.

The Intel Thermal Monitor controls the processor temperature by modulating (starting and stopping) the processor core clocks when the processor silicon reaches its maximum operating temperature. The Intel Thermal Monitor uses two modes to activate the TCC: automatic mode and on-demand mode. If both modes are activated, automatic mode takes precedence.

There is only one automatic modes called Intel Thermal Monitor 1 (TM1). This mode is selected by writing values to the MSRs of the processor. After automatic mode is enabled, the TCC will activate only when the internal die temperature reaches the maximum allowed value for operation.

The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 be enabled on the processor.

When TM1 is enabled and a high temperature situation exists, the clocks will be modulated by alternately turning the clocks off and on at a 50% duty cycle. Cycle times are processor speed dependent and will decrease linearly as processor core frequencies increase. Once the temperature has returned to a non-critical level, modulation ceases and TCC goes inactive. A small amount of hysteresis has been included to prevent rapid active/inactive transitions of the TCC when the processor temperature is near the trip point. The duty cycle is factory configured and cannot be modified. Also, automatic mode does not require any additional hardware, software drivers, or interrupt handling routines. Processor performance will be decreased by the same amount as the duty cycle when the TCC is active.

Note: **The Intel Thermal Monitor automatic mode must be enabled through BIOS for the processor to be operating within specifications. Intel recommends TM1 be enabled on the processors.**

Note: **TM1 feature is referred to as Adaptive Thermal Monitoring features.**

The TCC may also be activated via on-demand mode. If bit 4 of the ACPI Intel Thermal Monitor control register is written to a 1, the TCC will be activated immediately independent of the processor temperature. When using on-demand mode to activate the TCC, the duty cycle of the clock modulation is programmable via bits 3:1 of the same ACPI Intel Thermal Monitor control register. In automatic mode, the duty cycle is fixed at 50% on, 50% off, however in on-demand mode, the duty cycle can be programmed from 12.5% on/ 87.5% off, to 87.5% on/12.5% off in 12.5% increments. On-demand mode may be used at the same time automatic mode is enabled; however,

if the system tries to enable the TCC via on-demand mode at the same time automatic mode is enabled and a high temperature condition exists, automatic mode will take precedence.

An external signal, PROCHOT# (processor hot) is asserted when the processor detects that its temperature is above the thermal trip point. Bus snooping and interrupt latching are also active while the TCC is active.

Besides the thermal sensor and thermal control circuit, the Intel Thermal Monitor also includes one ACPI register, one performance counter register, three MSR, and one I/O pin (PROCHOT#). All are available to monitor and control the state of the Intel Thermal Monitor feature. The Intel Thermal Monitor can be configured to generate an interrupt upon the assertion or deassertion of PROCHOT#.

PROCHOT# will not be asserted when the processor is in the Stop Grant power states; hence, the thermal diode reading must be used as a safeguard to maintain the processor junction temperature within maximum specification. If the platform thermal solution is not able to maintain the processor junction temperature within the maximum specification, the system must initiate an orderly shutdown to prevent damage. If the processor enters one of the above power states with PROCHOT# already asserted, PROCHOT# will remain asserted until the processor exits the Stop Grant power state and the processor junction temperature drops below the thermal trip point.

If Intel Thermal Monitor automatic mode is disabled, the processor will be operating out of specification. Regardless of enabling the automatic or on-demand modes, in the event of a catastrophic cooling failure, the processor will automatically shut down when the silicon has reached a temperature of approximately 125 °C. At this point the THERMTRIP# signal will go active. THERMTRIP# activation is independent of processor activity and does not generate any bus cycles. When THERMTRIP# is asserted, the processor core voltage must be shut down within the time specified in Chapter 3.

5.1.3 Digital Thermal Sensor

The processor also contains an on-die Digital Thermal Sensor (DTS) that can be read via an MSR (no I/O interface). The processor has a unique digital thermal sensor whose temperature is accessible via the processor MSRs. The DTS is the preferred method of reading the processor die temperature since it can be located much closer to the hottest portions of the die and can thus more accurately track the die temperature and potential activation of processor core clock modulation via the Thermal Monitor. The DTS is only valid while the processor is in the normal operating state (the Normal package level low power state).

Unlike traditional thermal devices, the DTS will output a temperature relative to the maximum supported operating temperature of the processor (T_{J_max}). It is the responsibility of software to convert the relative temperature to an absolute temperature. The temperature returned by the DTS will always be at or below T_{J_max}. Catastrophic temperature conditions are detectable via an Out Of Spec status bit. This bit is also part of the DTS MSR. When this bit is set, the processor is operating out of specification and immediate shutdown of the system should occur. The processor operation and code execution is not ensured once the activation of the Out of Spec status bit is set.

The DTS-relative temperature readout corresponds to the Thermal Monitor (TM1) trigger point. When the DTS indicates maximum processor core temperature has been reached, the TM1 hardware thermal control mechanism will activate. The DTS and TM1 temperature may not correspond to the thermal diode reading since the thermal diode is located in a separate portion of the die and thermal gradient between the individual core DTS. Additionally, the thermal gradient from DTS to thermal diode can vary substantially due to changes in processor power, mechanical and thermal attach, and software application. The system designer is required to use the DTS to ensure proper operation of the processor within its temperature operating specifications.

Changes to the temperature can be detected via two programmable thresholds located in the processor MSRs. These thresholds have the capability of generating interrupts via the core's local APIC. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

5.1.4 Out of Specification Detection

Overheat detection is performed by monitoring the processor temperature and temperature gradient. This feature is intended for graceful shut down before the THERMTRIP# is activated. If the processor's TM1 are triggered and the temperature remains high, an "Out Of Spec" status and sticky bit are latched in the status MSR register and generates thermal interrupt.

5.1.5 PROCHOT# Signal Pin

An external signal, PROCHOT# (processor hot), is asserted when the processor die temperature has reached its maximum operating temperature. If TM1 is enabled, then the TCC will be active when PROCHOT# is asserted. The processor can be configured to generate an interrupt upon the assertion or de-assertion of PROCHOT#. Refer to the *Intel® 64 and IA-32 Architectures Software Developer's Manuals* for specific register and programming details.

The processor implements a bi-directional PROCHOT# capability to allow system designs to protect various components from overheating situations. The PROCHOT# signal is bi-directional in that it can either signal when the processor has reached its maximum operating temperature or be driven from an external source to activate the TCC. The ability to activate the TCC via PROCHOT# can provide a means for thermal protection of system components.

Only a single PROCHOT# pin exists at a package level of the processor. When the core's thermal sensor trips, PROCHOT# signal will be driven by the processor package. If TM1 is enabled, PROCHOT# will be asserted. It is important to note that Intel recommends TM1 to be enabled.

When PROCHOT# is driven by an external agent, if TM1 is enabled on the core, then the processor core will have the clocks modulated.

PROCHOT# may be used for thermal protection of voltage regulators (VR). System designers can create a circuit to monitor the VR temperature and activate the TCC when the temperature limit of the VR is reached. By asserting PROCHOT# (pulled-low) and activating the TCC, the VR will cool down as a result of reduced processor power consumption. Bi-directional PROCHOT# can allow VR thermal designs to target maximum sustained current instead of maximum current. Systems should still provide proper cooling for the VR and rely on bi-directional PROCHOT# only as a backup in case of system cooling failure. The system thermal design should allow the power delivery circuitry to operate within its temperature specification even while the processor is operating at its TDP. With a properly designed and characterized thermal solution, it is anticipated that bi-directional PROCHOT# would only be asserted for very short periods of time when running the most power intensive applications. An under-designed thermal solution that is not able to prevent excessive assertion of PROCHOT# in the anticipated ambient environment may cause a noticeable performance loss.

Refer to the *Voltage Regulation Specification* for details on implementing the bi-directional PROCHOT# feature.

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6 Debug Tools Specifications

The ITP-XDP debug port connector is the recommended debug port for platforms using the Intel® Atom™ processor. Contact your Intel representative for more information.