MOTOROLA

MC3232A

Advance Information

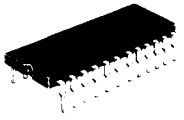
MEMORY ADDRESS MULTIPLEXER AND REFRESH ADDRESS COUNTER

SCHOTTKY
SILICON MONOLITHIC
INTEGRATED CIRCUITS

MEMORY ADDRESS MULTIPLEXER

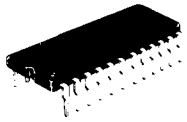
The Motorola MC3232A is an address multiplexer and refresh counter for 16-pin 4K dynamic RAMs that require a 64-cycle refresh. It multiplexes twelve system address bits to the six input address pins of the memory device. The MC3232A also contains a 6-bit refresh counter that is clocked externally to generate the 64 sequential addresses required for refresh. The high performance of the MC3232A will enhance the high speed of the fast N-channel RAMs such as the MCM4027.

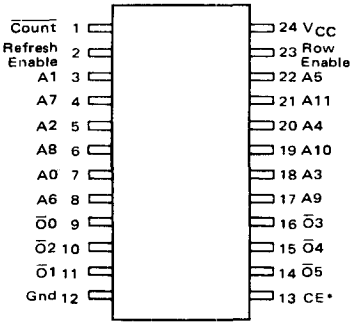
- Simplifies 16-Pin 4K Dynamic Memory Design
- Reduces Package Count
- 6-Bit Binary Counter for 64 Refresh Address
- Multiplexing: Row Address/Column Address/Refresh Address
- High Input Impedance for Minimum Loading of Bus:
  I_F = 0.25 mA Max
- Schottky TTL for High Performance Address
  Input to Output Delay
  t_{AO} = 25 ns @ C_L = 250 pF, 9.0 ns Max @ C_L = 15 pF
- Second Source to Intel 3232
  (Detect Zero Function Not Included and Additional Power Fail Feature Added at Pin 13)



L SUFFIX
CERAMIC PACKAGE
CASE 623

P SUFFIX
PLASTIC PACKAGE
CASE 649





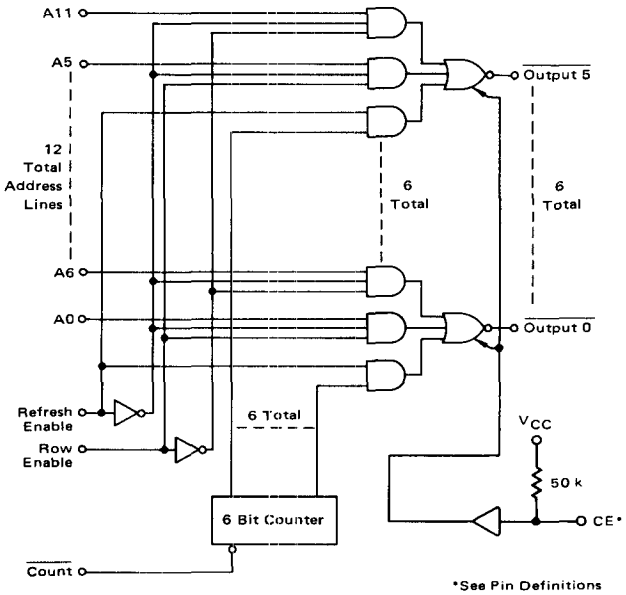
Note: A0 Through A5 Are Row Addresses
A6 Through A11 Are Column Addresses
*See Pin Definitions

TRUTH TABLE AND DEFINITIONS

Refresh Enable	Row Enable	Output
H	X	Refresh Address (From Internal Counter)
L	H	Row Address (A0 through A5)
L	L	Column Address (A6 through A11)

Count — Advances Internal Refresh Counter

LOGIC DIAGRAM



*See Pin Definitions

ORDERING INFORMATION		
Device	Temperature Range	Package
MC3232AL	0 to 75°C	Ceramic DIP
MC3232AP	0 to 75°C	Plastic DIP

This is advance information and specifications are subject to change without notice.

ADI-518

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ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Rating	Symbol	Value	Unit
Power Supply Voltage	V_{CC}	-0.5 to +7.0	V
Input Voltage	V_I	-0.5 to +7.0	V
Output Voltage	V_O	-0.5 to +7.0	V
Output Current	I_O	100	mA
Operating Ambient Temperature	T_A	0 to +75	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Junction Temperature Ceramic Package Plastic Package	T_J	 +175 +150	°C

"Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum ratings for extended periods may affect reliability.

ELECTRICAL CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C; typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Input Current, Low Logic State (V_{IL} = 0.45 V)	I_{IL}	–	-0.04	-0.25	mA
Input Current, High Logic State (V_{IH} = 5.5 V)	I_{IH}	–	–	10	μA
Input Voltage, Low Logic State	V_{IL}	–	–	0.8	V
Input Voltage, High Logic State	V_{IH}	2.0	–	–	V
Output Voltage, Low Logic State (I_{OL} = 5.0 mA)	V_{OL}	–	0.25	0.4	V
Output Voltage, High Logic State (I_{OH} = -1.0 mA)	V_{OH}	2.8	4.0	–	V
Input Clamp Voltage (I_{IC} = -12 mA)	V_{IC}	–	-0.8	-1.5	V
Power Supply Current (V_{CC} = 5.5 V)	I_{CC}	–	58	90	mA

SWITCHING CHARACTERISTICS (Unless otherwise noted, Min/Max values apply with 4.5 V ≤ V_{CC} ≤ 5.5 V, 0°C ≤ T_A ≤ 75°C; typical values apply with V_{CC} = 5.0 V, T_A = 25°C.)

Characteristic	Symbol	Min	Typ	Max	Unit
Propagation Delay Times Address Input to Output (Load = 1 TTL, C_L = 250 pF) (Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)	t_{AO}	 – –	 12 6.0	 25 9.0	ns
Row Enable to Output (Load = 1 TTL, C_L = 250 pF) (Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)	t_{OO}	 – –	 32 18	 41 27	ns
Refresh Enable to Output (Load = 1 TTL, C_L = 250 pF) (Load = 1 TTL, C_L = 15 pF, V_{CC} = 5.0 V, T_A = 25°C)	t_{EO}	 – –	 32 18	 45 27	ns
$\overline{Count}$ Pulse Width	$t_{W\overline{C}}$	30	–	–	ns
Counting Frequency	$f_{\overline{C}}$	5.0	10	–	MHz

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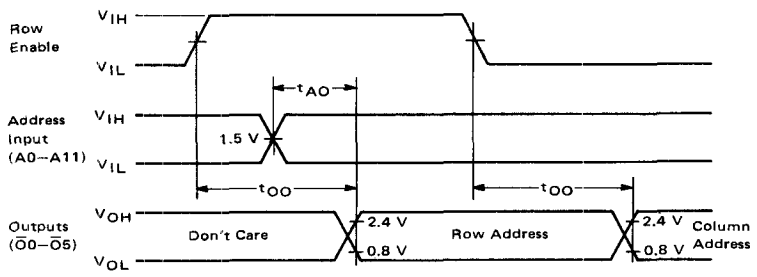
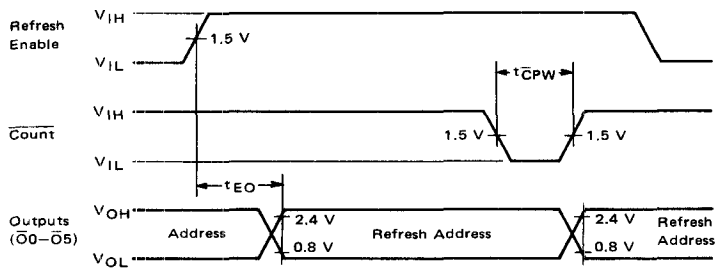
FIGURE 1 – AC WAVEFORMS with MCM6604 NORMAL CYCLE



Refresh Enable – Low Logic State

FIGURE 2 – REFRESH CYCLE



TYPICAL CHARACTERISTICS

FIGURE 3 – OUTPUT CURRENT versus OUTPUT LOW VOLTAGE

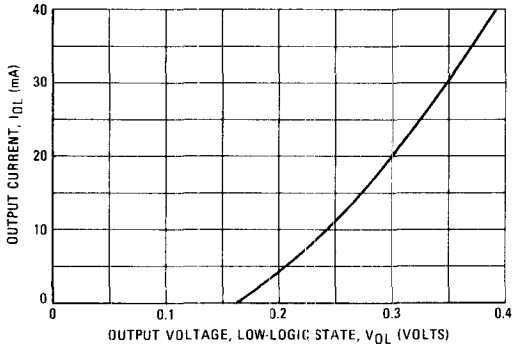
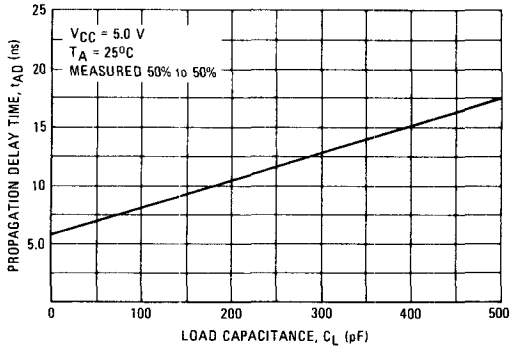


FIGURE 4 – PROPAGATION DELAY versus LOAD CAPACITANCE
Row or Column Address to Output



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PIN DEFINITIONS

$\overline{\text{Count}}$ Input – Pin 1
Active low input increments internal 6-bit counter by one for each count pulse in.

Refresh Enable Input – Pin 2
Active high input which determines whether the MC3232A is in refresh mode (H) or address enable (L).

A0–A5 Inputs – Pins 7, 3, 5, 18, 20, 22
Row address inputs.

A6–A11 Inputs – Pins 8, 4, 6, 17, 19, 21
Column address inputs.

$\overline{O}0$–$\overline{O}5$ Outputs – Pins 9, 11, 10, 16, 15, 14
Address outputs to memories. Inverted with respect to address inputs.

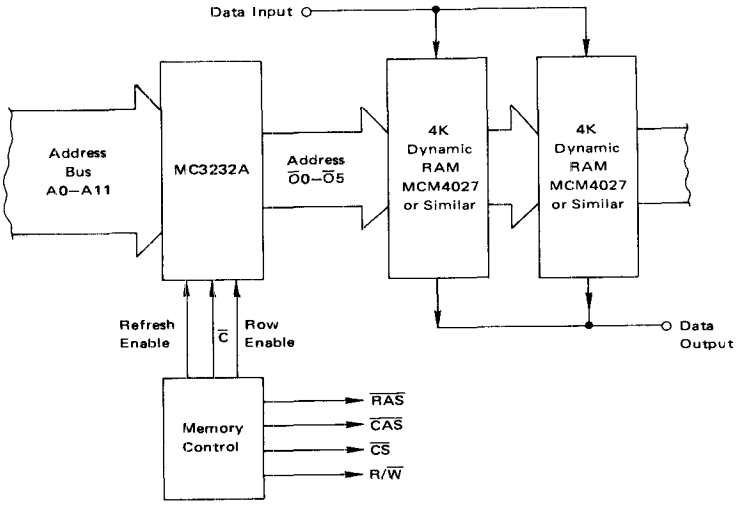
Gnd – Pin 12
Power supply ground.

CE Input – Pin 13
Optional use, chip enable control pin. Left open, an internal 50 kΩ pullup resistor keeps this pin high and the MC3242A is a functional replacement for the Intel 3242 (without detect zero function). As an active input, when pulled low, all 3242A outputs go three-state. Regardless of Pin 13 (CE) condition, when power (V_{CC}) is removed, all 3242A outputs go three-state. In addition, the refresh address counter is reset to all 1s so that upon return of supply power, control of refresh addressing can be returned to the MC3242A (by pulling Pin 13 high) at a known address (i.e., all 1s). This option is available tested by consulting factory.

Row Enable Input – Pin 23
High input selects row, low input selects column addresses of the driven memories.

V_{CC} – Pin 24
+5 V power supply input. Due to high capacitance drive capability, a 0.1 μF capacitor should be used to ground along with careful V_{CC} and Gnd Bus layout.

GENERAL 4K DYNAMIC RAM
SIMPLIFIED BLOCK DIAGRAM



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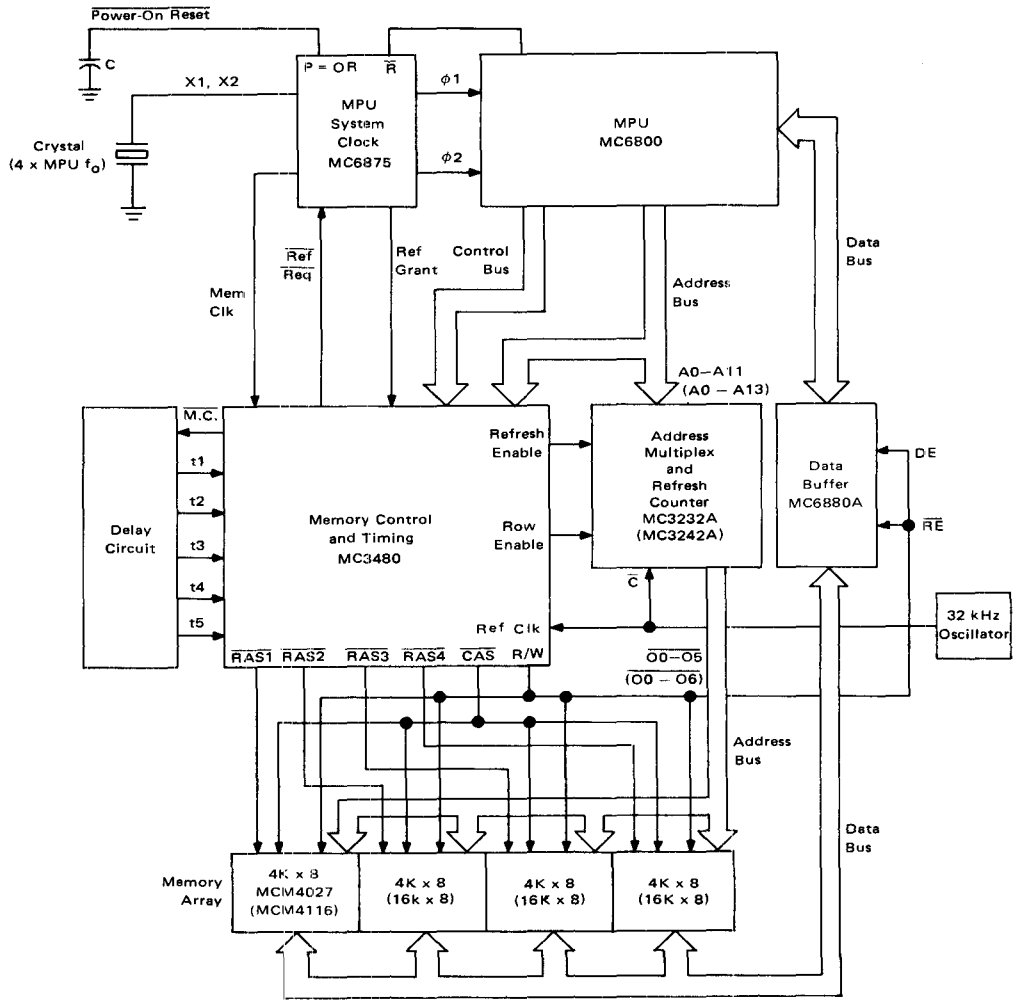
TYPICAL APPLICATION
16K X 8-BIT MEMORY SYSTEM FOR M6800 MPU

Note: Numbers in parenthesis indicate part types or values for 16K x 1 RAMs



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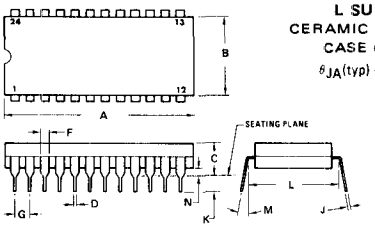
OUTLINE DIMENSIONS

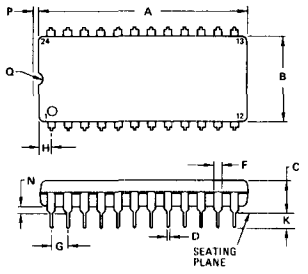
L SUFFIX
CERAMIC PACKAGE
CASE 623-02
θ_{JA}(typ) = 53°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.24	32.26	1.230	1.270
B	12.70	13.72	0.500	0.540
C	4.06	5.59	0.160	0.220
D	0.41	0.51	0.016	0.020
F	1.27	1.52	0.050	0.060
G	2.54 BSC		0.100 BSC	
J	0.20	0.30	0.008	0.012
K	3.18	4.06	0.125	0.160
L	15.24 BSC		0.600 BSC	
M	5°	15°	5°	15°
N	0.51	1.27	0.020	0.050

NOTES:
1. DIM "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.
2. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION. (WHEN FORMED PARALLEL)

P SUFFIX
PLASTIC PACKAGE
CASE 649-03
θ_{JA}(typ) = 90°C/W



DIM	MILLIMETERS MIN	MILLIMETERS MAX	INCHES MIN	INCHES MAX
A	31.50	32.13	1.240	1.265
B	13.21	13.72	0.520	0.540
C	4.70	5.21	0.185	0.205
D	0.38	0.51	0.015	0.020
F	1.02	1.52	0.040	0.060
G	2.54 BSC		0.100 BSC	
H	1.65	2.16	0.065	0.085
J	0.20	0.30	0.008	0.012
K	2.92	3.43	0.115	0.135
L	14.99	15.49	0.590	0.610
M	–	10°	–	10°
N	0.51	1.02	0.020	0.040
P	0.13	0.38	0.005	0.015
Q	0.51	0.76	0.020	0.030

NOTES:
1. LEADS WITHIN 0.13 mm (0.005) RADIUS OF TRUE POSITION AT SEATING PLANE AT MAXIMUM MATERIAL CONDITION.
2. DIMENSION "L" TO CENTER OF LEADS WHEN FORMED PARALLEL.

THERMAL INFORMATION

The maximum power consumption an integrated circuit can tolerate at a given operating ambient temperature, can be found from the equation:

$$P_{D(T_A)} = \frac{T_{J(max)} - T_A}{R_{\theta JA(Typ)}}$$

Where: $P_{D(T_A)}$ = Power Dissipation allowable at a given operating ambient temperature. This must be greater than the sum of the products of the supply voltages and supply currents at the worst case operating condition.

$T_{J(max)}$ = Maximum Operating Junction Temperature as listed in the Maximum Ratings Section

T_A = Maximum Desired Operating Ambient Temperature

$R_{\theta JA(Typ)}$ = Typical Thermal Resistance Junction to Ambient

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11886 PRINTED IN USA 8-78 IMPERIAL LITHO 873367 100
ADI 518