



## P-Channel Enhancement-Mode Vertical DMOS FET

### Features

- ☐ Low threshold, -2.4V max.
- ☐ High input impedance
- ☐ Low input capacitance, 110pFmax.
- ☐ Fast switching speeds
- ☐ Low on resistance
- ☐ Free from secondary breakdown
- ☐ Low input and output leakage
- ☐ Complementary N- and P-channel devices

### Application

- ☐ Logic level interfaces-ideal for TTL and CMOS
- ☐ Battery operated systems
- ☐ Photo voltaic devices
- ☐ Analog switches
- ☐ General purpose line drivers
- ☐ Telecom switches

### Absolute Maximum Ratings

Drain-to-Source Voltage	$BV_{DSS}$
Drain-to-Gate Voltage	$BV_{DGS}$
Gate-to-Source Voltage	$\pm 20V$
Operating and Storage Temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering Temperature****	$300^{\circ}C$

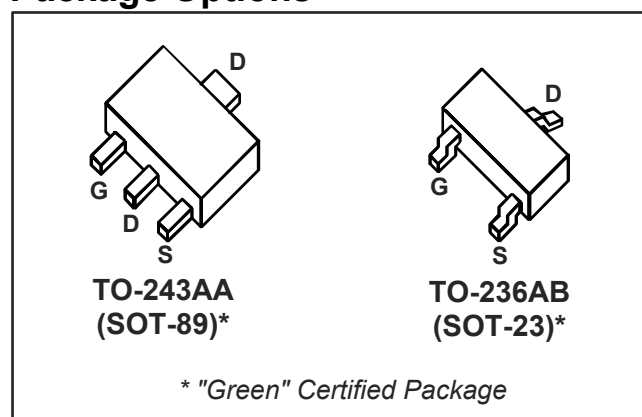
\*\*\*\*Distance of 1.6mm from case for 10 seconds.

### General Description

These low threshold enhancement-mode (normally-off) transistors utilize an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces devices with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, these devices are free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Package Options



### Ordering Information

Order Number / Package		$BV_{DSS} / BV_{DGS}$	$R_{DS(ON)}$ (max)	$V_{GS(th)}$ (max)	$I_{D(ON)}$ (min)
TO-243AA**	TO-236AB***				
TP5322N8	TP5322K1	-220V	$12\Omega$	-2.4V	-0.7A
TP5322N8-G*	TP5322K1-G*	-220V	$12\Omega$	-2.4V	-0.7A

\*\*Same as SOT-89. Product supplied on 2000 piece carrier tape reels.

\*\*\*Same as SOT-23. Products supplied on 3000 piece carrier tape reels.

Product Marking for SOT-89

TP3C\*

Where \*=2-week alpha date code

Product Marking for SOT-23

P3C\*

Where \*=2-week alpha date code



## Thermal Characteristics

Package	I <sub>D</sub> (continuous)	I <sub>D</sub> (pulsed)	Power Dissipation @ T <sub>A</sub> = 25°C	θ <sub>JC</sub> °C/W	θ <sub>JA</sub> °C/W	I <sub>DR</sub> *	I <sub>DRM</sub>
TO-243AA	-0.26A	-0.90A	1.6W	15	78**	-0.26A	-0.9A
TO-236AB	-0.12A	-0.70A	0.36W	200	350	-0.12A	-0.7A

\*I<sub>D</sub>(continuous) is limited by max rated T<sub>J</sub>.

\*\*Mounted on FR4 board, 25mm x 25mm x 1.57mm. Significant PD increase possible on ceramic substate.

## Electrical Characteristics (@25°C unless otherwise specified)

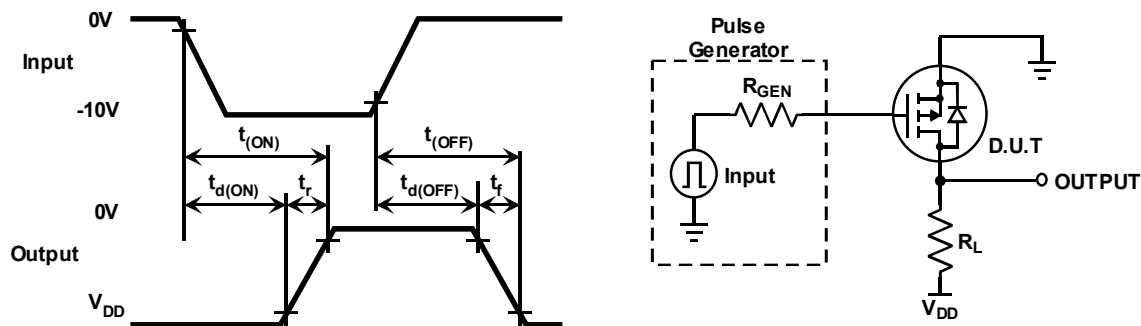
Symbol	Parameter	Min	Typ	Max	Units	Conditions
BV <sub>DSS</sub>	Drain-to-Source Breakdown Voltage	-220			V	V <sub>GS</sub> = 0V, I <sub>D</sub> = -2mA
V <sub>GS(th)</sub>	Gate Threshold Voltage	-1.0		-2.4	V	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1mA
ΔV <sub>GS(th)</sub>	Change in V <sub>GS(th)</sub> with Temperature			4.5	mV/°C	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = -1mA
I <sub>GSS</sub>	Gate Body Leakage			-100	nA	V <sub>GS</sub> = ±20V, V <sub>DS</sub> = 0V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current			-10	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = Max Rating
				-1.0	mA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0.8 Max Rating, T <sub>A</sub> = 125°C
I <sub>D(ON)</sub>	On-State Drain Current	-0.7	-0.95		A	V <sub>GS</sub> = -10V, V <sub>DS</sub> = -25V
R <sub>DS(ON)</sub>	Static Drain-to-Source ON-State Resistance		10	15	Ω	V <sub>GS</sub> = -4.5V, I <sub>D</sub> = -100mA
			8.0	12		V <sub>GS</sub> = -10V, I <sub>D</sub> = -200mA
ΔR <sub>DS(ON)</sub>	Change in R <sub>DS(ON)</sub> with Temperature			1.7	%/°C	V <sub>GS</sub> = -10V, I <sub>D</sub> = -200mA
G <sub>FS</sub>	Forward Transconductance	100	250		mmho	V <sub>DS</sub> = -25V, I <sub>D</sub> = -200mA
C <sub>ISS</sub>	Input Capacitance			110	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = -25V f = 1MHz
C <sub>OSS</sub>	Common Source Output Capacitance			45		
C <sub>RSS</sub>	Reverse Transfer Capacitance			20		
t <sub>d(ON)</sub>	Turn-ON Delay Time			10	ns	V <sub>DD</sub> = -25V, I <sub>D</sub> = -0.7A R <sub>GEN</sub> = 25 Ω
t <sub>r</sub>	Rise Time			15		
t <sub>d(OFF)</sub>	Turn-Off Delay Time			20		
t <sub>f</sub>	Fall Time			15		
V <sub>SD</sub>	Diode Forward Voltage Drop			-1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -0.5A
t <sub>rr</sub>	Reverse Recovery Time		300		ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = -0.5A

Notes:

1) All DC parameters 100% tested at 25°C unless otherwise stated. (Pulsed test: 300μs pulse at 2% duty cycle.)

2) All AC parameters sample tested.

## Switching Waveforms and Test Circuit



Supertex Inc. does not recommend the use of its products in life support applications and will not knowingly sell its products for use in such applications unless it receives an adequate "products liability indemnification insurance agreement." Supertex does not assume responsibility for use of devices described and limits its liability to the replacement of devices determined to be defective due to workmanship. No responsibility is assumed for possible omissions or inaccuracies. Circuitry and specifications are subject to change without notice. For the latest product specifications, refer to the Supertex website: <http://www.supertex.com>. For complete liability information on all Supertex products, refer to the most current databook or to the Legal/Disclaimer page on the Supertex website.