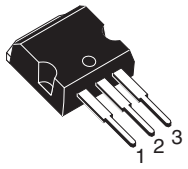
STB12NK80Z-S

N-channel 800V - 0.65Ω - 10.5A I^2SPAK Zener-protected superMESH™ Power MOSFET

General features

Type	V_{DSS}	$R_{DS(on)}$	I_D	Pw
STB12NK80Z-S	800V	<0.75Ω	10.5A	190W

- Extremely high dv/dt capability
- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitances

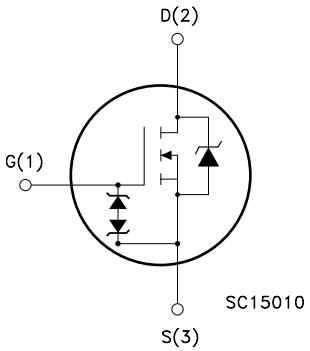


I^2SPAK

Description

The SuperMESH™ series is obtained through an extreme optimization of ST's well established strip-based PowerMESH™ layout. In addition to pushing on-resistance significantly down, special care is taken to ensure a very good dv/dt capability for the most demanding applications. Such series complements ST full range of high voltage MOSFETs including revolutionary MDmesh™ products.

Internal schematic diagram



Applications

- Switching application

Order codes

Sales type	Marking	Package	Packaging
STB12NK80Z-S	B12NK80Z-S	I^2SPAK	Tube

Contents

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage (V_{GS} = 0)	800	V
V_{DGR}	Drain-gate voltage (R_{GS} = 20 kΩ)	800	V
V_{GS}	Gate- source voltage	± 30	V
I_D	Drain current (continuous) at T_C = 25°C	10.5	A
I_D	Drain current (continuous) at T_C = 100°C	6.6	A
I_{DM} (1)	Drain current (pulsed)	42	A
P_{tot}	Total dissipation at T_C = 25°C	190	W
	Derating Factor	1.51	W/°C
$V_{ESD(G-S)}$	Gate source ESD(HBM-C=100pF, R=1.5KΩ)	6000	V
dv/dt (2)	Peak diode recovery voltage slope	4.5	V/ns
T_{stg}	Storage temperature	--55 to 150	°C
T_j	Max. operating junction temperature		

1. Pulse width limited by safe operating area.
2. $I_{SD} \leq 10.5A$, di/dt ≤200A/µs, $V_{DD} \leq V_{(BR)DSS}$, Tj ≤T_{JMAX}

Table 2. Thermal data

Rthj-case	Thermal resistance junction-case max	0.66	°C/W
Rthj-amb	Thermal resistance junction-ambient max	62.5	°C/W
T_J	Maximum lead temperature for soldering purpose	300	°C

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AS}	Avalanche current, repetitive or not-repetitive (pulse width limited by Tj Max)	10.5	A
E_{AS}	Single pulse avalanche energy (starting Tj=25°C, Id=Iar, Vdd=50V)	400	mJ

Table 4. Gate-source zener diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
BV_{GSO} (1)	Gate-Source Breakdown Voltage	Igs=±1mA (Open Drain)	30			V

1. The built-in back-to-back Zener diodes have specifically been designed to enhance not only the device's ESD capability, but also to make them safely absorb possible voltage transients that may occasionally be applied from gate to source. In this respect the Zener voltage is appropriate to achieve an efficient and cost-effective intervention to protect the device's integrity. These integrated Zener diodes thus avoid the usage of external components.

2 Electrical characteristics

(T_{CASE}=25°C unless otherwise specified)

Table 5. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	I_D = 1mA, V_{GS} =0	800			V
I_{DSS}	Zero gate voltage drain current (V_{GS} = 0)	V_{DS} = max ratings V_{DS} = max ratings, T_C = 125°C			1 50	µA µA
I_{GSS}	Gate-body leakage current (V_{DS} = 0)	V_{GS} = ± 20V			±10	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 100µA	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	V_{GS} = 10V, I_D = 5.25A		0.65	0.75	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g_{fs} (1)	Forward transconductance	V_{DS} =15V, I_D = 5.25A		12		S
C_{iss} C_{oss} C_{rss}	Input capacitance Output capacitance Reverse transfer capacitance	V_{DS} =25V, f=1 MHz, V_{GS}=0		2620 250 53		pF pF pF
$C_{oss\ eq}$ (2).	Equivalent output capacitance	V_{GS}=0, V_{DS} =0V to 640V		100		pF
Q_g Q_{gs} Q_{gd}	Total gate charge Gate-source charge Gate-drain charge	V_{DD}=640V, I_D = 10.5A V_{GS} =10V		87 14 44		nC nC nC

1. Pulsed: pulse duration=300µs, duty cycle 1.5%
2. $C_{oss\ eq.}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} inceases from 0 to 80% V_{DSS}

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ t_r	Turn-on Delay Time Rise Time	V_{DD}=400 V, I_D=5.25A, R_G=4.7Ω, V_{GS}=10V (see *Figure 14*)		30 18		ns ns
$t_{d(off)}$ t_f	Turn-off Delay Time Fall Time	V_{DD}=400 V, I_D=5.25A, R_G=4.7Ω, V_{GS}=10V (See *Figure 14*)		70 20		ns ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD} I_{SDM} (1)	Source-drain current Source-drain current (pulsed)				10.5 42	A A
V_{SD} (2)	Forward on voltage	I_{SD} = 10.5A, V_{GS} = 0			1.6	V
t_{rr} Q_{rr} I_{RRM}	Reverse recovery time Reverse recovery charge Reverse recovery current	I_{SD} = 10.5A, di/dt = 100A/µs, V_{DD} = 100V, T_j = 150°C (see *Figure 16*)		635 5.9 18.5		ns nC A

1. Pulse width limited by safe operating area.
2. Pulsed: Pulse duration = 300 µs, duty cycle 1.5 %

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

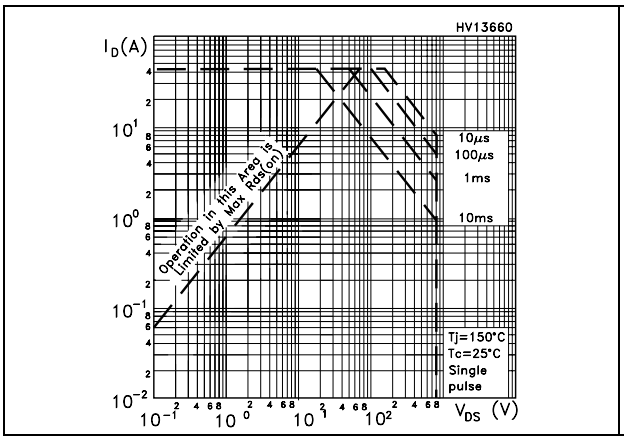


Figure 2. Thermal impedance

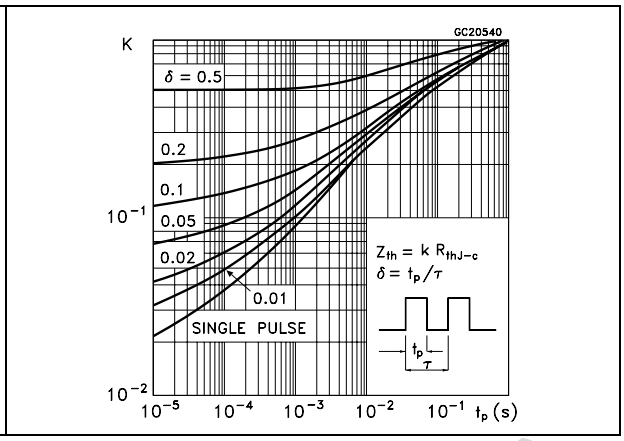


Figure 3. Output characterisics

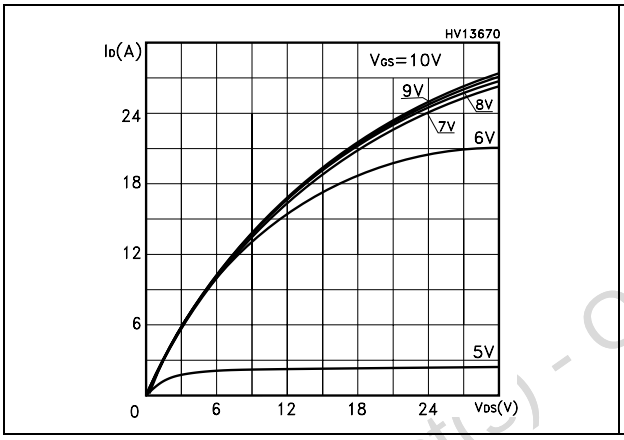


Figure 4. Transfer characteristics

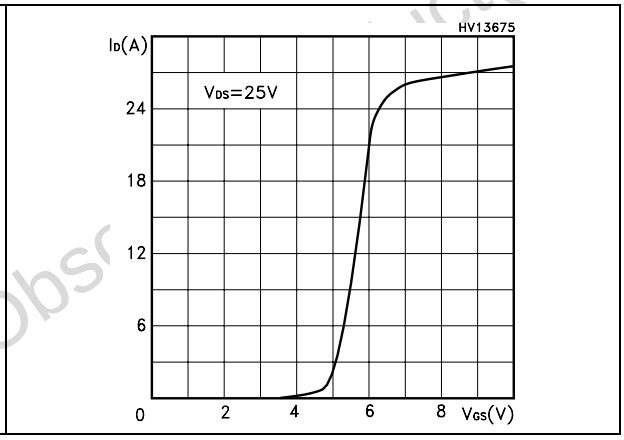


Figure 5. Transconductance

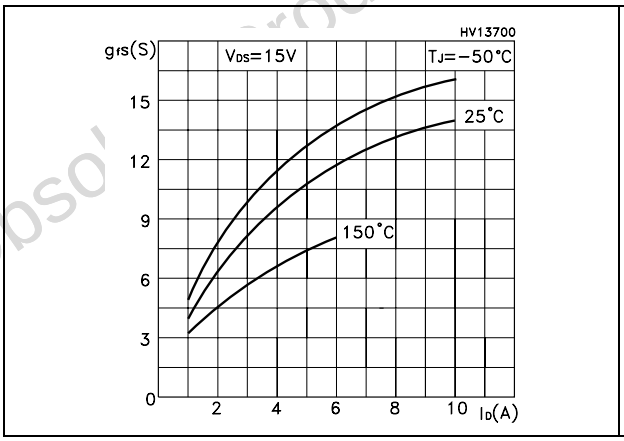


Figure 6. Static drain-source on resistance

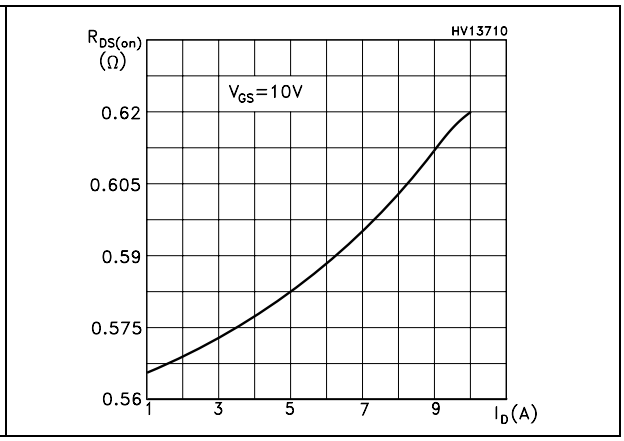


Figure 7. Gate charge vs gate-source voltage

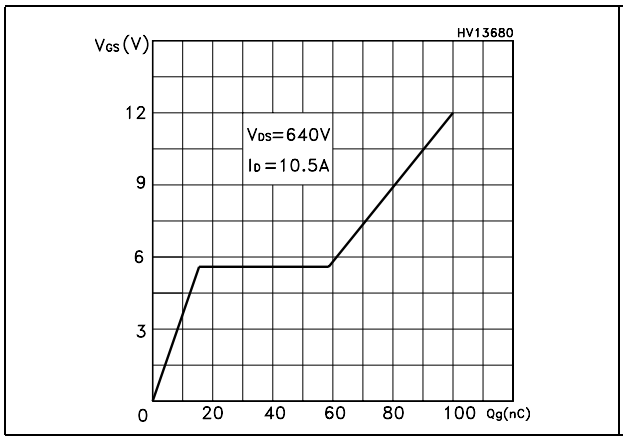


Figure 8. Capacitance variations

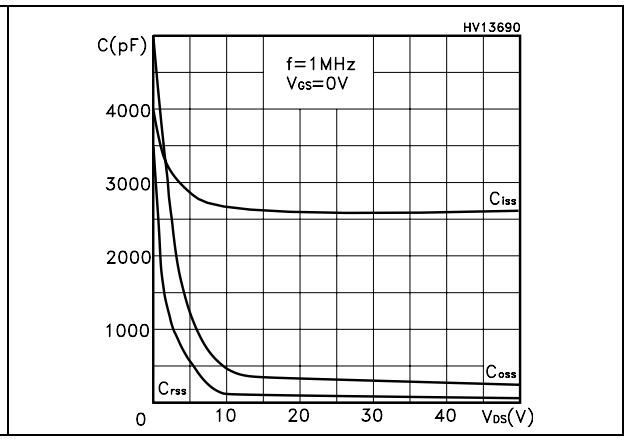


Figure 9. Normalized gate threshold voltage vs temperature

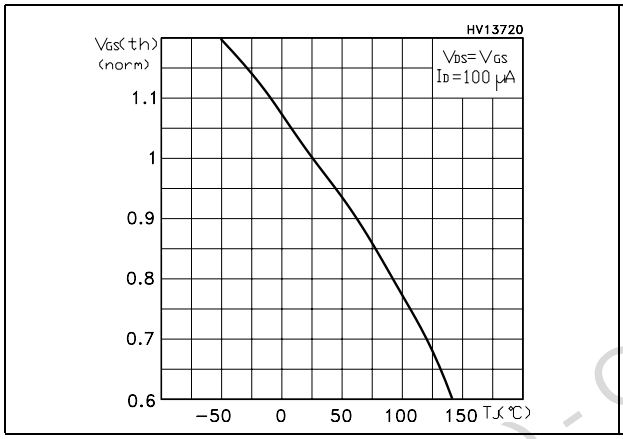


Figure 10. Normalized on resistance vs temperature

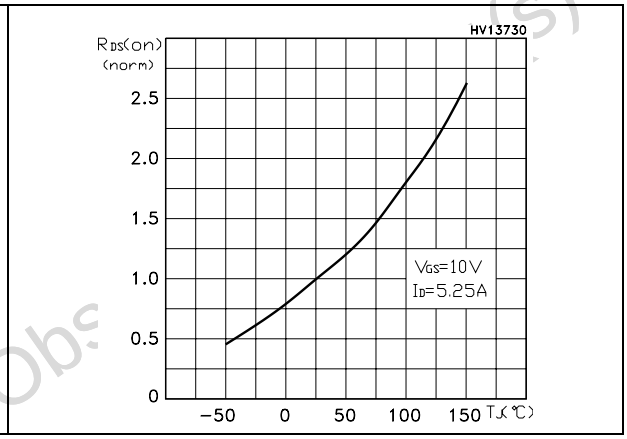


Figure 11. Source-drain diode forward characteristics

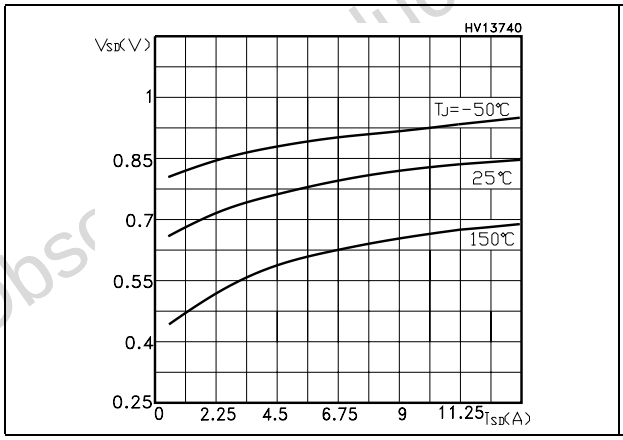


Figure 12. Normalized BV_{DSS} vs temperature

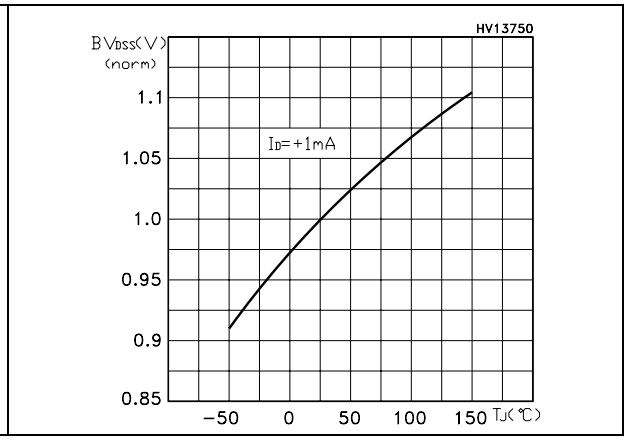
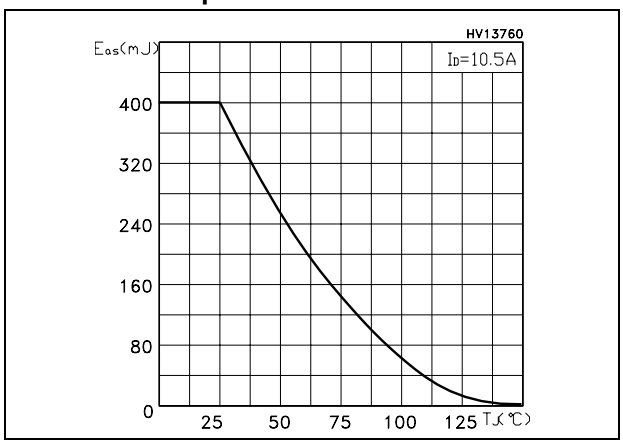


Figure 13. Maximum avalanche energy vs temperature



3 Test circuit

Figure 14. Switching times test circuit for resistive load

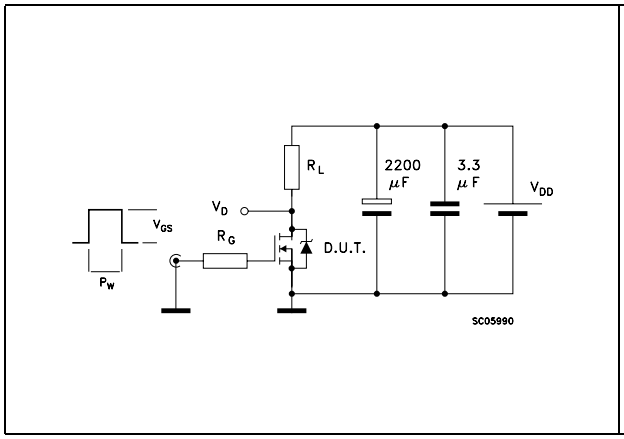


Figure 15. Gate charge test circuit

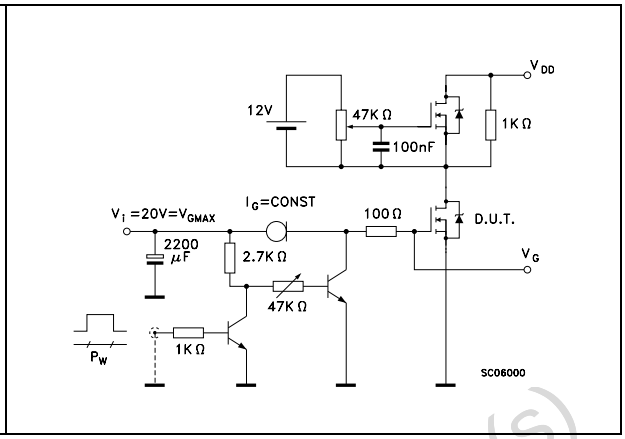


Figure 16. Test circuit for inductive load switching and diode recovery times

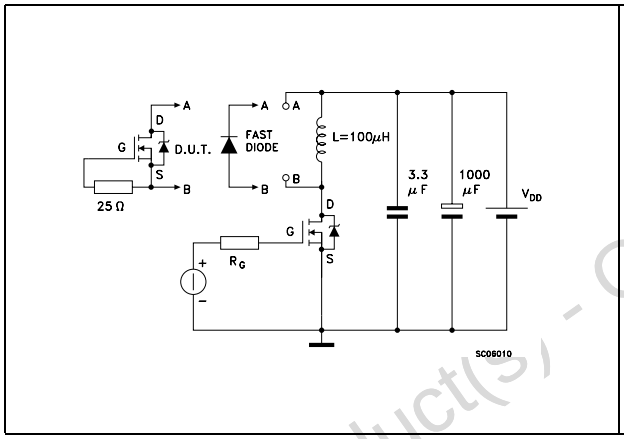


Figure 17. Unclamped Inductive load test circuit

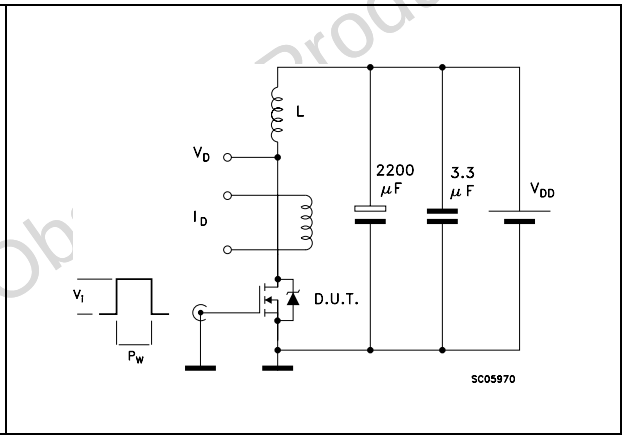


Figure 18. Unclamped inductive waveform

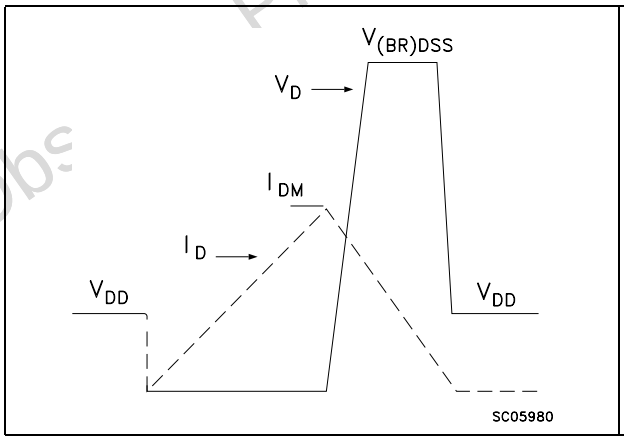
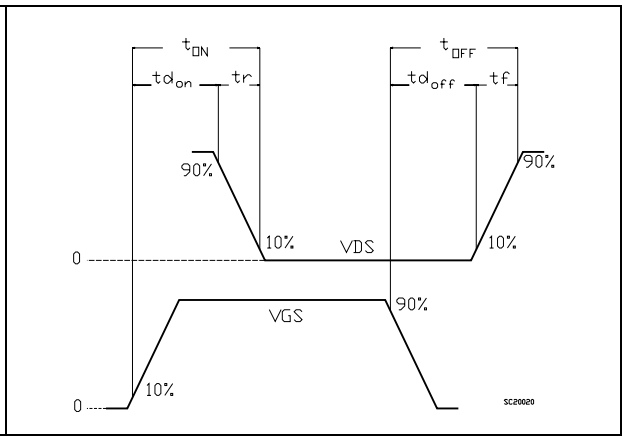


Figure 19. Switching time waveform

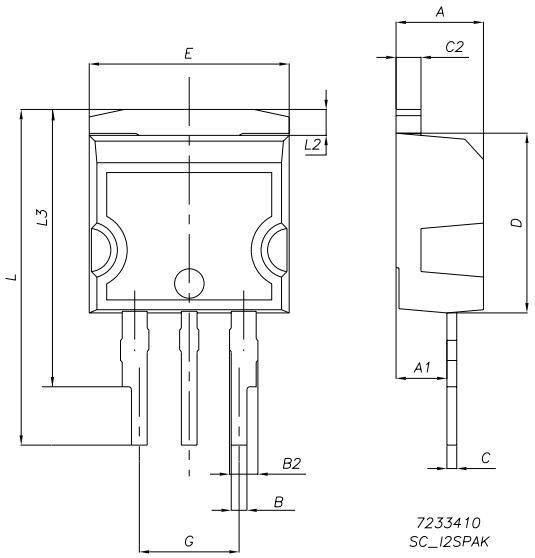


4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

I^2SPAK MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
A1	2.49		2.69	0.098		0.106
B	0.70		0.93	0.027		0.037
B2	1.14		1.70	0.045		0.067
C	0.45		0.60	0.018		0.024
C2	1.23		1.36	0.048		0.053
D	8.95		9.35	0.352		0.368
E	10.00		10.40	0.394		0.409
G	4.88		5.28	0.192		0.208
L	16.7		17.5	0.657		0.689
L2	1.27		1.4	0.05		0.055
L3	13.82		14.42	0.544		0.568



5 Revision history

Table 9. Revision history

Date	Revision	Changes
22-Jun-2004	1	First version
28-Oct-2005	2	*Figure 1: Safe operating area* changed
20-Jun-2006	3	New template, no content change

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