

## Single-Ended Bus Transceiver

## DESCRIPTION

The Si9243AEY is a monolithic bus transceiver designed to provide bidirectional serial communication in automotive diagnostic applications.

The device incorporates protection against overvoltages and short circuits to  $V_{BAT}$ . The transceiver pin is protected and can be driven beyond the  $V_{BAT}$  voltage.

The RX output is capable of driving CMOS or 1 x LS-TTL load.

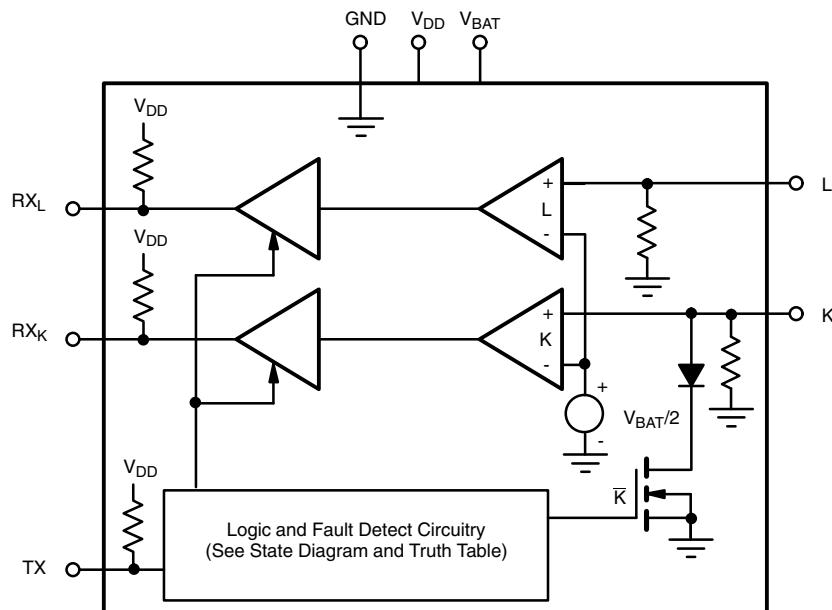
The Si9243AEY is built on the Vishay Siliconix BiC/DMOS process. This process supports bipolar transistors, CMOS, and DMOS. An epitaxial layer prevents latchup.

The Si9243AEY is available in a 8-pin SO package and operates over the automotive temperature range (- 40 °C to 125 °C). The Si9243AEY is available in both standard and lead (Pb)-free packages.

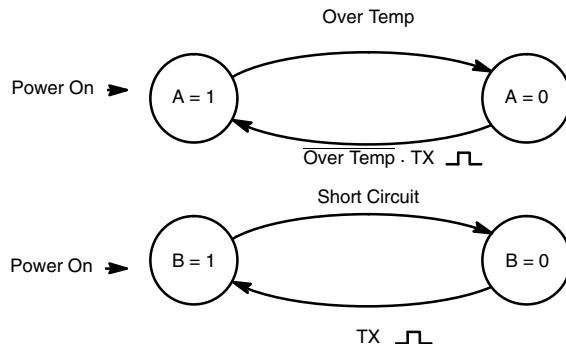
## FEATURES

- Operating Power Supply Range  
 $6 \text{ V} \leq V_{\text{BAT}} \leq 36 \text{ V}$
- Reverse Battery Protection Down to  $V_{\text{BAT}} \geq -24 \text{ V}$
- Standby Mode With Very Low Current Consumption  
 $I_{\text{BAT(SB)}} = 1 \mu\text{A}$  at  $V_{\text{DD}} = 0.5 \text{ V}$
- Low Quiescent Current in OFF Condition  
 $I_{\text{BAT}} = 120 \mu\text{A}$  and  $I_{\text{DD}} \leq 10 \text{ A}$
- ISO 9141 Compatible
- Overtemperature Shutdown Function For K Output
- Defined K Output OFF for Open GND
- Defined Receive Output Status for Open K Input
- Defined K Output OFF for TX Input Open
- Open Drain Fault Output
- 2 kV ESD
- Typical Transmit Speeds of 200 kBaud

## **PIN CONFIGURATION AND FUNCTIONAL BLOCK DIAGRAM**



## OUTPUT TABLE AND STATE DIAGRAMS



Note: Over Temp is an internal condition, not meant to be a logic signal.

INPUTS		STATE VARIABLE		OUTPUT TABLE			
TX	L	A	B	K	$RX_K$	$RX_L$	Comments
0	0	1	1	0	0	0	
1	1	1	1	1	1	1	
0	1	1	1	0	0	1	
1	0	1	1	1	1	0	
X	L	0	1	HiZ	K	L	Over Temp
0	L	1	0	HiZ	K	L	Short Circuit
1	1	1	1	1	1	1	Receive Mode
1	0	1	1	0	0	0	

X = "1" or "0"  
HiZ = High Impedance State

## ABSOLUTE MAXIMUM RATINGS

Parameter	Limit	Unit	
<b>Voltages Referenced to Ground</b>			
Voltage On $V_{BAT}$	- 24 to 45	V	
Voltage K, L	- 16 to ( $V_{BAT} + 1$ )		
Voltage Difference $V_{(V_{BAT}, K, L)}$	55		
Voltage On Any Pin (Except $V_{BAT}$ , K, L) or Max. Current	- 0.3 V to ( $V_{DD} + 0.3$ V) or 10	mA	
Voltage on $V_{DD}$	7	V	
K Pin Only, Short Circuit Duration (to $V_{BAT}$ or GND)	Continuous		
Operating Temperature ( $T_A$ )	- 40 to 125	°C	
Junction and Storage Temperature	- 55 to 150		
Thermal Impedance ( $\Theta_{JA}$ )	125	°C/W	

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## RECOMMENDED OPERATING RANGE

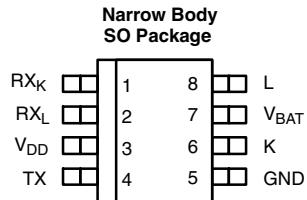
Parameter	Limit	Unit
<b>Voltages Referenced to Ground</b>		
$V_{DD}$	4.5 to 5.5	V
$V_{BAT}$	6 to 36	
K, L	6 to 36	
Digital Inputs	0 to $V_{DD}$	

SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Specified $V_{DD} = 4.5$ V to 5.5 V $V_{BAT} = 6$ V to 36 V	Temp. <sup>a</sup>	Limits - 40 to 125 °C			Unit	
				Min. <sup>b</sup>	Typ. <sup>c</sup>	Max. <sup>b</sup>		
<b>Transmitter and Logic Levels</b>								
TX Input Low Voltage	$V_{ILT}$		Full			1.5	V	
TX Input High Voltage	$V_{IHT}$		Full	3.5				
TX Input Capacitance <sup>d</sup>	$C_{INT}$		Full			10	pF	
TX Input Pull-up Resistance	$R_{TX}$	$V_{DD} = 5.5$ V, TX = 1.5 V, 3.5 V	Full	10	20	40	kΩ	
<b>K Transmit</b>								
K Output Low Voltage	$V_{OLK}$	$R_L = 510 \Omega \pm 5\%$ , $V_{BAT} = 6$ to 18	Full			0.2 $V_{BAT}$	V	
		$R_L = 1 \text{ k}\Omega \pm 5\%$ , $V_{BAT} = 16$ to 36	Full			0.2 $V_{BAT}$		
		$R_L = 510 \Omega \pm 5\%$ , $V_{BAT} = 4.5$	Full			1.2		
K Output High Voltage	$V_{OHK}$	$R_L = 510 \Omega \pm 5\%$ , $V_{BAT} = 4.5$ to 18	Full	0.95 $V_{BAT}$				
		$R_L = 1 \text{ k}\Omega \pm 5\%$ , $V_{BAT} = 16$ to 36	Full	0.95 $V_{BAT}$				
K Rise, Fall Times	$t_{p, tf}$	See Test Circuit	Full			9.6	μs	
K Output Sink Resistance	$R_{SI}$	TX = 0 V	Full			110	Ω	
K Output Capacitance <sup>d</sup>	$C_O$		Full			20	pF	
<b>Receiver</b>								
L and K Input High Voltage	$V_{IH}$		Full	0.65 $V_{BAT}$			V	
L and K Input Hysteresis <sup>c, d</sup>	$V_{HYS}$		Full		0.05 $V_{BAT}$			
L and K Input Currents	$I_{IH}$	TX = 4	$V_{IH} = V_{BAT}$	Full		20	μA	
$R_{XL}$ and $R_{XK}$ Output Low Voltage	$V_{OLR}$		$V_{ILK}, V_{ILL} = 0.35 V_{BAT}$ $I_{OLR} = 1 \text{ mA}$	Full		0.4	V	
$R_{XL}$ and $R_{XK}$ Pull-up Resistance	$R_{RX}$			Full	5	20	kΩ	
RX <sub>K</sub> Turn On Delay	$t_{d(on)}$	$R_L = 510 \Omega \pm 5\%$ , $V_{BAT} = 6$ V to 18 V $C_L = 10 \text{ nF}$ , See Test Circuit	Full		3	10	μs	
		$R_L = 1 \text{ k}\Omega \pm 5\%$ , $V_{BAT} = 16$ V to 36 V $C_L = 4.7 \text{ nF}$ , See Test Circuit	Full		3	10		
RX <sub>K</sub> Turn Off Delay	$t_{d(off)}$	$R_L = 510 \Omega \pm 5\%$ , $V_{BAT} = 6$ V to 18 V $C_L = 10 \text{ nF}$ , See Test Circuit	Full		3	10		
		$R_L = 1 \text{ k}\Omega \pm 5\%$ , $V_{BAT} = 16$ V to 36 V $C_L = 4.7 \text{ nF}$ , See Test Circuit	Full		3	10		
<b>Supplies</b>								
Bat Supply Current On	$I_{BAT(on)}$	TX = 0 V, $V_{BAT} \leq 16$ V		Full		1.2	3	mA
Bat Supply Current Off	$I_{BAT(off)}$	$V_{IHT} \leq V_{TX}, V_{IHK} \leq V_K, V_{IHL} \leq V_L$ $V_{BAT} \leq 12$ V		Full		120	220	μA
Bat Supply Current Standby	$I_{BAT(SB)}$	$V_{DD} \leq 0.5$ V, $V_{BAT} \leq 12$ V		Full		< 1	10	
Logic Supply Current On	$I_{DD(on)}$	$V_{DD} \leq 5.5$ V, TX = 0 V		Full		1.4	2.3	mA
Logic Supply Current Off	$I_{DD(off)}$	$V_{IHT} \leq V_{TX}, V_{IHK} \leq V_K, V_{IHL} \leq V_L$ $V_{BAT} \leq 12$ V		Full			10	μA
<b>Miscellaneous</b>								
TX Transmit Baud Rate	$BR_T$	$R_L = 510 \Omega, C_L = 10 \text{ nF}$		Full	10.4			kBaud
$R_{XL}$ and $R_{XK}$ Receive Baud Rate <sup>c</sup>	$BR_R$	6 V < $V_{BAT} < 16$ V, $C_{RX} = 20 \text{ pF}$		Full		200		
Transmission Frequency	$f_{K-RXK}$	6 V < $V_{BAT} < 16$ V, $R_K = 510 \Omega, C_K \leq 1.3 \text{ nF}$		Full	50	200		kHz
TX Minimum Pulse Width <sup>d, e</sup>	$t_{TX}$			Full	1			μs
Over Temperature Shutdown <sup>d</sup>	$T_{SHUT}$	Temperature Rising		160	180			°C
Temperature Shutdown Hysteresis <sup>c</sup>	$T_{HYST}$					30		

Notes:

- Room = 25 °C, Cold and Hot = as determined by the operating temperature suffix.
- The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
- Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
- Guaranteed by design, not subject to production test.
- Minimum pulse width to reset a fault condition.

## PIN CONFIGURATION



Top View

## ORDERING INFORMATION

Part Number	Temperature Range
Si9243AEY-T1	- 40 to 125 °C
Si9243AEY-T1-E3 (Lead (Pb)-free)	

## PIN DESCRIPTION

Pin Number	Symbol	Description
1	$RX_K$	K Receiver, Output
2	$RX_L$	L Receiver, Output
3	$V_{DD}$	Positive Power Supply
4	TX	Transmit, Input
5	GND	Ground Connection
6	K	K Transmit/Receive, Bidirectional
7	$V_{BAT}$	Battery Power Supply
8	L	L Transmit, Input

## FUNCTIONAL DESCRIPTION

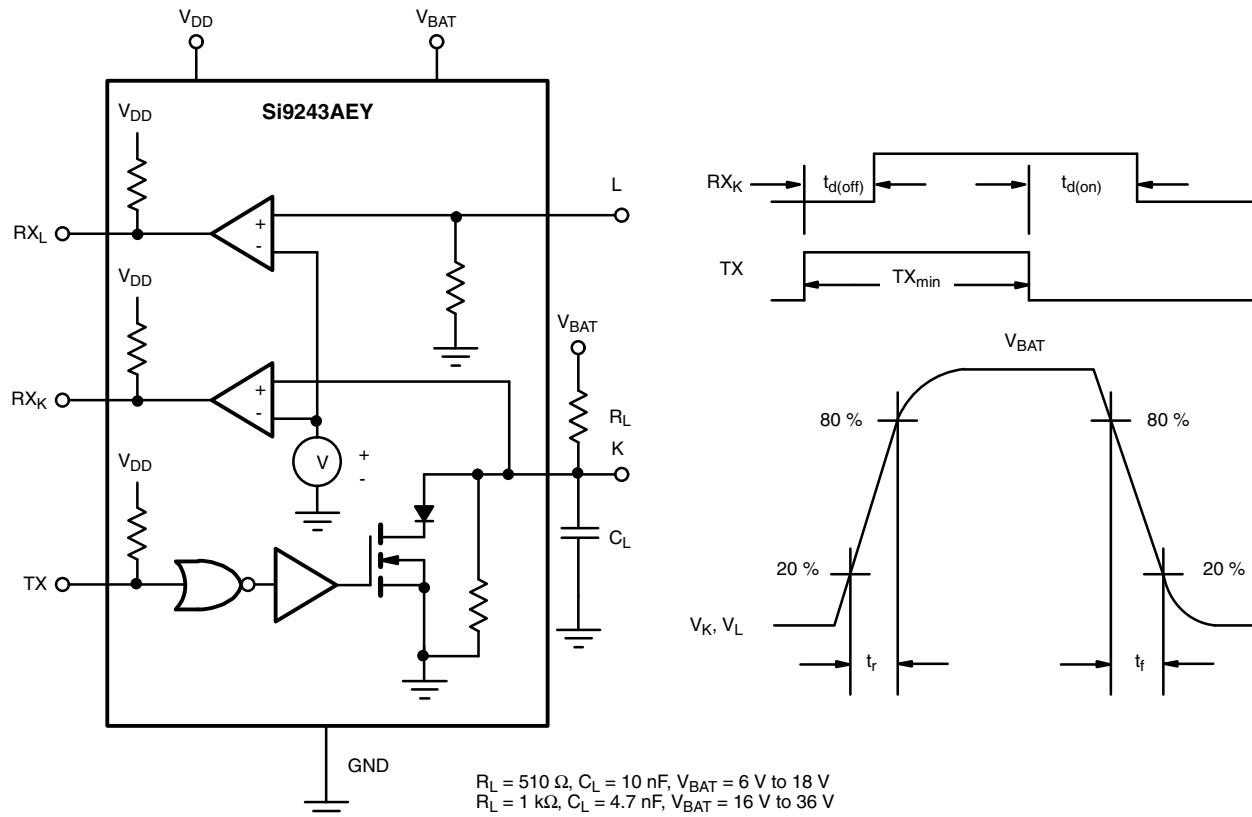
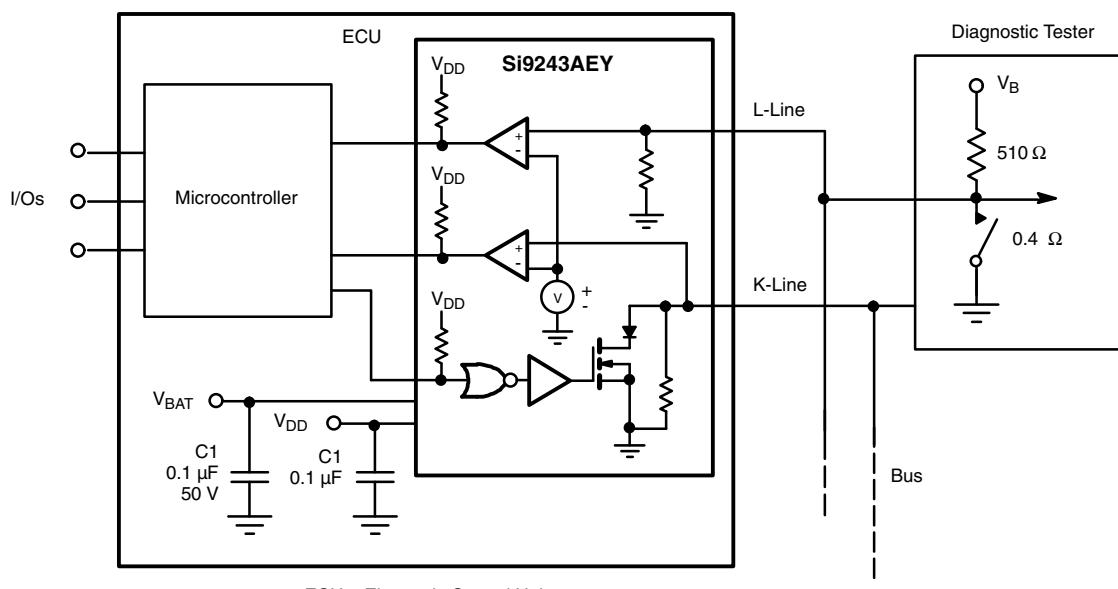
The Si9243AEY can be either in transmit or receive mode and it contains over temperature, and short circuit  $V_{BAT}$  fault detection circuits.

The voltage on the K and L pins are internally compared to  $V_{BAT}/2$ . If the voltage on the K or L pin is less than  $V_{BAT}/2$  then  $RX_K$  or  $RX_L$  output will be "low". If the voltage on the K or L pin is greater than  $V_{BAT}/2$  then  $RX_K$  or  $RX_L$  output will be "high".

In order to be in transmit mode, TX must be set "low". The TX signal is then internally inverted and turns the MOSFET on, causing the K pin to be "low". In transmit mode, the processor monitors the  $RX_K$  and TX. When the two mirror each other there is no fault. In the event of over temperature, or short circuit to  $V_{BAT}$ , the Si9243AEY will turn off the K

output to protect the IC. The K pin will stay in high impedance and  $RX_K$  will follow the K pin. The fault will be reset when TX is toggled high.  $RX_K$ ,  $RX_L$  and TX pins have internal pull up resistor to  $V_{DD}$  while K and L pins have internal pull down resistors. When any one of the TX,  $V_{BAT}$  or GND pins is open the K output is off.

When the TX pin is set "high" the Si9243AEY is in receive mode and the internal MOSFET is turned off.  $RX_L$  and  $RX_K$  outputs will follow L and K inputs respectively.

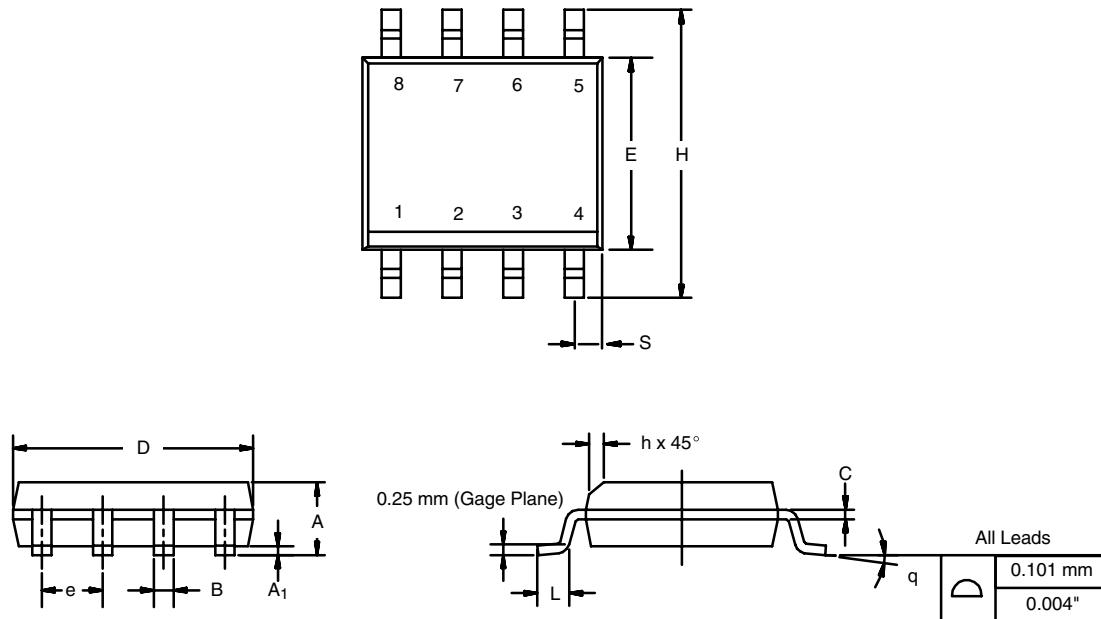
**TEST CIRCUIT AND TIMING DIAGRAMS (TRANSMIT ONLY)**

**APPLICATIONS CIRCUIT**


ECU = Electronic Control Unit

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?70788](http://www.vishay.com/ppg?70788).

### SOIC (NARROW): 8-LEAD

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06				
DWG: 5498				

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