

Precision Low Voltage Amplifier; DC to 2 kHz

Features

- Low Offset: 10 μV Max
- Low Drift: 0.05 $\mu\text{V}/^\circ\text{C}$ Max
- Low Noise
 - 6 $\text{nV}/\sqrt{\text{Hz}}$ @ 0.5 Hz
 - 0.1 to 10 Hz = 125 nVp-p
 - 1/f corner @ 0.08 Hz
- Open-Loop Voltage Gain
 - 1000 Trillion Typ
 - 10 Billion Min
- Rail-to-Rail Output Swing
- Slew rate: 5 $\text{V}/\mu\text{s}$

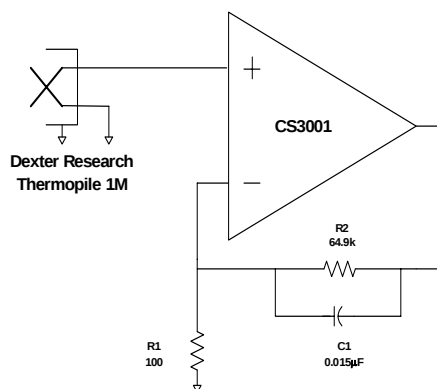
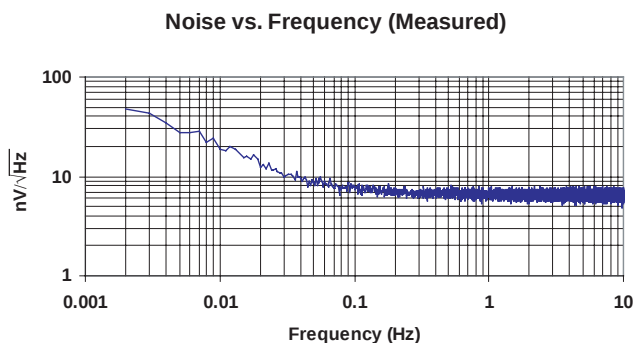
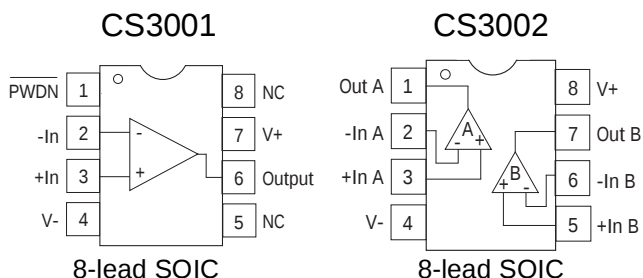
Applications

- Thermocouple/Thermopile Amplifiers
- Load Cell and Bridge Transducer Amplifiers
- Precision Instrumentation
- Battery-Powered Systems

Description

The CS3001 single amplifier and the CS3002 dual amplifier are designed for precision amplification of low level signals and are ideally suited to applications that require very high closed loop gains. These amplifiers achieve excellent offset stability, super high open loop gain, and low noise over time and temperature. The devices also exhibit excellent CMRR and PSRR. The common mode input range includes the negative supply rail. The amplifiers operate with any total supply voltage from 2.7 V to 6.7 V (± 1.35 V to ± 3.35 V).

Pin Configurations



Thermopile Amplifier with a Gain of 650 V/V

TABLE OF CONTENTS

1. CHARACTERISTICS AND SPECIFICATIONS	3
1.1 Electrical Characteristics	3
1.2 Absolute Maximum Ratings	4
2. PERFORMANCE PLOTS	4
3. CS3001/CS3002 OVERVIEW	7
3.1 Open Loop Gain and Phase Response	7
3.2 Open Loop Gain and Stability Compensation	8
3.3 Powerdown (PDWN)	10
3.4 Applications	10
4. PACKAGE DRAWING	13
5. ORDERING INFORMATION	14

LIST OF FIGURES

Figure 1. Noise vs Frequency (Measured)	4
Figure 2. 0.01 Hz to 10 Hz Noise	4
Figure 3. Noise vs Frequency	4
Figure 4. Offset Voltage Stability (DC to 3.2 Hz)	4
Figure 5. Open Loop Gain and Phase vs Frequency	5
Figure 6. Open Loop Gain and Phase vs Frequency (Expanded)	5
Figure 7. Input Bias Current vs Supply Voltage (CS3002)	6
Figure 8. Input Bias Current vs Common Mode Voltage	6
Figure 9. CS3001/CS3002 Open Loop Gain and Phase Response	7
Figure 10. Non-Inverting Gain Configuration	8
Figure 11. Non-Inverting Gain Configuration with Compensation	9
Figure 12. Loop Gain Plot: Unity Gain and with Pole-Zero Compensation	10
Figure 13. Thermopile Amplifier with a Gain of 650 V/V	11
Figure 14. Load Cell Bridge Amplifier and A/D Converter	12

Contacting Cirrus Logic Support

For all product questions and inquiries contact a Cirrus Logic Sales Representative.

To find one nearest you go to www.cirrus.com

IMPORTANT NOTICE

Cirrus Logic, Inc. and its subsidiaries ("Cirrus") believe that the information contained in this document is accurate and reliable. However, the information is subject to change without notice and is provided "AS IS" without warranty of any kind (express or implied). Customers are advised to obtain the latest version of relevant information to verify, before placing orders, that information being relied on is current and complete. All products are sold subject to the terms and conditions of sale supplied at the time of order acknowledgment, including those pertaining to warranty, patent infringement, and limitation of liability. No responsibility is assumed by Cirrus for the use of this information, including use of this information as the basis for manufacture or sale of any items, or for infringement of patents or other rights of third parties. This document is the property of Cirrus and by furnishing this information, Cirrus grants no license, express or implied under any patents, mask work rights, copyrights, trademarks, trade secrets or other intellectual property rights. Cirrus owns the copyrights associated with the information contained herein and gives consent for copies to be made of the information only for use within your organization with respect to Cirrus integrated circuits or other products of Cirrus. This consent does not extend to other copying such as copying for general distribution, advertising or promotional purposes, or for creating any work for resale.

An export permit needs to be obtained from the competent authorities of the Japanese Government if any of the products or technologies described in this material and controlled under the "Foreign Exchange and Foreign Trade Law" is to be exported or taken out of Japan. An export license and/or quota needs to be obtained from the competent authorities of the Chinese Government if any of the products or technologies described in this material is subject to the PRC Foreign Trade Law and is to be exported or taken out of the PRC.

CERTAIN APPLICATIONS USING SEMICONDUCTOR PRODUCTS MAY INVOLVE POTENTIAL RISKS OF DEATH, PERSONAL INJURY, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE ("CRITICAL APPLICATIONS"). CIRRUS PRODUCTS ARE NOT DESIGNED, AUTHORIZED OR WARRANTED FOR USE IN AIRCRAFT SYSTEMS, MILITARY APPLICATIONS, PRODUCTS SURGICALLY IMPLANTED INTO THE BODY, LIFE SUPPORT PRODUCTS OR OTHER CRITICAL APPLICATIONS (INCLUDING MEDICAL DEVICES, AIRCRAFT SYSTEMS OR COMPONENTS AND PERSONAL OR AUTOMOTIVE SAFETY OR SECURITY DEVICES). INCLUSION OF CIRRUS PRODUCTS IN SUCH APPLICATIONS IS UNDERSTOOD TO BE FULLY AT THE CUSTOMER'S RISK AND CIRRUS DISCLAIMS AND MAKES NO WARRANTY, EXPRESS, STATUTORY OR IMPLIED, INCLUDING THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR PARTICULAR PURPOSE, WITH REGARD TO ANY CIRRUS PRODUCT THAT IS USED IN SUCH A MANNER. IF THE CUSTOMER OR CUSTOMER'S CUSTOMER USES OR PERMITS THE USE OF CIRRUS PRODUCTS IN CRITICAL APPLICATIONS, CUSTOMER AGREES, BY SUCH USE, TO FULLY INDEMNIFY CIRRUS, ITS OFFICERS, DIRECTORS, EMPLOYEES, DISTRIBUTORS AND OTHER AGENTS FROM ANY AND ALL LIABILITY, INCLUDING ATTORNEYS' FEES AND COSTS, THAT MAY RESULT FROM OR ARISE IN CONNECTION WITH THESE USES.

Cirrus Logic, Cirrus, and the Cirrus Logic logo designs are trademarks of Cirrus Logic, Inc. All other brand and product names in this document may be trademarks or service marks of their respective owners.

1. CHARACTERISTICS AND SPECIFICATIONS

1.1 Electrical Characteristics

V+ = +5 V, V- = 0V, VCM = 2.5 V (Note 1)

Parameter		CS3001/CS3002			Unit
		Min	Typ	Max	
Input Offset Voltage (Note 2)	•	-	-	±10	μV
Average Input Offset Drift (Note 2)	•	-	±0.01	±0.05	μV/°C
Long Term Input Offset Voltage Stability		(Note 3)			
Input Bias Current $T_A = 25^\circ\text{C}$	•	-	±100	-	pA
	•	-	-	±1000	pA
Input Offset Current $T_A = 25^\circ\text{C}$	•	-	±200	-	pA
	•	-	-	±2000	pA
Input Noise Voltage Density $R_S = 100\ \Omega$, $f_0 = 1\ \text{Hz}$ $R_S = 100\ \Omega$, $f_0 = 1\ \text{kHz}$		-	6		nV/√Hz
		-	6		nV/√Hz
Input Noise Voltage 0.1 to 10 Hz		-	125		nV _{p-p}
Input Noise Current Density $f_0 = 1\ \text{Hz}$		-	100		fA/√Hz
Input Noise Current 0.1 to 10 Hz		-	1.9		pA _{p-p}
Input Common Mode Voltage Range	•	-0.1	-	(V+)-1.25	V
Common Mode Rejection Ratio (dc) (Note 4)	•	115	120	-	dB
Power Supply Rejection Ratio	•	120	136	-	dB
Large Signal Voltage Gain $R_L = 2\ \text{k}\Omega$ to V+/2 (Note 5)	•	200	300	-	dB
Output Voltage Swing $R_L = 2\ \text{k}\Omega$ to V+/2 $R_L = 100\ \text{k}\Omega$ to V+/2	•	+4.7	-	-	V
			+4.99		V
Slew Rate $R_L = 2\ \text{k}\Omega$, 100 pF			5	-	V/μs
Overload Recovery Time		-	100	-	μs
Supply Current CS3001 CS3002 PWDN active (CS3001 Only) (Note 6)	•	-	2.1	2.8	mA
	•	-	3.6	4.8	mA
	•			15	μA
PWDN Threshold (Note 6)	•	(V+) -1.0	-	-	V
Start-up Time (Note 7)	•	-	9	12	ms

- Notes:
1. Symbol “•” denotes specification applies over -40 to +85 °C.
 2. This parameter is guaranteed by design and laboratory characterization. Thermocouple effects prohibit accurate measurement of these parameters in automatic test systems.
 3. 1000-hour life test data @ 125 °C indicates randomly distributed variation approximately equal to measurement repeatability of 1 μV.
 4. Measured within the specified common mode range limits.
 5. Guaranteed within the output limits of (V+ -0.3 V) to (V- +0.3 V). Tested with proprietary production test method.
 6. PWDN input has an internal pullup resistor to V+ of approximately 800 kΩ and is the major source of current consumption when PWDN is active low.
 7. The device has a controlled start-up behavior due to its complex open loop gain characteristics. Start-up time applies when supply voltage is applied or when PWDN is released.

1.2 Absolute Maximum Ratings

Parameter	Min	Typ	Max	Unit
Supply Voltage [(V+) - (V-)]			6.8	V
Input Voltage	V- -0.3		V+ +0.3	V
Storage Temperature Range	-65		+150	°C

2. PERFORMANCE PLOTS

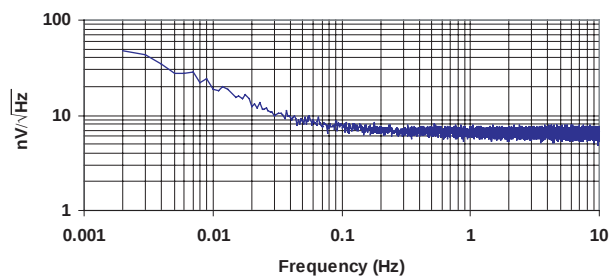


Figure 1. Noise vs Frequency (Measured)

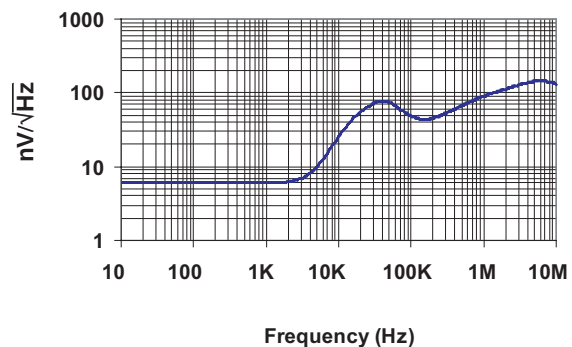


Figure 3. Noise vs Frequency

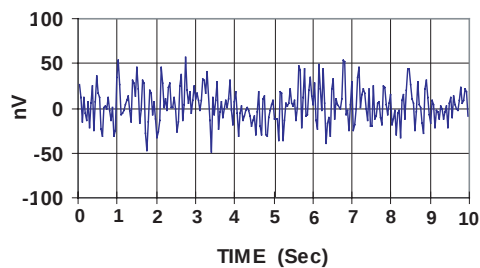


Figure 2. 0.01 Hz to 10 Hz Noise

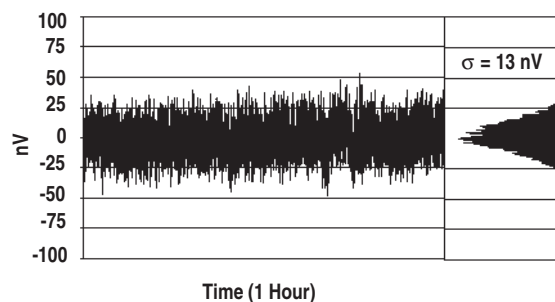


Figure 4. Offset Voltage Stability (DC to 3.2 Hz)

Performance Plots (Cont.)

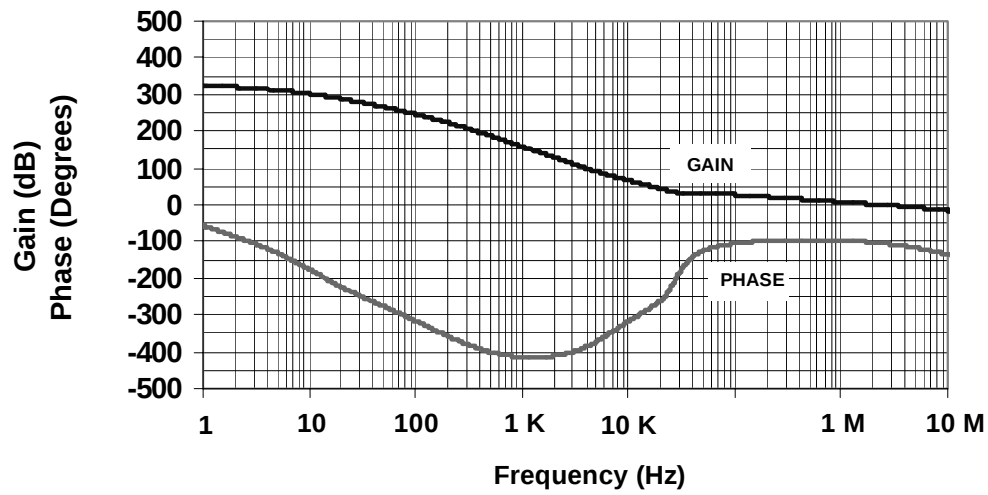


Figure 5. Open Loop Gain and Phase vs Frequency

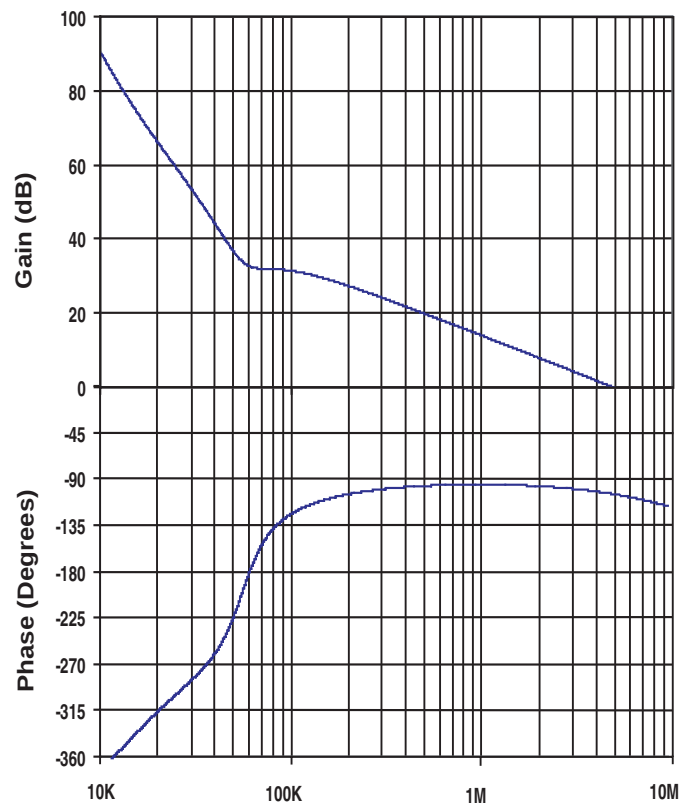


Figure 6. Open Loop Gain and Phase vs Frequency (Expanded)

Performance Plots (Cont.)

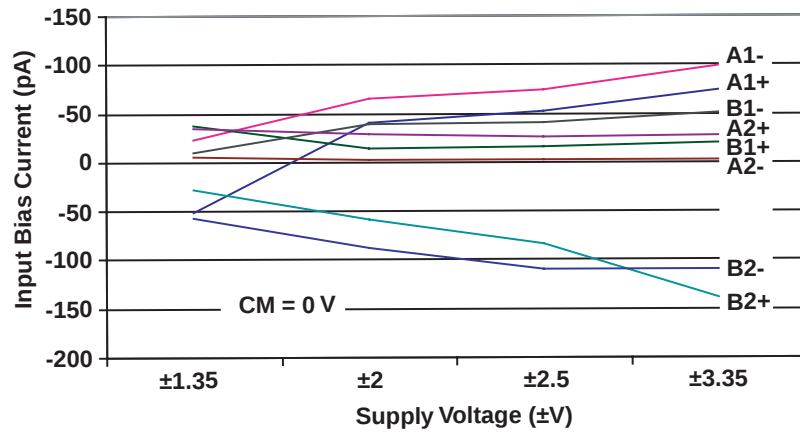


Figure 7. Input Bias Current vs Supply Voltage (CS3002)

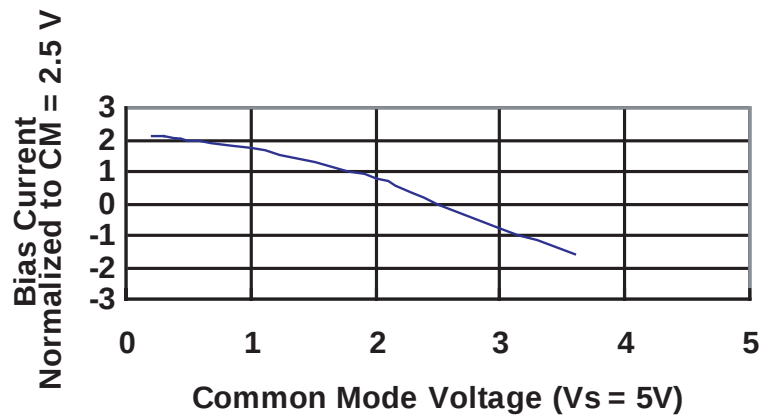


Figure 8. Input Bias Current vs Common Mode Voltage

3. CS3001/CS3002 OVERVIEW

The CS3001/CS3002 amplifiers are designed for precision measurement of signals from DC to 2 kHz when operating from a supply voltage of +2.7 V to +6.7 V (± 1.35 to ± 3.35 V). The amplifiers are designed with a patented architecture that utilizes multiple amplifier stages to yield very high open loop gain at frequencies of 10 kHz and below. The amplifiers yield low noise and low offset drift while consuming relatively low supply current. An increase in noise floor above 2 kHz is the result of intermediate stages of the amplifier being operated at very low currents. The amplifiers are intended

for amplifying small signals with large gains in applications where the output of the amplifier can be band-limited to frequencies below 2 kHz.

3.1 Open Loop Gain and Phase Response

Figure 9 illustrates the open loop gain and phase response of the CS3001/CS3002. The gain slope of the amplifier is about -100 dB/decade between 500 Hz and 60 kHz and transitions to -20 dB/decade between 60 kHz and its unity gain crossover frequency at about 4.8 MHz. Phase margin at unity gain is about 70 degrees; gain margin is about 20 dB.

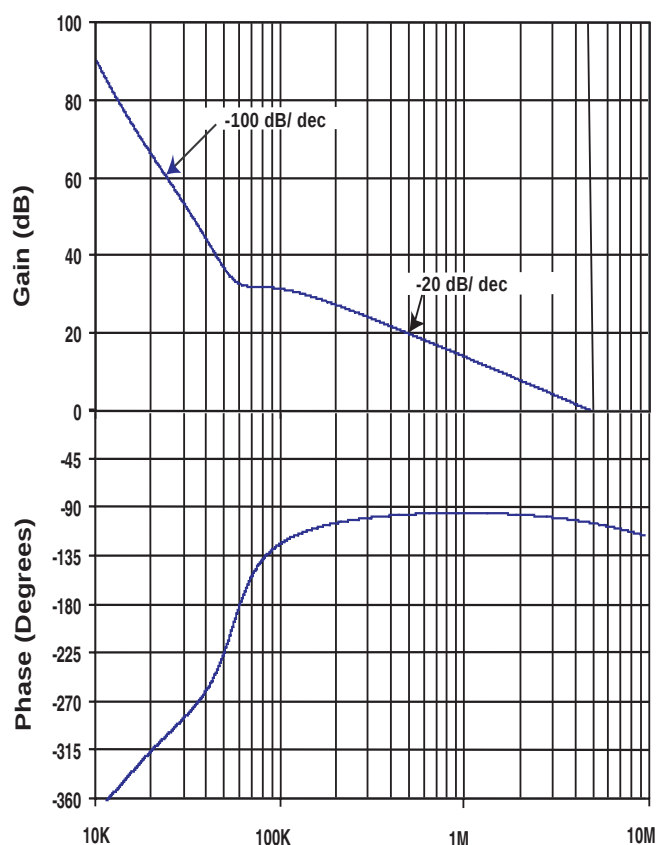


Figure 9. CS3001/CS3002 Open Loop Gain and Phase Response

3.2 Open Loop Gain and Stability Compensation

The CS3001 and CS3002 achieve ultra-high open loop gain. Figure 10 illustrates the amplifier in a non-inverting gain configuration. The open loop gain and phase plots indicate that the amplifier is stable for closed-loop gains less than 50 V/V. For a gain of 50, the phase margin is between 40° and 60° depending upon the loading conditions. As shown in Figure 11 on page 9, the op amp has an input capacitance at the + and – signal inputs of typically 50 pF. This capacitance adds an additional pole in

the loop gain transfer function at a frequency of $f = 1/(2\pi R \cdot C_{in})$ where R is the parallel combination of R1 and R2 ($R1 \parallel R2$). A higher value for R produces a pole at a lower frequency, thus reducing the phase margin. R1 is recommended to be less than or equal to 100 ohms, which results in a pole at 30 MHz or higher. If a higher value of R1 is desired, a compensation capacitor (C2) should be added in parallel with R2. C2 should be chosen such that $R2 \cdot C2 \geq R1 \cdot C_{in}$.

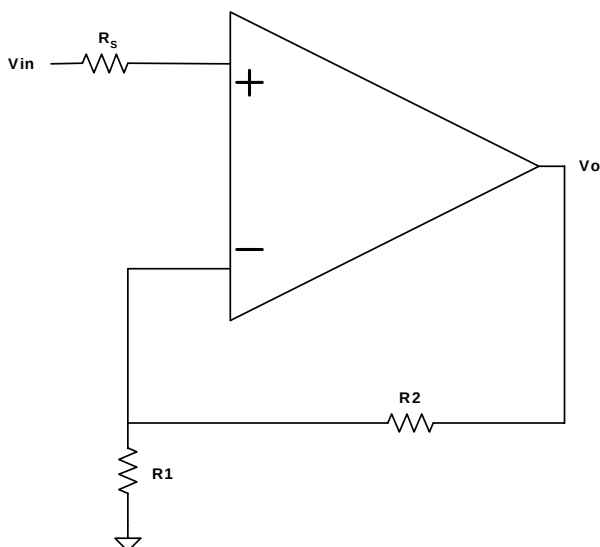


Figure 10. Non-Inverting Gain Configuration

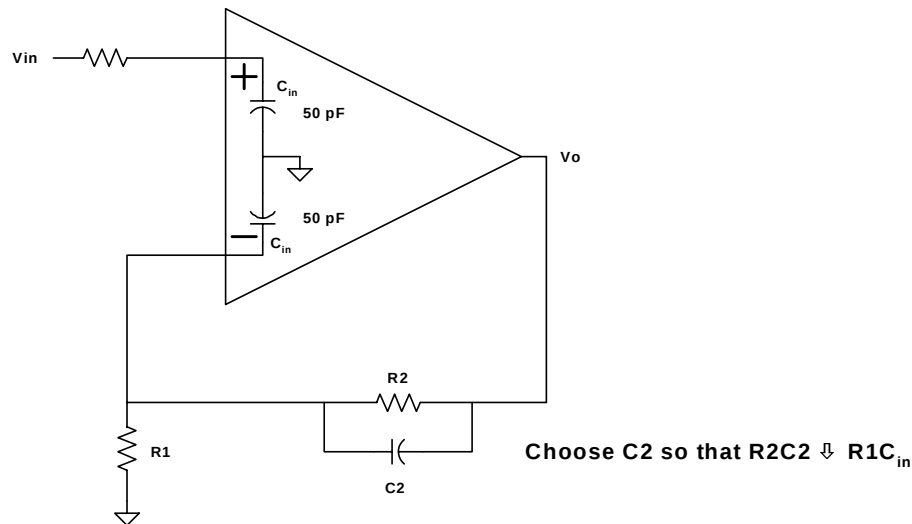


Figure 11. Non-Inverting Gain Configuration with Compensation

The feedback capacitor C2 is required for closed-loop gains greater than 50 V/V. The capacitor introduces a pole and a zero in the loop gain transfer function,

$$T = \frac{-\left(1 + \frac{s}{z_1}\right)}{\left(1 + \frac{s}{p_1}\right)} A_{ol}$$

$$p_1 = \frac{1}{2\pi(R_1 \parallel R_2)C_2} \cong \frac{1}{2\pi(R_1 C_2)} \quad \text{for} \quad R_2 \gg R_1$$

$$z_1 = \frac{1}{2\pi(A \times R_1)C_2} \quad \text{where} \quad |A| = \frac{R_2}{R_1}$$

This indicates that the separation of the pole and the zero is governed by the closed loop gain. It is required that the zero falls on the steep slope (–100 dB/decade) of the loop gain plot so that there is some gain higher than 0 dB (typically 20 dB) at the hand-over frequency (the frequency at which the slope changes from – 100 dB/decade to –20 dB/decade).

The loop gain plot shown in Figure 12 illustrates the unity gain configuration, and indicates how this is modified when using the amplifier in a higher gain configuration with compensation. If it is configured for higher gain, for example, 60 dB, the x-axis will move up by 60 dB (line B). Capacitor C2 adds a zero and a pole. The modified plot indicates the effects of introducing the pole and zero due to capacitor C2. The pole can be located at any frequency higher than the hand-over frequency, the zero has to be at a frequency lower than the hand-over frequency so as to provide adequate gain margin. The separation between the pole and the zero is governed by the closed loop gain. The zero (z_1) occurs at the intersection of the -100 dB/decade and -80 dB/decade slopes. The point X in the figure should be at closed loop gain plus 20 dB gain margin. The value for $C2 = 1/(2\pi R1 p1)$. Using $p1 = 1$ MHz works very well and is independent of gain. As the closed loop gain is changed, the zero location is also modified if R1 remains fixed.

Capacitor C2 can be increased in value to limit the amplifier's rising noise above 2 kHz.

3.3 Powerdown (PDWN)

The CS3001 single amplifier provides a power-down function on pin 1. If this pin is left open the amplifier will operate normally. If the powerdown is asserted low, the amplifier will go into a low power state. There is a pull-up resistor (approximately 800 k ohm) inside the amplifier from pin 1 to the V+ supply. The current through this pull-up resistor is the main source of current drain in the powerdown state.

3.4 Applications

The CS3001 and CS3002 amplifiers are optimum for applications that require high gain and low drift. Figure 13 illustrates a thermopile amplifier with a gain of 650 V/V. The thermopile outputs only a few millivolts when subjected to infrared radiation. The amplifier is compensated and bandlimited by C1 in combination with R2.

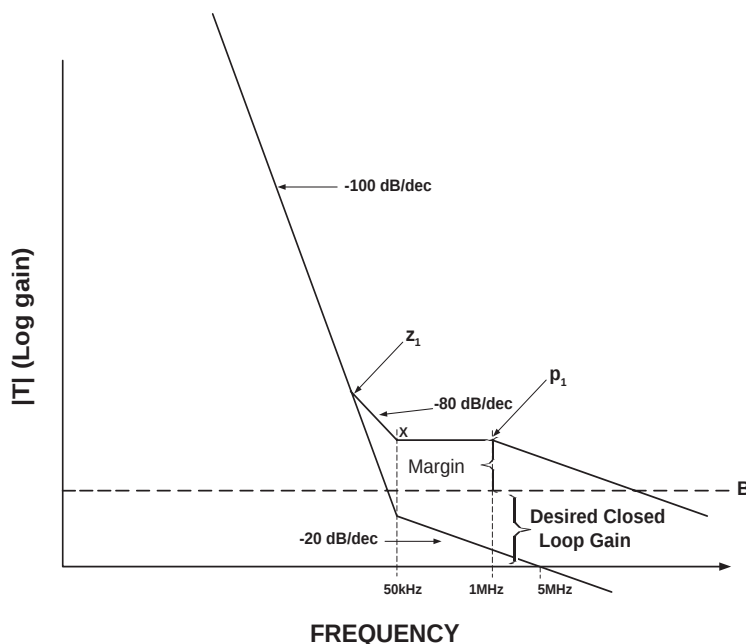


Figure 12. Loop Gain Plot: Unity Gain and with Pole-Zero Compensation

Figure 14 on page 12 illustrates a load cell bridge amplifier with a gain of 768 V/V. The load cell is excited with +5 V and has a 1 mV/V sensitivity. Its full scale output signal is amplified to produce a

fully differential ± 3.8 V into the CS5510/12 A/D converter. This circuit operates from +5 V.

A similar circuit operating from +3 V can be constructed using the CS5540/CS5541 A/D converters.

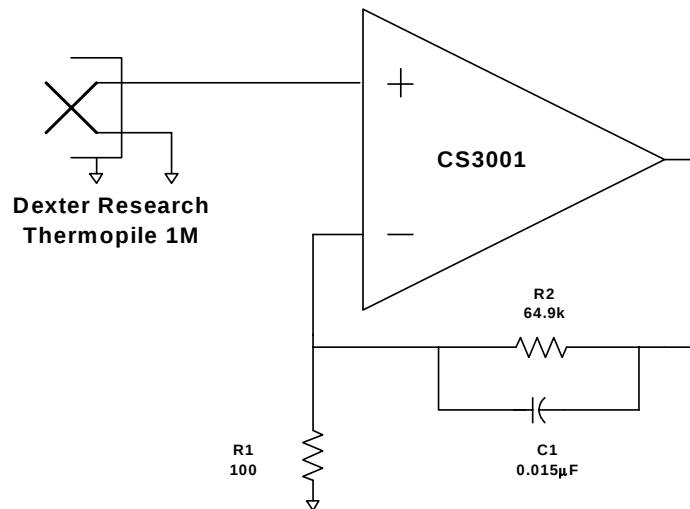


Figure 13. Thermopile Amplifier with a Gain of 650 V/V

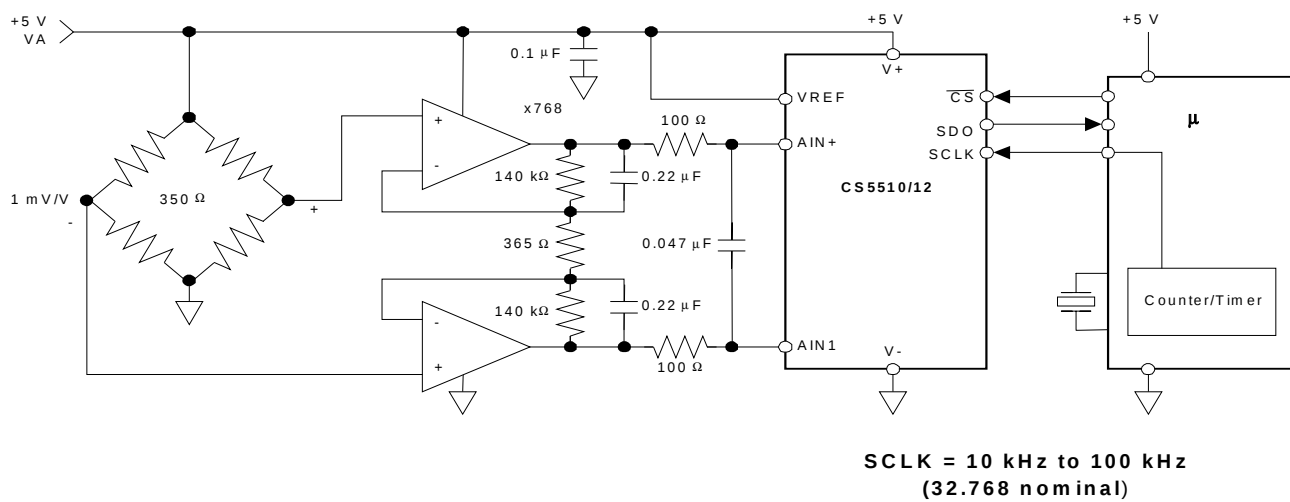
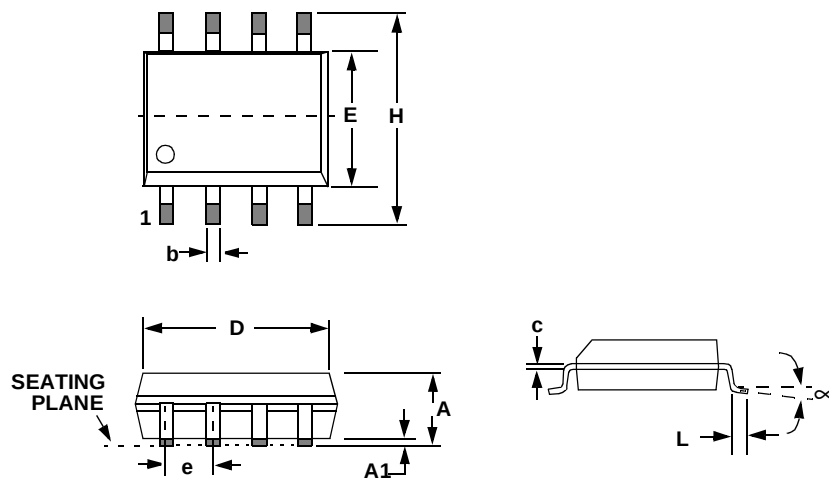


Figure 14. Load Cell Bridge Amplifier and A/D Converter

4. PACKAGE DRAWING

8L SOIC (150 MIL BODY) PACKAGE DRAWING



DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
B	0.013	0.020	0.33	0.51
C	0.007	0.010	0.19	0.25
D	0.189	0.197	4.80	5.00
E	0.150	0.157	3.80	4.00
e	0.040	0.060	1.02	1.52
H	0.228	0.244	5.80	6.20
L	0.016	0.050	0.40	1.27
∞	0°	8°	0°	8°

JEDEC # : MS-012

5. ORDERING INFORMATION

Part #	Temperature Range	Package Description
CS3001-IS	-40 °C to +85 °C	8-lead SOIC
CS3002-IS	-40 °C to +85 °C	8-lead SOIC

Note: Add the letter R to the Part # to order reels. There are 2000 pieces per reel.