

74LV165A-Q100

8-bit parallel-in/serial-out shift register

Rev. 3 — 28 March 2014

Product data sheet

1. General description

The 74LV165A-Q100 is an 8-bit parallel-load or serial-in shift register with complementary serial outputs (Q_7 and \overline{Q}_7) available from the last stage. When the parallel-load input (PL) is LOW, parallel data from the inputs D0 to D7 are loaded into the register asynchronously. When input PL is HIGH, data enters the register serially at the input DS. It shifts one place to the right ($Q_0 \rightarrow Q_1 \rightarrow Q_2$, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by tying the output Q_7 to the input DS of the succeeding stage. The clock input is a gate-OR structure which allows one input to be used as an active LOW clock enable input (\overline{CE}) input. The pin assignment for the inputs CP and \overline{CE} is arbitrary and can be reversed for layout convenience. The LOW-to-HIGH transition of the input \overline{CE} should only take place while CP HIGH for predictable operation.

Schmitt-trigger action at all inputs, makes the circuit tolerant for slower input rise and fall times. It is fully specified for partial-power-down applications using I_{OFF} . The I_{OFF} circuitry disables the output, preventing the damaging current backflow through the device when it is powered down.

This product has been qualified to the Automotive Electronics Council (AEC) standard Q100 (Grade 3) and is suitable for use in automotive applications.

2. Features and benefits

- Automotive product qualification in accordance with AEC-Q100 (Grade 3)
 - ◆ Specified from -40°C to $+85^{\circ}\text{C}$
- Wide supply voltage range from 2.0 V to 5.5 V
- Synchronous parallel-to-serial applications
- Synchronous serial input for easy expansion
- Latch-up performance exceeds 250 mA
- CMOS LOW power consumption
- 5.5 V tolerant inputs/outputs
- Direct interface with TTL levels (2.7 V to 3.6 V)
- Power-down mode
- Complies with JEDEC standards:
 - ◆ JESD8-5 (2.3 V to 2.7 V)
 - ◆ JESD8B/JESD36 (2.7 V to 3.6 V)
 - ◆ JESD8-1A (4.5 V to 5.5 V)
- ESD protection:
 - ◆ MIL-STD-833, method 3015 exceeds 2000 V
 - ◆ HBM JESD22-A114F exceeds 2000 V
 - ◆ MM JESD22-A115-A exceeds 200 V ($C = 200 \text{ pF}$, $R = 0 \Omega$)

nexperia

3. Ordering information

Table 1. Ordering information

Type number	Package			
	Temperature range	Name	Description	Version
74LV165AD-Q100	−40 °C to +85 °C	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1
74LV165APW-Q100	−40 °C to +85 °C	TSSOP16	plastic thin shrink small outline package; 16 leads; body width 4.4 mm	SOT403-1

4. Functional diagram

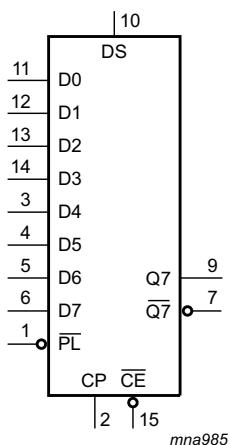


Fig 1. Logic symbol

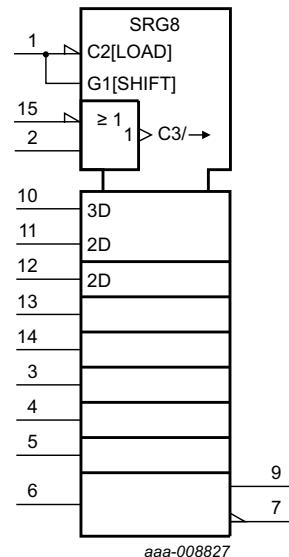


Fig 2. IEC logic symbol

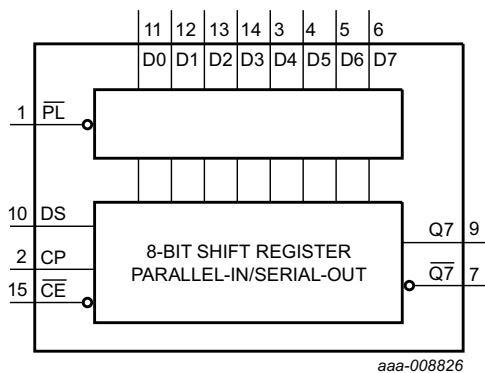


Fig 3. Functional diagram

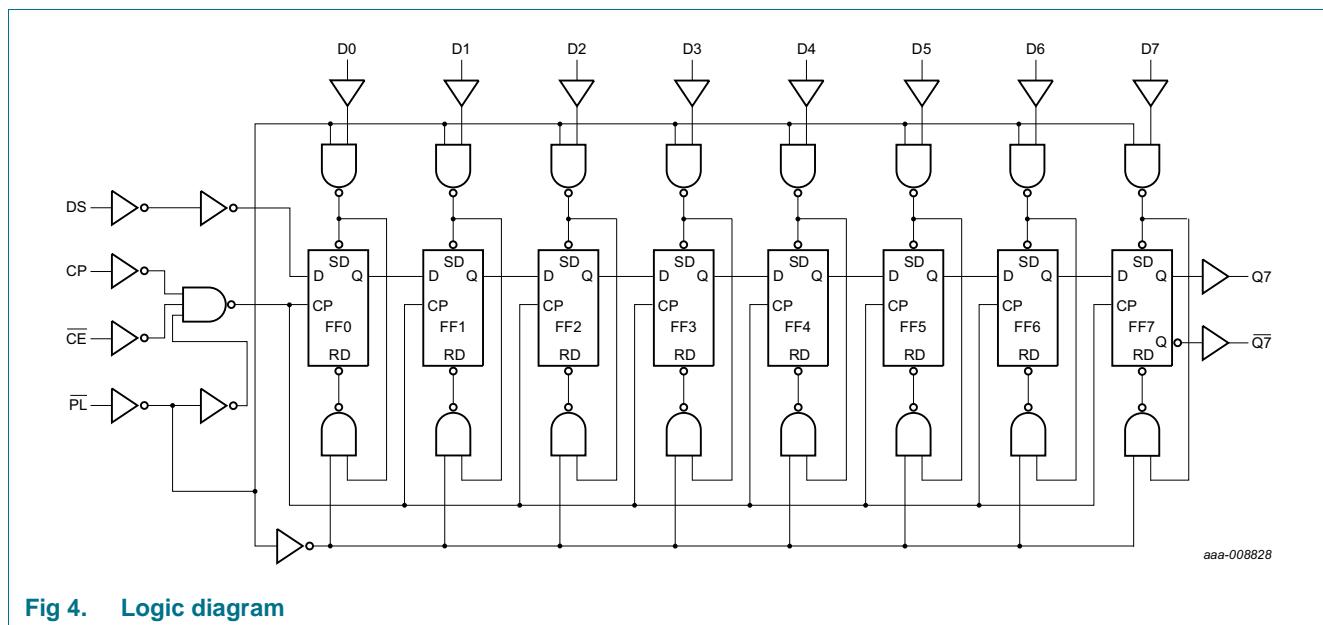


Fig 4. Logic diagram

5. Pinning information

5.1 Pinning

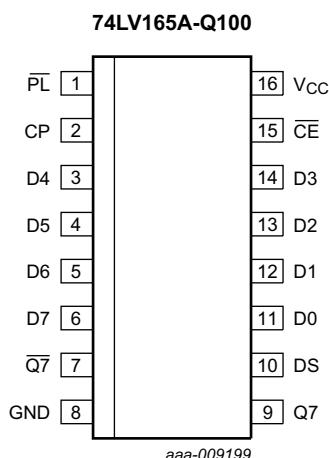


Fig 5. Pin configuration (SO16 and TSSOP16)

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
PL	1	parallel enable input (active LOW)
CP	2	clock input (LOW-to-HIGH edge-triggered)
Q7	7	complementary serial output from the last stage
GND	8	ground (0 V)
Q7	9	serial output from the last stage
DS	10	serial data input
D0 to D7	11, 12, 13, 14, 3, 4, 5, 6	parallel data inputs
CE	15	clock enable input (active LOW)
V _{CC}	16	positive supply voltage

6. Functional description

Table 3. Function table^[1]

Operating modes	Inputs					Qn registers		Output	
	PL	CE	CP	DS	D0 to D7	Q0	Q1 to Q6	Q7	Q̄7
parallel load	L	X	X	X	L	L	L to L	L	H
	L	X	X	X	H	H	H to H	H	L
serial shift	H	L	↑	I	X	L	q0 to q5	q6	q̄6
	H	L	↑	h	X	H	q0 to q5	q6	q̄6
	H	↑	L	I	X	L	q0 to q5	q6	q̄6
	H	↑	L	h	X	H	q0 to q5	q6	q̄6
hold "do nothing"	H	H	X	X	X	q0	q1 to q6	q7	q̄7
	H	X	H	X	X	q0	q1 to q6	q7	q̄7

[1] H = HIGH voltage level;

h = HIGH voltage level one set-up time prior to the LOW-to-HIGH clock transition;

L = LOW voltage level;

I = LOW voltage level one set-up time prior to the LOW-to-HIGH clock transition;

q = state of the referenced output one set-up time prior to the LOW-to-HIGH clock transition;

X = don't care;

↑ = LOW-to-HIGH clock transition.

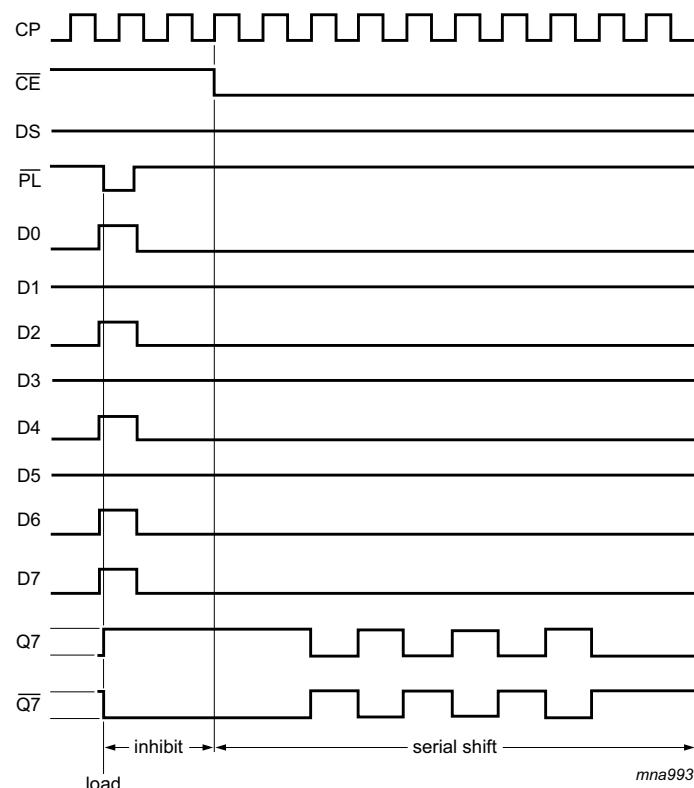


Fig 6. Timing diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V)^[1]

Symbol	Parameter	Conditions	Min	Max	Unit
V _{CC}	supply voltage		-0.5	+7	V
I _{IK}	input clamping current	V _I < 0 V	-	-20	mA
V _I	input voltage		-0.5	+7	V
I _{OK}	output clamping current	V _O > V _{CC} or V _O < 0	-	±50	mA
V _O	output voltage		-0.5	V _{CC} + 0.5	V
		power-down mode	-0.5	+7	V
I _O	output current	0 V < V _O < V _{CC}	-	±25	mA
I _{CC}	supply current		-	+50	mA
I _{GND}	ground current		-50	-	mA
T _{stg}	storage temperature		-65	+150	°C
P _{tot}	total power dissipation	T _{amb} = -40 °C to +85 °C			
		SO16 package	^[2] -	500	mW
		TSSOP16 package	^[3] -	500	mW

[1] The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

[2] P_{tot} derates linearly with 8 mW/K above 70 °C.

[3] P_{tot} derates linearly with 5.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V _{CC}	supply voltage		2.0	-	5.5	V
V _I	input voltage		0	-	5.5	V
V _O	output voltage		0	-	V _{CC}	V
T _{amb}	ambient temperature		-40	-	+85	°C
Δt/ΔV	input transition rise and fall rate	V _{CC} = 2.3 V to 2.7 V	0	-	200	ns/V
		V _{CC} = 3.0 V to 3.6 V	0	-	100	ns/V
		V _{CC} = 4.5 V to 5.5 V	0	-	20	ns/V

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

Symbol	Parameter	Conditions	T _{amb} = -40 °C to +85 °C			Unit
			Min	Typ	Max	
V _{IH}	HIGH-level input voltage	V _{CC} = 2.0 V	1.5	-	-	V
		V _{CC} = 2.3 V to 2.7 V	0.7V _{CC}	-	-	V
		V _{CC} = 3.0 V to 3.6 V	0.7V _{CC}	-	-	V
		V _{CC} = 4.5 V to 5.5 V	0.7V _{CC}	-	-	V
V _{IL}	LOW-level input voltage	V _{CC} = 2.0 V	-	-	0.5	V
		V _{CC} = 2.3 V to 2.7 V	-	-	0.3V _{CC}	V
		V _{CC} = 3.0 V to 3.6 V	-	-	0.3V _{CC}	V
		V _{CC} = 4.5 V to 5.5 V	-	-	0.3V _{CC}	V
V _{OH}	HIGH-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = -50 µA; V _{CC} = 2.0 V to 5.5 V	V _{CC} - 0.1	-	-	V
		I _O = -2.0 mA; V _{CC} = 2.3 V	2.0	-	-	V
		I _O = -6.0 mA; V _{CC} = 3.0 V	2.48	-	-	V
		I _O = -12 mA; V _{CC} = 4.5 V	3.8	-	-	V
V _{OL}	LOW-level output voltage	V _I = V _{IH} or V _{IL}				
		I _O = 50 µA; V _{CC} = 2.0 V to 5.5 V	-	-	0.10	V
		I _O = 2.0 mA; V _{CC} = 2.3 V	-	-	0.40	V
		I _O = 6.0 mA; V _{CC} = 3.0 V	-	-	0.44	V
		I _O = 12 mA; V _{CC} = 4.5 V	-	-	0.55	V
I _I	input leakage current	V _I = V _{CC} or GND; V _{CC} = 5.5 V	-	±0.01	±1	µA
I _{OFF}	power-off leakage current	V _I or V _O = 5.5 V; V _{CC} = 0.0 V	-	±0.05	±5	µA
I _{CC}	supply current	V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V	-	0.2	20	µA
C _I	input capacitance		-	3.0	-	pF

10. Dynamic characteristics

Table 7. Dynamic characteristics

GND (ground = 0 V); for test circuit, see [Figure 12](#)

Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
			Min	Typ ^[1]	Max	
t_{pd}	propagation delay	\overline{CE} , CP to Q7, $\overline{Q7}$; $C_L = 15 \text{ pF}$; see Figure 7 [2] and Figure 8				
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	[3]	1.0	11.0	22.0
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	[4]	1.0	7.5	18.0
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	[5]	1.0	5.5	11.5
		\overline{PL} to Q7, $\overline{Q7}$; $C_L = 15 \text{ pF}$; see Figure 8				
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	[3]	1.0	11.5	23.5
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	[4]	1.0	8.0	18.5
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	[5]	1.0	5.5	11.5
		D7 to Q7, $\overline{Q7}$; $C_L = 15 \text{ pF}$; see Figure 9				
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	[3]	1.0	12.0	24.0
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	[4]	1.0	8.5	16.5
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	[5]	1.0	6.0	10.5
		\overline{CE} , CP to Q7, $\overline{Q7}$; see Figure 7 and Figure 8				
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	[3]	1.0	13.0	26.0
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	[4]	1.0	9.0	21.5
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	[5]	1.0	6.1	13.5
		\overline{PL} to Q7, $\overline{Q7}$; see Figure 8				
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	[3]	1.0	14.0	28.0
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	[4]	1.0	10.0	22.0
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	[5]	1.0	6.5	13.5
		D7 to Q7, $\overline{Q7}$; see Figure 9				
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	[3]	1.0	14.0	28.0
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	[4]	1.0	10.0	20
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	[5]	1.0	6.5	12.5
t_w	pulse width	CP input HIGH to LOW; see Figure 7				
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	[3]	9.0	-	-
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	[4]	7.0	-	-
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	[5]	4.0	-	-
		\overline{PL} input LOW; see Figure 8				
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	[3]	13.0	-	-
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	[4]	9.0	-	-
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	[5]	6.0	-	-
t_{rec}	recovery time	\overline{PL} to CP, \overline{CE} ; see Figure 8				
		$V_{CC} = 2.3 \text{ V}$ to 2.7 V	[3]	8.5	-	-
		$V_{CC} = 3.0 \text{ V}$ to 3.6 V	[4]	6.0	-	-
		$V_{CC} = 4.5 \text{ V}$ to 5.5 V	[5]	4.0	-	-

Table 7. Dynamic characteristics ...continued
GND (ground = 0 V); for test circuit, see [Figure 12](#)

Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit
			Min	Typ ^[1]	Max	
t_{su}	set-up time	DS to CP, \overline{CE} ; see Figure 10				
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	[3]	6.0	-	-
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	[4]	4.0	-	-
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	[5]	7.0	-	-
		\overline{CE} to CP, CP to \overline{CE} ; see Figure 10				
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	[3]	7.0	-	-
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	[4]	5.0	-	-
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	[5]	3.5	-	-
		D7 to \overline{PL} ; see Figure 11				
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	[3]	12	-	-
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	[4]	8.5	-	-
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	[5]	5.0	-	-
t_h	hold time	DS to CP, \overline{CE} ; \overline{PL} to CP, \overline{CE} ; see Figure 10				
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	[3]	0	-	-
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	[4]	0	-	-
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	[5]	0.5	-	-
		Dn to \overline{PL} ; see Figure 11				
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	[3]	0.5	-	-
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	[4]	0.5	-	-
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	[5]	1.0	-	-
f_{max}	maximum frequency	CP input; $C_L = 15\text{ pF}$; see Figure 7				
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	[3]	45	80	-
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	[4]	50	115	-
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	[5]	90	165	-
		CP input; see Figure 7				
		$V_{CC} = 2.3\text{ V}$ to 2.7 V	[3]	35	65	-
		$V_{CC} = 3.0\text{ V}$ to 3.6 V	[4]	50	90	-
		$V_{CC} = 4.5\text{ V}$ to 5.5 V	[5]	85	125	-

Table 7. Dynamic characteristics ...continued
GND (ground = 0 V); for test circuit, see [Figure 12](#)

Symbol	Parameter	Conditions	$T_{amb} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$			Unit	
			Min	Typ ^[1]	Max		
C_{PD}	power dissipation capacitance	$V_I = \text{GND}$ to V_{CC} ; $V_{CC} = 3.3\text{ V}$	[6]	-	24	-	pF

[1] Typical values are measured at $T_{amb} = 25^{\circ}\text{C}$ and nominal V_{CC} .

[2] t_{pd} is the same as t_{PHL} and t_{PLH} .

[3] Typical values are measured at $V_{CC} = 2.5\text{ V}$.

[4] Typical values are measured at $V_{CC} = 3.3\text{ V}$.

[5] Typical values are measured at $V_{CC} = 5.0\text{ V}$.

[6] C_{PD} is used to determine the dynamic power dissipation $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ (P_D in μW), where:

f_i = input frequency in MHz;

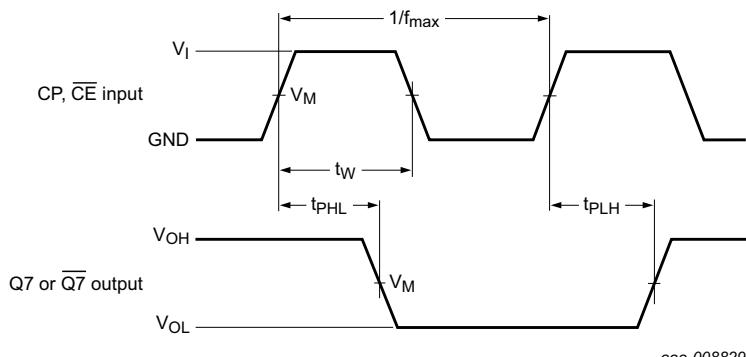
f_o = output frequency in MHz;

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs;

C_L = output load capacitance in pF;

V_{CC} = supply voltage in V.

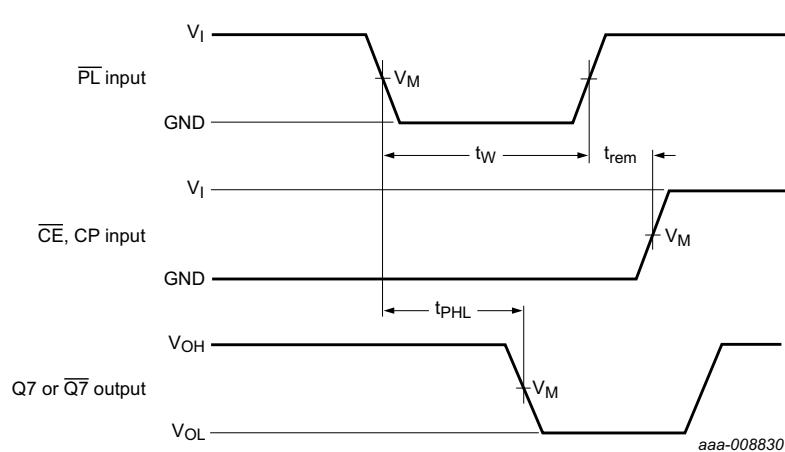
11. Waveforms



Measurement points are given in [Table 8](#).

The changing to output assumes that internal Q6 is opposite state from Q7.

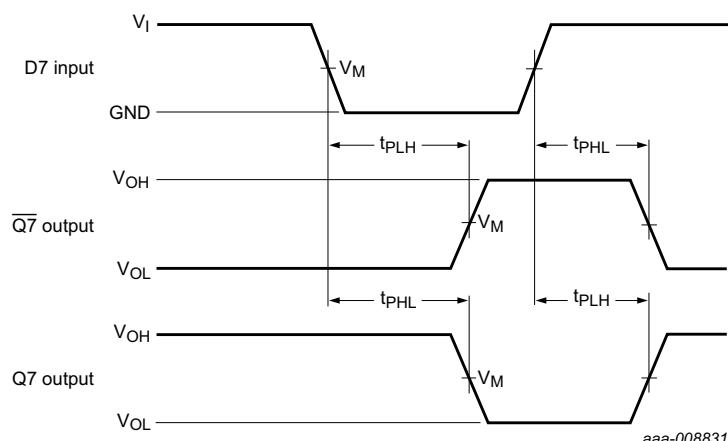
Fig 7. Clock pulse (CP) and clock enable (CE) to output (Q7 or $\overline{Q7}$) propagation delays, clock pulse width and maximum clock frequency



Measurement points are given in [Table 8](#).

The changing to output assumes that internal Q6 is opposite state from Q7.

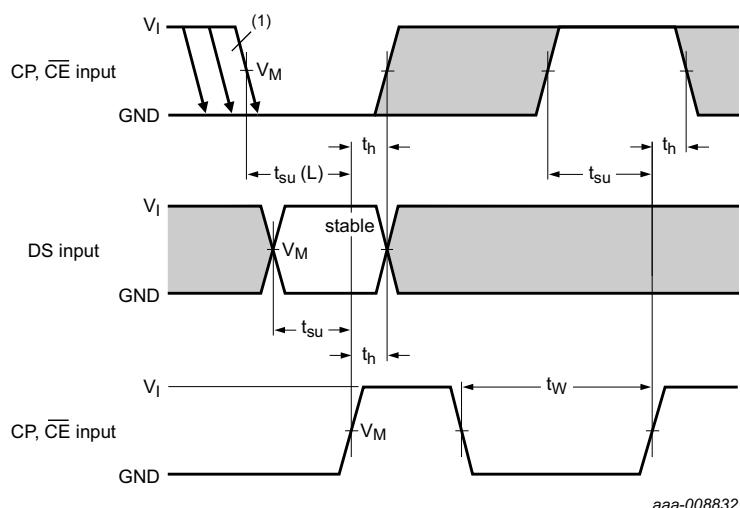
Fig 8. Parallel load (PL) pulse width, parallel load to output (Q7 or $\overline{Q7}$) propagation delays, parallel load to clock (CP) and clock enable (CE) recovery time



Measurement points are given in [Table 8](#).

The changing to output assumes that internal Q6 is opposite state from Q7.

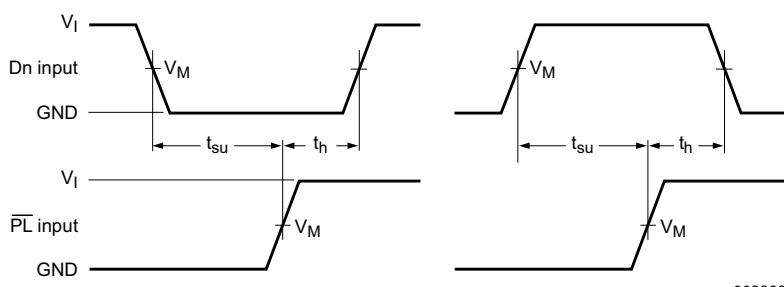
Fig 9. Data input (D7) to output (Q7 or $\overline{Q7}$) propagation delays when PL is LOW



Measurement points are given in [Table 8](#).

(1) CE may change only from HIGH-to-LOW while CP is LOW. The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 10. Set-up and hold times

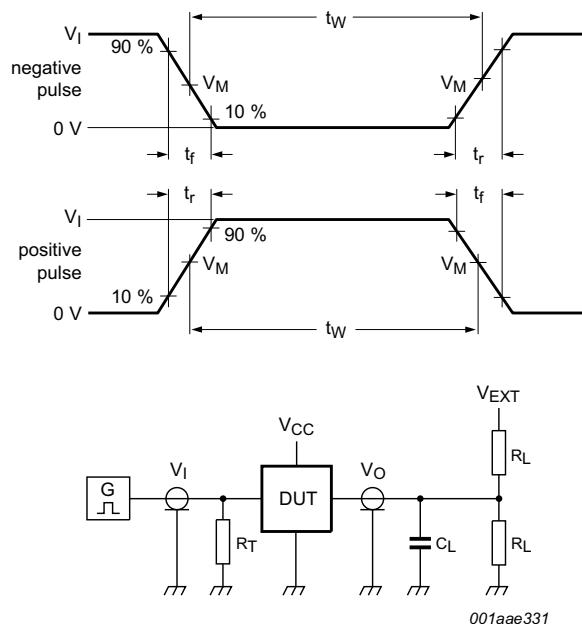


Measurement points are given in [Table 8](#).

Fig 11. Set-up and hold times from the data inputs (Dn) to the parallel load input (PL)

Table 8. Measurement points

Supply voltage	Input	Output
V_{CC}	V_M	V_M
2.0 V to 5.5 V	$0.5V_{CC}$	$0.5V_{CC}$



Test data is given in [Table 9](#).

Definitions for test circuit:

R_L = Load resistance.

C_L = Load capacitance including jig and probe capacitance.

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

V_{EXT} = External voltage for measuring switching times.

Fig 12. Test circuit for measuring switching times

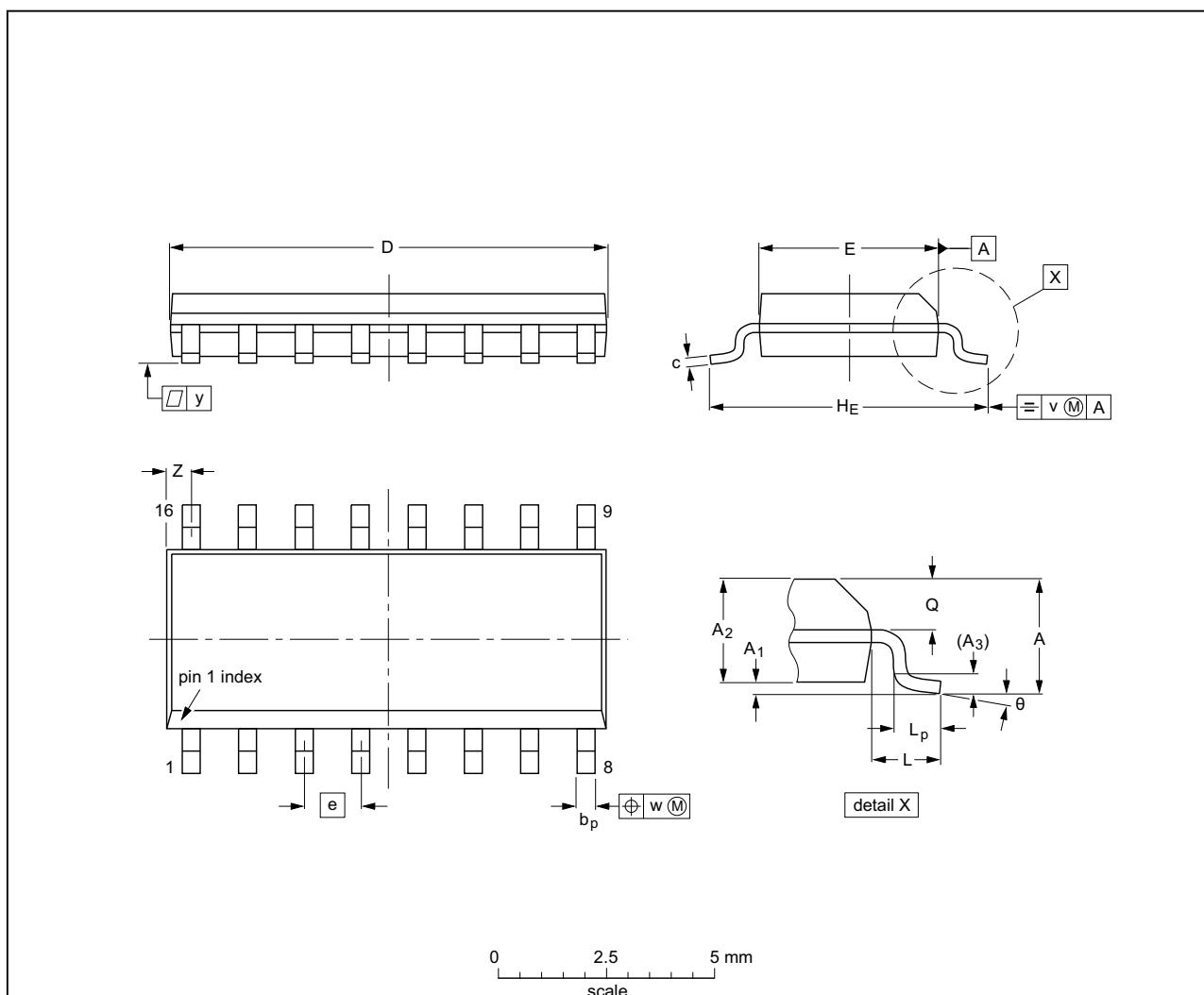
Table 9. Test data

Supply voltage	Input		Load		V_{EXT}
	V_I	t_r, t_f	C_L	R_L	
2.0 V to 5.5 V	V_{CC}	3.0 ns	50 pF, 15 pF	1 k Ω	open

12. Package outline

SO16: plastic small outline package; 16 leads; body width 3.9 mm

SOT109-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A ₁	A ₂	A ₃	b _p	c	D ⁽¹⁾	E ⁽¹⁾	e	H _E	L	L _p	Q	v	w	y	z ⁽¹⁾	θ
mm	1.75 0.10	0.25 1.25	1.45	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8°
inches	0.069 0.004	0.010 0.049	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	0°

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				99-12-27 03-02-19

Fig 13. Package outline SOT109-1 (SO16)

TSSOP16: plastic thin shrink small outline package; 16 leads; body width 4.4 mm

SOT403-1

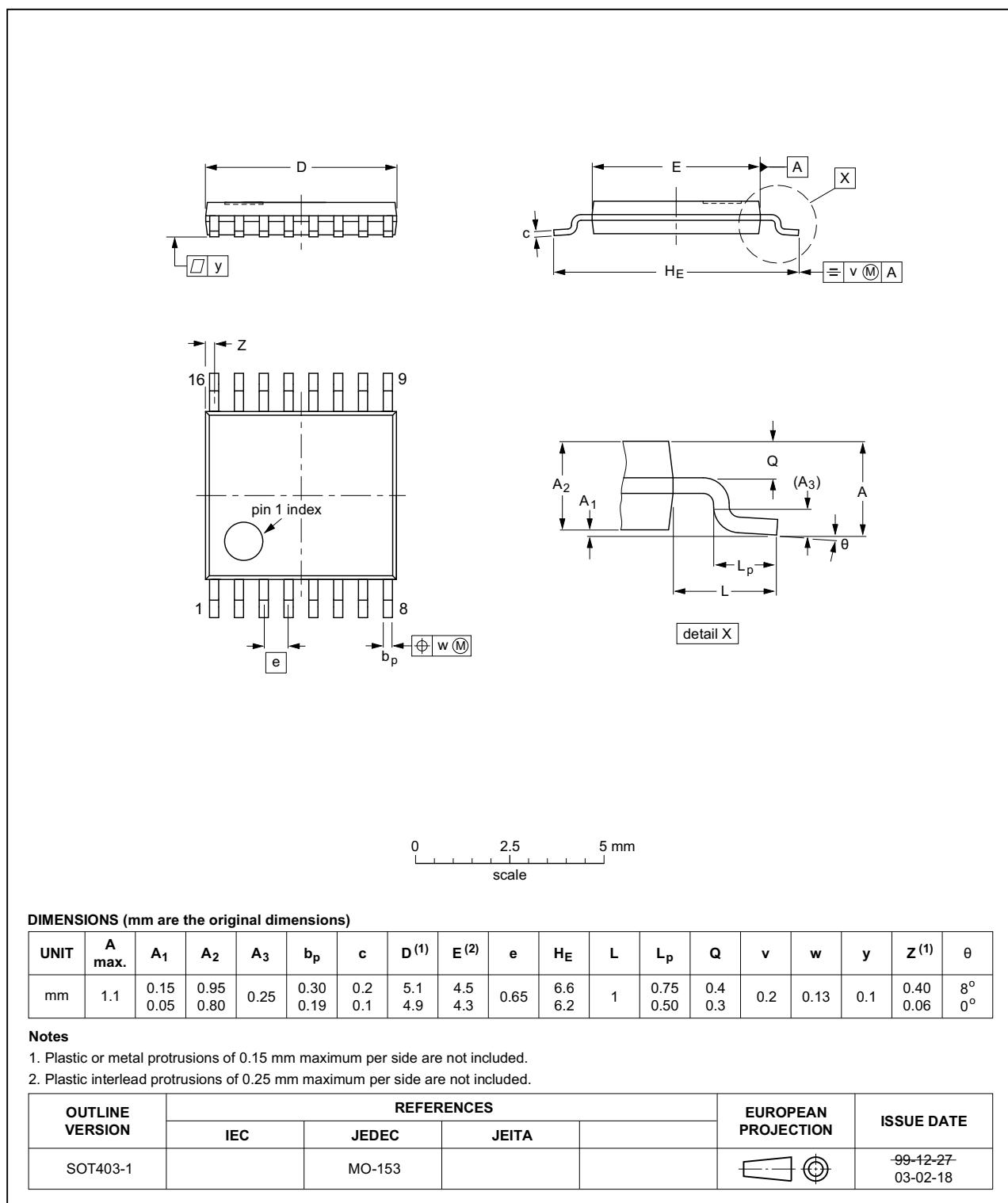


Fig 14. Package outline SOT403-1 (TSSOP16)

13. Abbreviations

Table 10. Abbreviations

Acronym	Description
CMOS	Complementary Metal-Oxide Semiconductor
DUT	Device Under Test
ESD	ElectroStatic Discharge
HBM	Human Body Model
MIL	Military
MM	Machine Model
TTL	Transistor-Transistor Logic

14. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
74LV165A_Q100 v.3	20140328	Product data sheet	-	74LV165A_Q100 v.2
Modifications:	<ul style="list-style-type: none">Minimum limit V_{OH} for $V_{CC} = 4.5$ V corrected from 3.0 V to 3.8 V (errata) in Table 6 "Static characteristics"			
74LV165A_Q100 v.2	20140219	Product data sheet	-	74LV165A_Q100 v.1
Modifications:	<ul style="list-style-type: none">Typo corrected in Table 2 "Pin description"			
74LV165A_Q100 v.1	20131021	Product data sheet	-	-

15. Legal information

15.1 Data sheet status

Document status ^{[1][2]}	Product status ^[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nexperia.com>.

15.2 Definitions

Draft — The document is a draft version only. The content is still under internal review and subject to formal approval, which may result in modifications or additions. Nexperia does not give any representations or warranties as to the accuracy or completeness of information included herein and shall have no liability for the consequences of use of such information.

Short data sheet — A short data sheet is an extract from a full data sheet with the same product type number(s) and title. A short data sheet is intended for quick reference only and should not be relied upon to contain detailed and full information. For detailed and full information see the relevant full data sheet, which is available on request via the local Nexperia sales office. In case of any inconsistency or conflict with the short data sheet, the full data sheet shall prevail.

Product specification — The information and data provided in a Product data sheet shall define the specification of the product as agreed between Nexperia and its customer, unless Nexperia and customer have explicitly agreed otherwise in writing. In no event however, shall an agreement be valid in which the Nexperia product is deemed to offer functions and qualities beyond those described in the Product data sheet.

Suitability for use in automotive applications — This Nexperia product has been qualified for use in automotive applications. Unless otherwise agreed in writing, the product is not designed, authorized or warranted to be suitable for use in life support, life-critical or safety-critical systems or equipment, nor in applications where failure or malfunction of a Nexperia product can reasonably be expected to result in personal injury, death or severe property or environmental damage. Nexperia and its suppliers accept no liability for inclusion and/or use of Nexperia products in such equipment or applications and therefore such inclusion and/or use is at the customer's own risk.

Applications — Applications that are described herein for any of these products are for illustrative purposes only. Nexperia makes no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

Customers are responsible for the design and operation of their applications and products using Nexperia products, and Nexperia accepts no liability for any assistance with applications or customer product design. It is customer's sole responsibility to determine whether the Nexperia product is suitable and fit for the customer's applications and products planned, as well as for the planned application and use of customer's third party customer(s). Customers should provide appropriate design and operating safeguards to minimize the risks associated with their applications and products.

Nexperia does not accept any liability related to any default, damage, costs or problem which is based on any weakness or default in the customer's applications or products, or the application or use by customer's third party customer(s). Customer is responsible for doing all necessary testing for the customer's applications and products using Nexperia products in order to avoid a default of the applications and the products or of the application or use by customer's third party customer(s). Nexperia does not accept any liability in this respect.

Limiting values — Stress above one or more limiting values (as defined in the Absolute Maximum Ratings System of IEC 60134) will cause permanent damage to the device. Limiting values are stress ratings only and (proper) operation of the device at these or any other conditions above those given in the Recommended operating conditions section (if present) or the Characteristics sections of this document is not warranted. Constant or repeated exposure to limiting values will permanently and irreversibly affect the quality and reliability of the device.

Terms and conditions of commercial sale — Nexperia products are sold subject to the general terms and conditions of commercial sale, as published at <http://www.nexperia.com/profile/terms>, unless otherwise agreed in a valid written individual agreement. In case an individual agreement is concluded only the terms and conditions of the respective agreement shall apply. Nexperia hereby expressly objects to applying the customer's general terms and conditions with regard to the purchase of Nexperia products by customer.

15.3 Disclaimers

Limited warranty and liability — Information in this document is believed to be accurate and reliable. However, Nexperia does not give any representations or warranties, expressed or implied, as to the accuracy or completeness of such information and shall have no liability for the consequences of use of such information. Nexperia takes no responsibility for the content in this document if provided by an information source outside of Nexperia.

In no event shall Nexperia be liable for any indirect, incidental, punitive, special or consequential damages (including - without limitation - lost profits, lost savings, business interruption, costs related to the removal or replacement of any products or rework charges) whether or not such damages are based on tort (including negligence), warranty, breach of contract or any other legal theory.

Notwithstanding any damages that customer might incur for any reason whatsoever, Nexperia's aggregate and cumulative liability towards customer for the products described herein shall be limited in accordance with the *Terms and conditions of commercial sale* of Nexperia.

Right to make changes — Nexperia reserves the right to make changes to information published in this document, including without limitation specifications and product descriptions, at any time and without notice. This document supersedes and replaces all information supplied prior to the publication hereof.

No offer to sell or license — Nothing in this document may be interpreted or construed as an offer to sell products that is open for acceptance or the grant, conveyance or implication of any license under any copyrights, patents or other industrial or intellectual property rights.

Export control — This document as well as the item(s) described herein may be subject to export control regulations. Export might require a prior authorization from competent authorities.

Translations — A non-English (translated) version of a document is for reference only. The English version shall prevail in case of any discrepancy between the translated and English versions.

15.4 Trademarks

Notice: All referenced brands, product names, service names and trademarks are the property of their respective owners.

16. Contact information

For more information, please visit: <http://www.nexperia.com>

For sales office addresses, please send an email to: salesaddresses@nexperia.com

17. Contents

1	General description	1
2	Features and benefits	1
3	Ordering information	2
4	Functional diagram	2
5	Pinning information	4
5.1	Pinning	4
5.2	Pin description	4
6	Functional description	5
7	Limiting values	6
8	Recommended operating conditions	6
9	Static characteristics	7
10	Dynamic characteristics	8
11	Waveforms	10
12	Package outline	14
13	Abbreviations	16
14	Revision history	16
15	Legal information	17
15.1	Data sheet status	17
15.2	Definitions.....	17
15.3	Disclaimers.....	17
15.4	Trademarks.....	18
16	Contact information	18
17	Contents	19

Mouser Electronics

Authorized Distributor

Click to View Pricing, Inventory, Delivery & Lifecycle Information:

NXP:

[74LV165AD-Q100J](#) [74LV165APW-Q100J](#)