



## STS25NH3LL

N-channel 30 V - 0.0032  $\Omega$  - 25 A - SO-8  
STripFET™ III Power MOSFET for DC/DC conversion

### Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STS25NH3LL	30 V	<0.0035 $\Omega$	25 A <sup>(1)</sup>

1. This value is rated according to R<sub>thj-pcb</sub>

- Optimal R<sub>DS(on)</sub> x Q<sub>g</sub> trade off @ 4.5 V
- Conduction losses reduced
- Switching losses reduced

### Applications

- Switching applications

### Description

This device utilizes the advanced design rules of ST's proprietary STripFET™ technology. The innovative process coupled with unique metallization techniques makes it possible to produce the most advanced low voltage Power MOSFET in an SO-8 package. The device is therefore suitable for demanding DC-DC converter applications where high efficiency at high output current is needed.

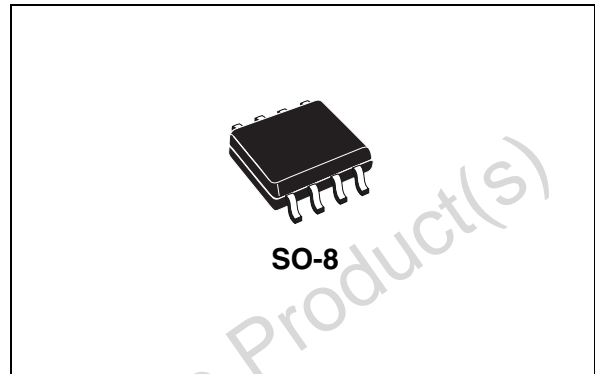


Figure 1. Internal schematic diagram

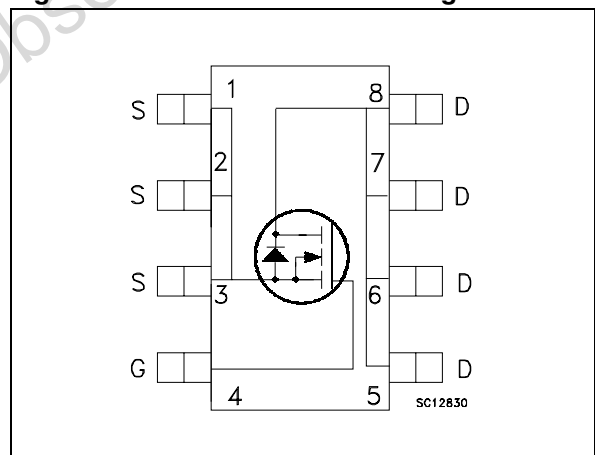


Table 1. Device summary

Order code	Marking	Package	Packaging
STS25NH3LL	25H3LL	SO-8	Tape & reel

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS} = 0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 18$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	25	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	18	A
$I_{DM}^{(2)}$	Drain current (pulsed)	100	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	3.2	W

1. This value is rated according to  $R_{thj-pcb}$
2. Pulse width limited by safe operating area

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-amb max	47	$^\circ\text{C}/\text{W}$
$T_j$ $T_{stg}$	Operation junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu,  $t < 10$  sec

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AV}$	Not-repetitive avalanche current (pulse width limited by $T_j$ max.)	12.5	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AV}$ , $V_{DD} = 24\text{ V}$ )	1.3	J

## 2 Electrical characteristics

( $T_{CASE}=25^{\circ}\text{C}$  unless otherwise specified)

**Table 5. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = \text{Max rating}$ , $V_{DS} = \text{Max rating @ } 125^{\circ}\text{C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 18\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	1			V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 12.5\text{ A}$ $V_{GS} = 4.5\text{ V}$ , $I_D = 12.5\text{ A}$		0.0032 0.004	0.0035 0.005	$\Omega$ $\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$g_{fs}^{(1)}$	Forward transconductance	$V_{DS} = 10\text{ V}$ , $I_D = 12.5\text{ A}$		30		S
$C_{iss}$ $C_{oss}$ $C_{rss}$	Input capacitance Output capacitance Reverse transfer capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$		4450 655 50		pF pF pF
$Q_g$ $Q_{gs}$ $Q_{gd}$	Total gate charge Gate-source charge Gate-drain charge	$V_{DD} = 15\text{ V}$ , $I_D = 25\text{ A}$ $V_{GS} = 4.5\text{ V}$ <a href="#">Figure 14</a>		30 12.5 10	40	nC nC nC
$Q_{OSS}^{(2)}$	Output charge	$V_{DD} = 24\text{ V}$ , $V_{GS} = 0$		23		nC
$R_G$	Gate input resistance	$f = 1\text{ MHz}$ , gate DC bias = 0 test signal level = 20 mV open drain	1	2	3	$\Omega$

1. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

2.  $Q_{OSS} = C_{oss} * \Delta V_{in}$ ,  $C_{oss} = C_{gd} + C_{ds}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 15\text{ V}$ , $I_D = 12.5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ <i>Figure 13</i>		18		ns
$t_r$	Rise time			50		ns
$t_{d(off)}$	Turn-off delay time			75		ns
$t_f$	Fall time			8		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				25	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				100	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 25\text{ A}$ , $V_{GS} = 0$			1.3	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 25\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ , $V_{DD} = 25\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ <i>Figure 18</i>		32		ns
$Q_{rr}$	Reverse recovery charge			34		nC
$I_{RRM}$	Reverse recovery current			2.1		A

1. Pulse width limited by safe operating area
2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

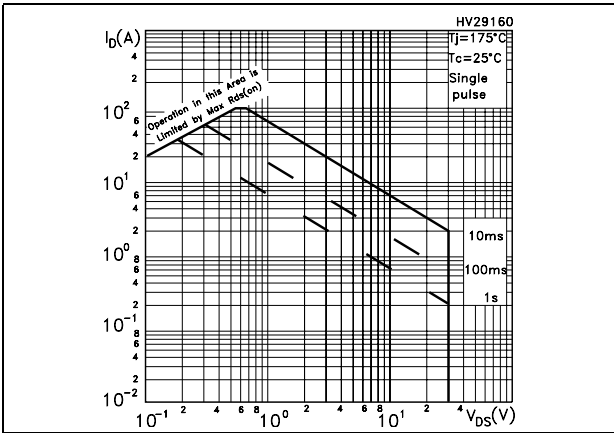


Figure 3. Thermal impedance

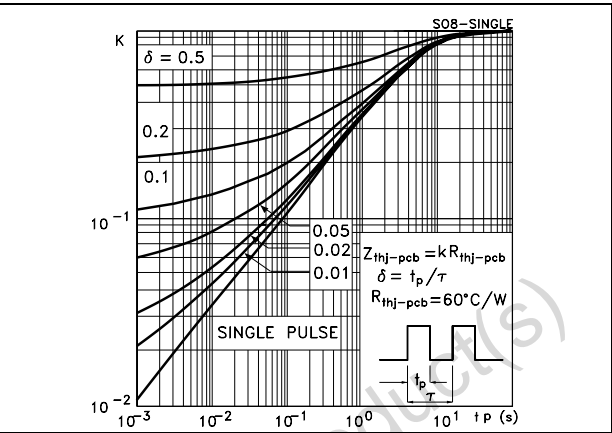


Figure 4. Output characteristics

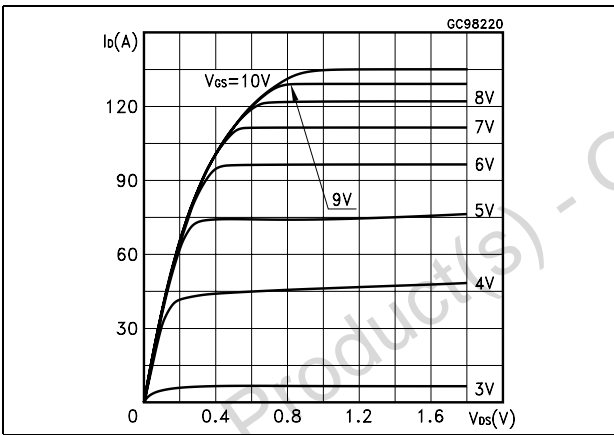


Figure 5. Transfer characteristics

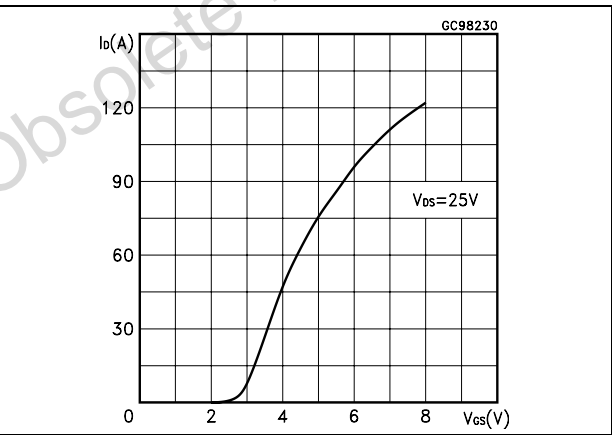


Figure 6. Normalized  $B_{V_{DSS}}$  vs temperature

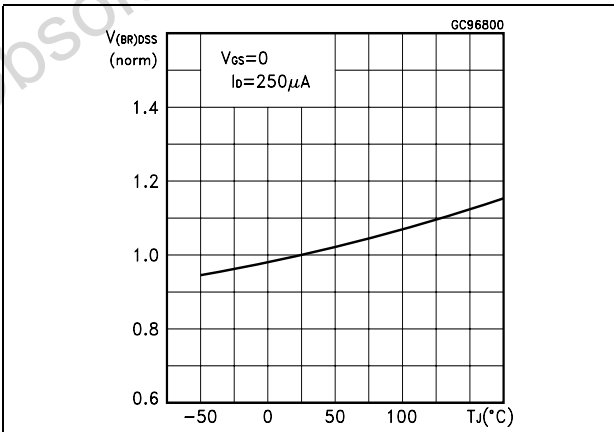


Figure 7. Static drain-source on resistance

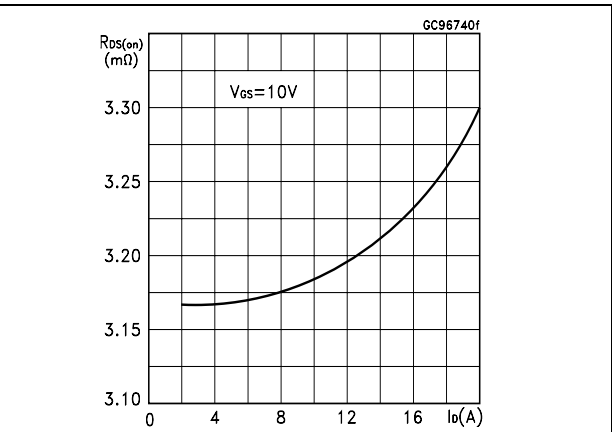


Figure 8. Gate charge vs gate-source voltage    Figure 9. Capacitance variations

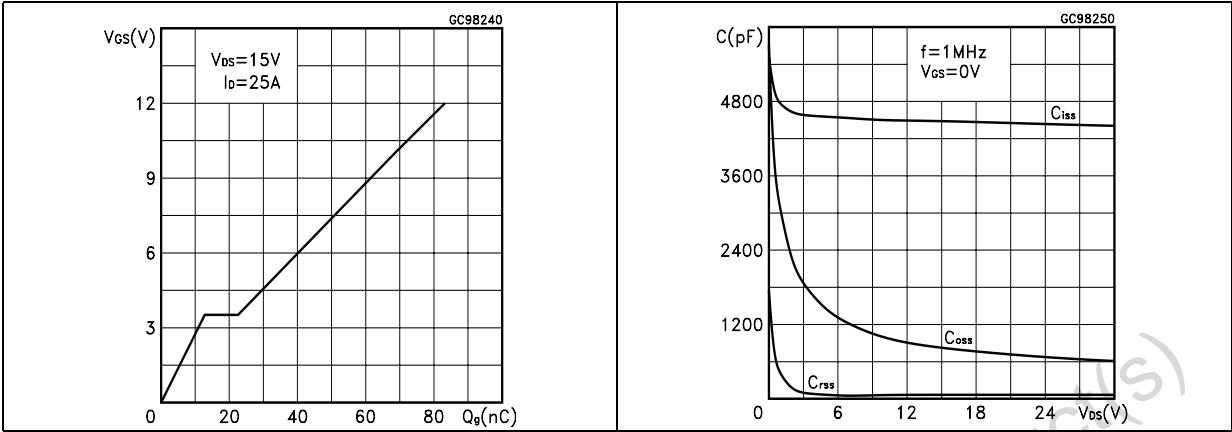


Figure 10. Normalized gate threshold voltage vs temperature    Figure 11. Normalized on resistance vs temperature

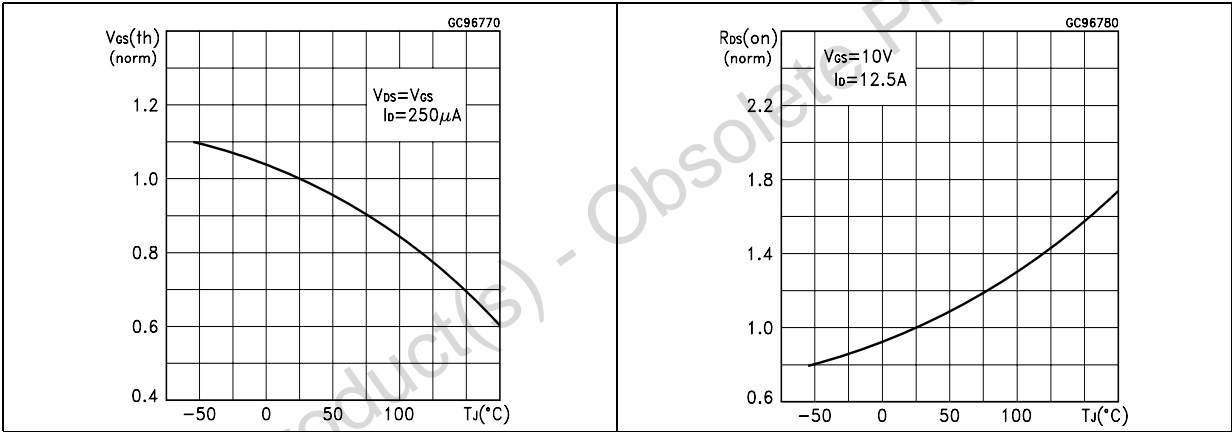
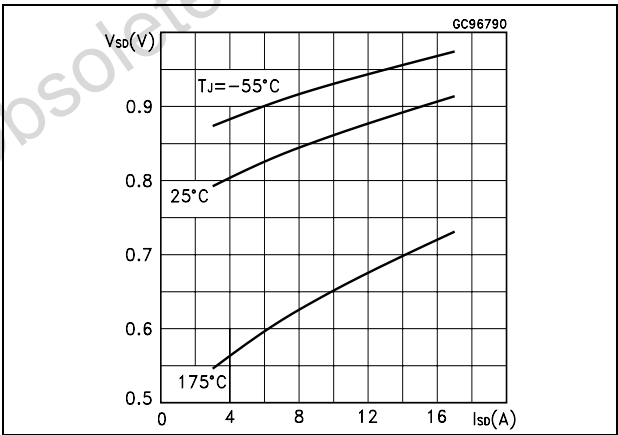


Figure 12. Source-drain diode forward characteristics



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

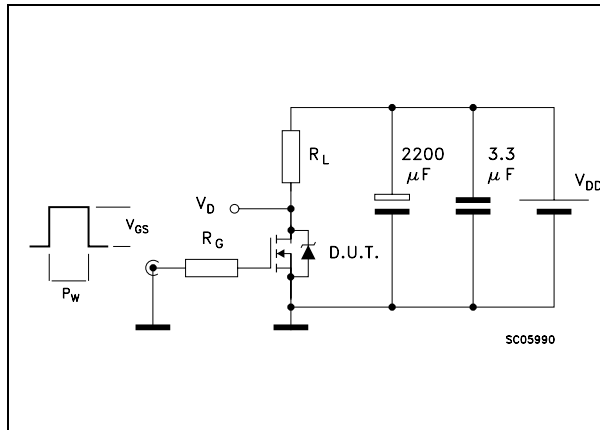


Figure 14. Gate charge test circuit

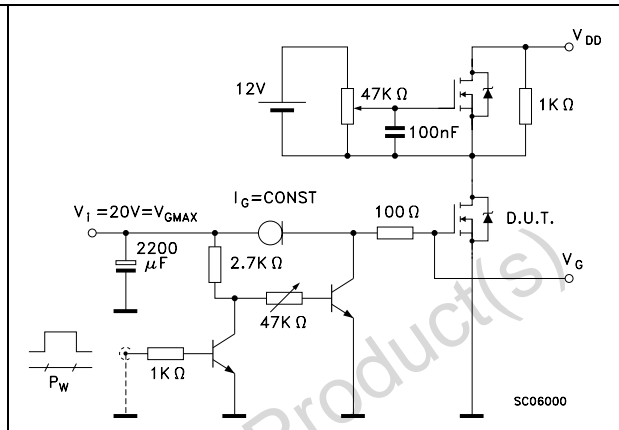


Figure 15. Test circuit for inductive load switching and diode recovery times

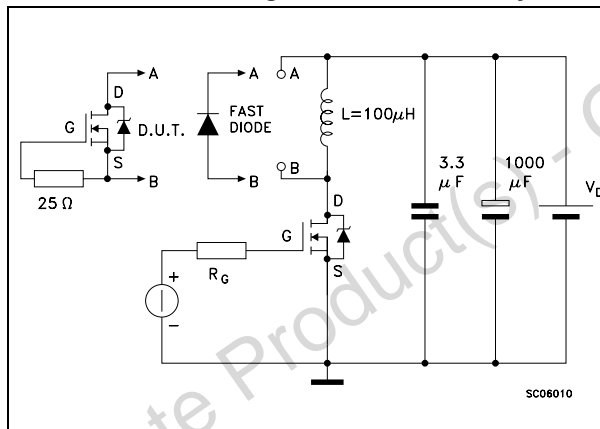


Figure 16. Unclamped inductive load test circuit

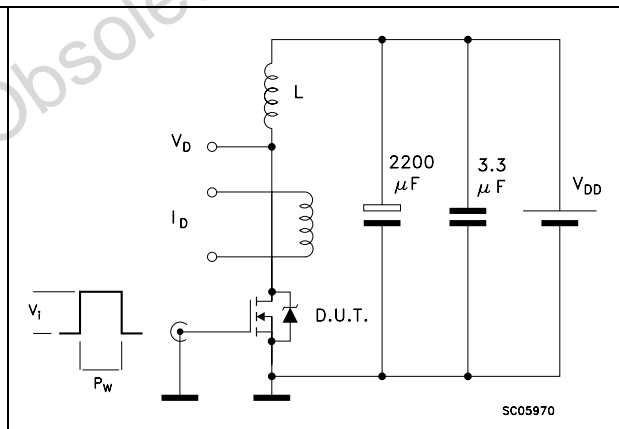


Figure 17. Unclamped inductive waveform

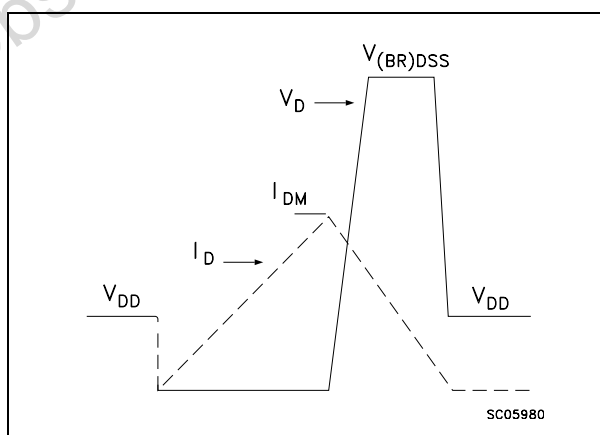
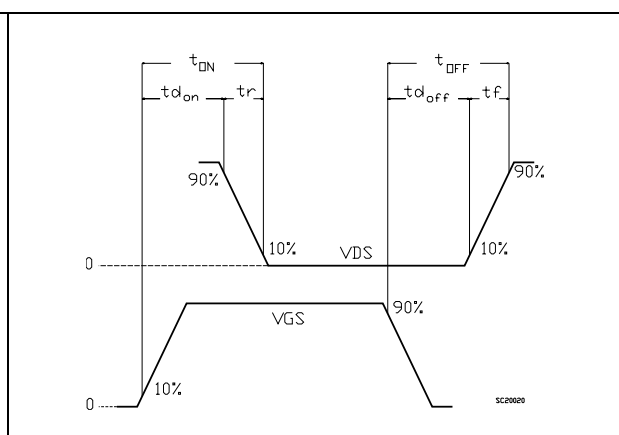


Figure 18. Switching time waveform



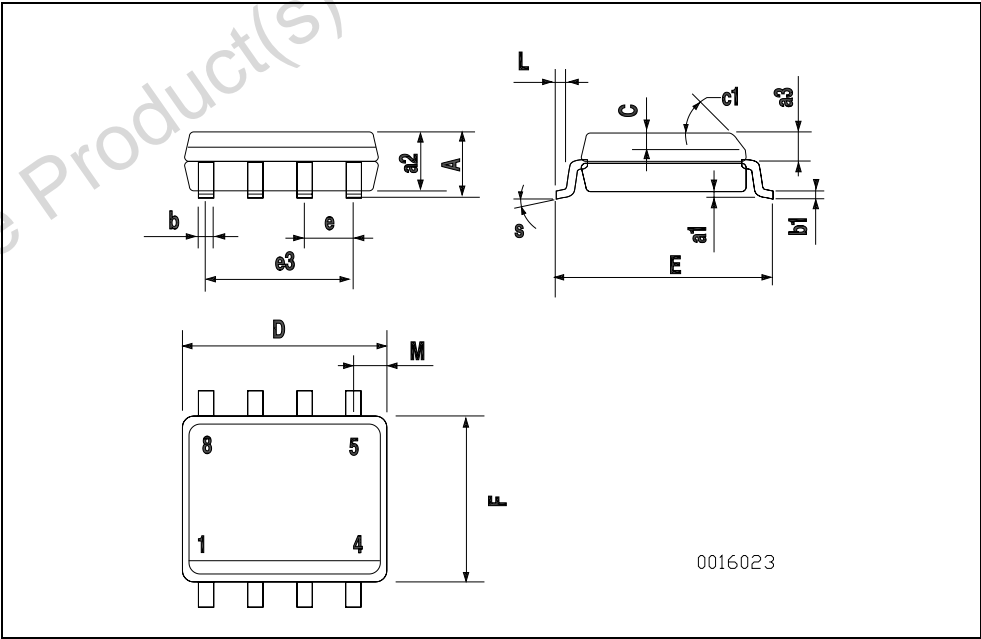
## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

Obsolete Product(s) - Obsolete Product(s)



SO-8 MECHANICAL DATA						
DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



## 5 Revision history

**Table 9. Document revision history**

Date	Revision	Changes
19-Nov-2007	10	Document status promoted from preliminary data to datasheet

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