LM48823

Boomer® Audio Power Amplifier Series

Mono, Bridge-Tied Load, Ceramic Speaker Driver with I^2C Volume Control and Reset

Check for Samples: LM48823, LM48823TLEVAL

FEATURES

- **Integrated Charge Pump**
- **Bridge-Tied Load Output**
- **High PSRR**
- **I^2C Volume and Mode Control**
- **Reset Input**
- **Advanced Click-and-Pop Suppression**
- **Low Supply Current**
- **Minimum External Components**
- **Micro-Power Shutdown**
- **Available in Space-Saving 16-Bump DSBGA Package**

APPLICATIONS

- **Cell Phones**
- **Smart Phones**
- **Portable Media Devices**
- **Notebook PCs**

KEY SPECIFICATIONS

- **Output Voltage at V_{DD} = 4.2V, R_L = 2.2µF + 15Ω THD+N ≤ 1%: 5.4V_{RMS} (typ)**
- **Quiescent Power Supply Current at 4.2V: 3.3mA (typ)**
- **PSRR at 217Hz: 93dB (typ)**
- **Shutdown Current: 0.01µA (typ)**

DESCRIPTION

The LM48823 is a single supply, mono, ceramic speaker driver with an integrated charge-pump, designed for portable devices, such as cell phones, where board space is at a premium. The LM48823 charge pump allows the device to deliver 5.4V_{RMS} from a single 4.2V supply.

The LM48823 features high power supply rejection ratio (PSRR), 93dB at 217Hz, allowing the device to operate in noisy environments without additional power supply conditioning. Flexible power supply requirements allow operation from 2.0V to 4.5V. The LM48823 features an active low reset input that reverts the device to its default state. Additionally, the LM48823 features a 32-step I^2C volume control. The low power Shutdown mode reduces supply current consumption to 0.01µA.

The LM48823's superior click and pop suppression eliminates audible transients on power-up/down and during shutdown. The LM48823 is available in an ultra-small 16-bump DSBGA package (2mmx2mm).

Typical Application

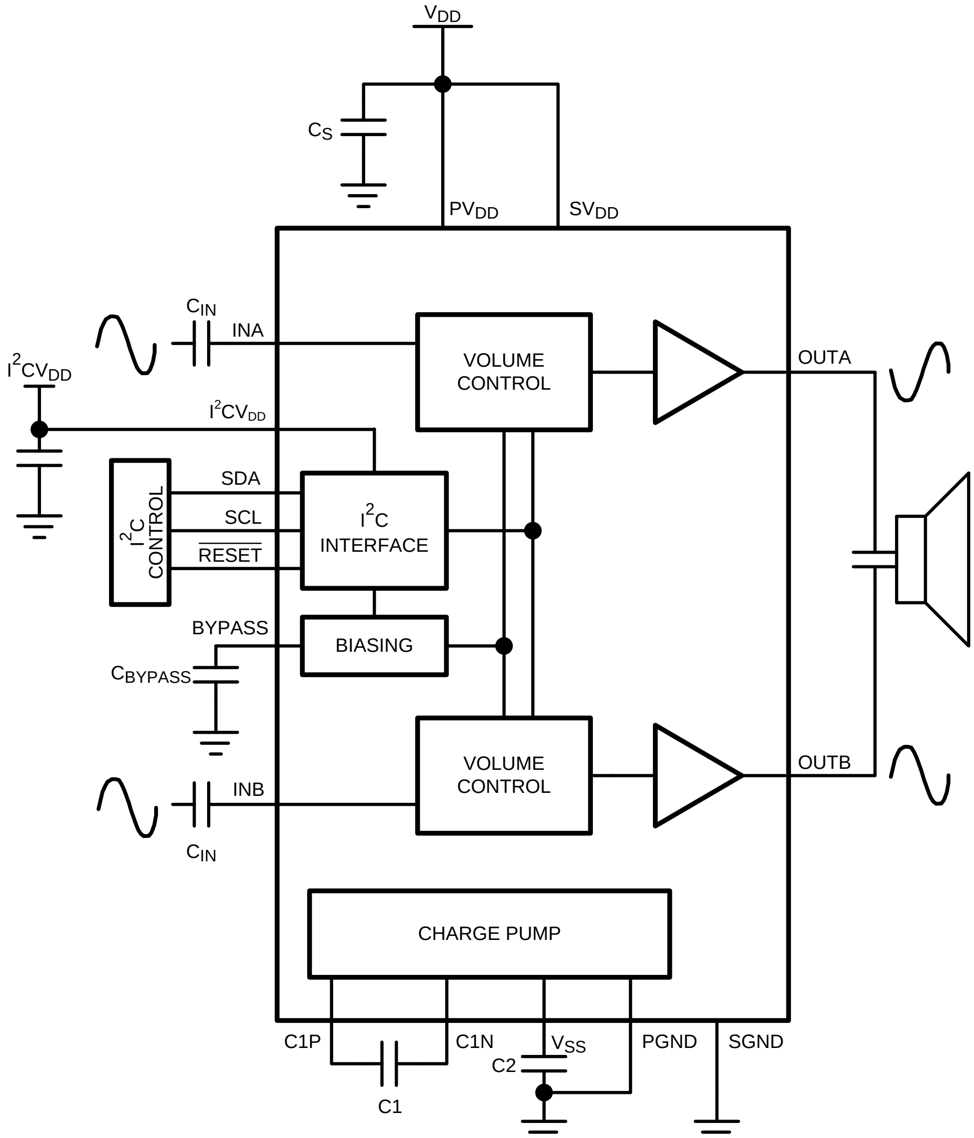

Figure 1. Typical Audio Amplifier Application Circuit

Connection Diagram

YZR Package
2mm x 2mm x 0.8mm

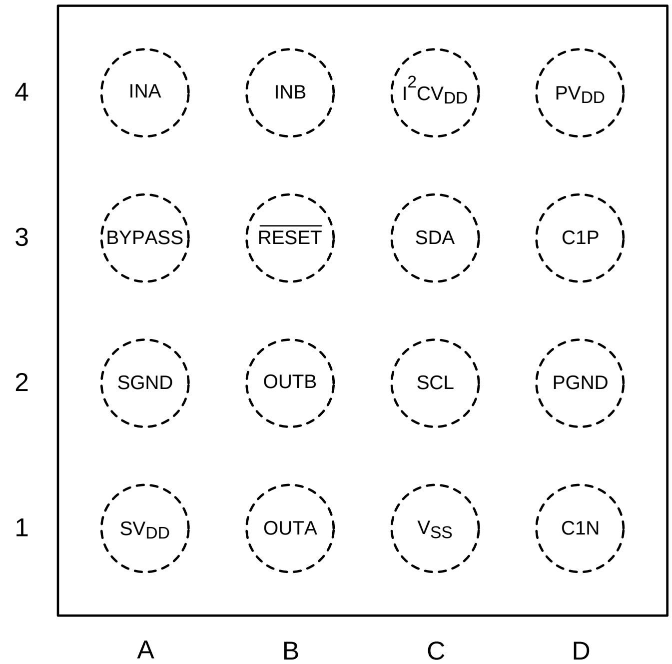

Figure 2. Top View
See Package Number YZR 16

Bump Descriptions

Pin Designator	Pin Name	Pin Function
A1	SV_{DD}	Signal Power Supply
A2	SGND	Signal Ground
A3	BYPASS	Amplifier Reference Bypass
A4	INA	Amplifier Inverting input A
B1	OUTA	Amplifier Inverting output A
B2	OUTB	Amplifier Non-Inverting Output B
B3	$\overline{RESET}$	Active Low Reset Input. Connect to V_{DD} for normal operation. Toggle between V_{DD} and GND to reset the device.
B4	INB	Amplifier Non-Inverting Input B
C1	V_{SS}	Charge Pump Output
C2	SCL	I^2C Serial Clock Input
C3	SDA	I^2C Serial Data Input
C4	I^2CV_{DD}	I^2C Supply Voltage
D1	C1N	Charge Pump Flying Capacitor Negative Terminal
D2	PGND	Power Ground
D3	C1P	Charge Pump Flying Capacitor Positive Terminal
D4	PV_{DD}	Power Supply

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ABSOLUTE MAXIMUM RATINGS (1) (2)

Supply Voltage (1)	5.25V
Storage Temperature	−65°C to +150°C
Input Voltage	−0.3V to V_{DD} +0.3V
Power Dissipation (3)	Internally Limited
ESD Rating (4)	8kV
ESD Rating (5)	250V
Junction Temperature	150°C
Thermal Resistance	
θ_{JA} (typ) - (TLA1611A)	63.2°C/W

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
(2) The Electrical Characteristics tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.
(3) The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation is $P_{DMAX} = (T_{JMAX} - T_A) / \theta_{JA}$ or the number given in *Absolute Maximum Ratings*, whichever is lower.
(4) Human body model, applicable std. JESD22-A114C.
(5) Machine model, applicable std. JESD22-A115-A.

OPERATING RATINGS

Temperature Range	
$T_{MIN} \le T_A \le T_{MAX}$	$-40°C \le T_A \le +85°C$
Supply Voltage	
PV_{DD} and SV_{DD}	$2.0V \le V_{DD} \le 4.5V$
I^2CV_{DD}	$1.8V \le I^2CV_{DD} \le 4.5V$

AUDIO AMPLIFIER ELECTRICAL CHARACTERISTICS V_{DD} = 4.2V (1) (2)

The following specifications apply for A_V = 6dB, R_L = 2.2µF+15Ω, C1 = C2 = 2.2µF, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions		LM48823 Typical (3)	LM48823 Limits (4)	Units (Limits)
I_{DD}	Quiescent Power Supply Current	V_{IN} = 0V, R_L = ∞		3.3	4.3	mA (max)
I_{SD}	Shutdown Current	Shutdown Enabled		0.01	1	µA (max)
V_{OS}	Differential Output Offset Voltage	V_{IN} = 0V		0.5	3	mV (max)
V_{IH}	Logic High Input Threshold	$\overline{\text{RESET}}$			1.4	V (min)
V_{IL}		$\overline{\text{RESET}}$			0.4	V (max)
A_V	Gain	Minimum Gain Setting		–70		dB
		Maximum Gain Setting		24		dB
R_{IN}	Input Resistance	Maximum Gain Setting		9	7	kΩ (min)
				9	11	kΩ (max)
		Minimum Gain Setting		80	64	kΩ (min)
				80	96	kΩ (max)
V_O	Output Voltage	R_L = 2.2µF+15Ω, THD+N = 1%	f = 1kHz	5.4		V_{RMS}
			f = 5kHz	3.1		V_{RMS}
THD+N	Total Harmonic Distortion + Noise	V_O = 4V_{RMS}		0.015		%
PSRR	Power Supply Rejection Ratio	V_{RIPPLE} = 200mV_{P-P} Sine, Inputs AC GND, C_{IN} = 1µF, input referred	f = 217Hz	93	82	dB (min)
			f = 1kHz	93		dB
SNR	Signal-to-Noise-Ratio	P_{OUT} = 40mW, R_L = 16Ω f = 1kHz		119		dB
ϵ_{OS}	Output Noise	AV = 4dB, Input Referred, A-weighted Filter		5.5		µV
T_{WU}	Wake-Up Time			200		µs

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(2) The Electrical Characteristics tables list ensured specifications under the listed *Recommended Operating Conditions* except as otherwise modified or specified by the *Electrical Characteristics Conditions* and/or Notes. Typical specifications are estimations only and are not ensured.

(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.

(4) Datasheet min/max specification limits are specified by test or statistical analysis.

I^2C INTERFACE CHARACTERISTICS V_{DD} = 3.0V (1) (2)

The following specifications apply for A_V = 6dB, R_L = 2.2µF+15Ω, C1 = C2 = 2.2µF, f = 1kHz, unless otherwise specified. Limits apply for T_A = 25°C.

Symbol	Parameter	Conditions	LM48823		Units (Limits)
			Typical (3)	Limits (4)	
t_1	SCL period			2.5	µs (min)
t_2	SDA Setup Time			100	ns (min)
t_3	SDA Stable Time			0	ns (min)
t_4	Start Condition Time			100	ns (min)
t_5	Stop Condition Time			100	ns (min)
V_{IH}	Logic High Input Threshold			0.7 x I^2CV_{DD}	V (min)
V_{IL}	Logic Low Input Threshold			0.3 x I^2CV_{DD}	V (max)

(1) "*Absolute Maximum Ratings*" indicate limits beyond which damage to the device may occur, including inoperability and degradation of device reliability and/or performance. Functional operation of the device and/or non-degradation at the *Absolute Maximum Ratings* or other conditions beyond those indicated in the *Recommended Operating Conditions* is not implied. The *Recommended Operating Conditions* indicate conditions at which the device is functional and the device should not be operated beyond such conditions. All voltages are measured with respect to the ground pin, unless otherwise specified.
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(3) Typical values represent most likely parametric norms at T_A = +25ºC, and at the *Recommended Operation Conditions* at the time of product characterization and are not ensured.
(4) Datasheet min/max specification limits are specified by test or statistical analysis.

TYPICAL PERFORMANCE CHARACTERISTICS

THD+N vs Frequency
V_{DD} = 3.6V

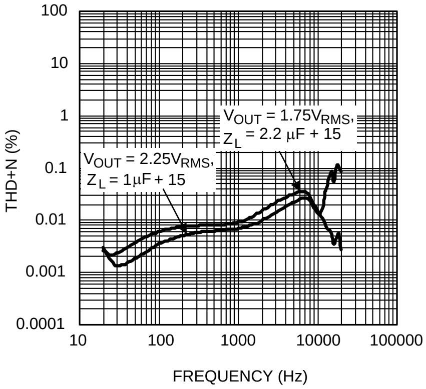

Figure 3.

THD+N vs Frequency
V_{DD} = 4.2V

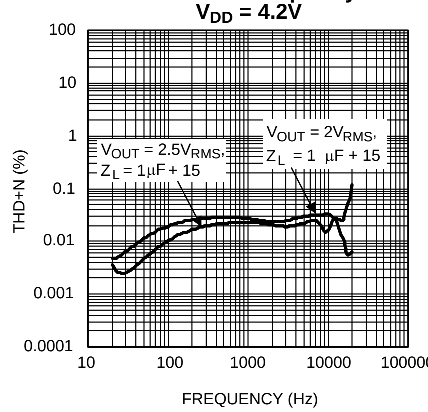

Figure 4.

THD+N vs Output Voltage
A_V = 6dB, Z_L = 1μF+15Ω, f = 1kHz

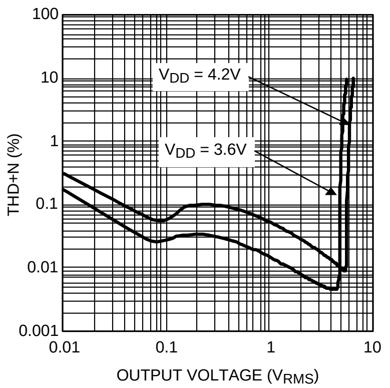

Figure 5.

THD+N vs Output Voltage
A_V = 6dB, Z_L = 2.2μF+15Ω, f = 1kHz

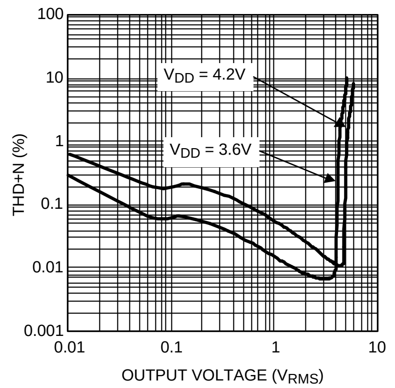

Figure 6.

Output Voltage vs Frequency
V_{DD} = 4.2V, Z_L = 1μF+15Ω,THD+N = 1%

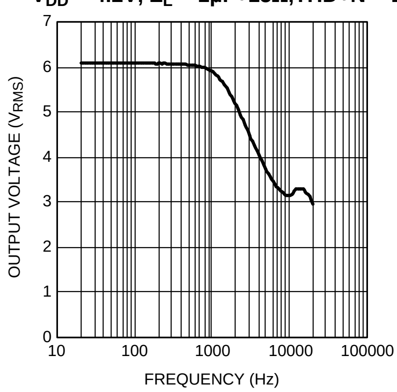

Figure 7.

Output Voltage vs Frequency
V_{DD} = 4.2V, Z_L = 2.2μF+15Ω,THD+N = 1%

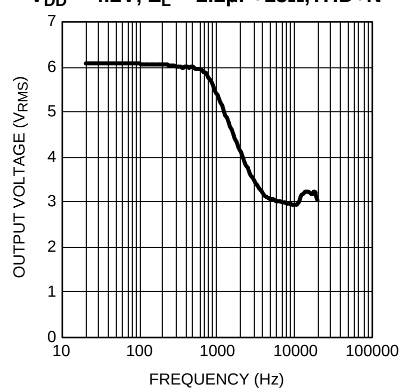

Figure 8.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

Power Consumption vs Output Voltage
V_{DD} = 3.6V, Z_L = 1µF+15Ω

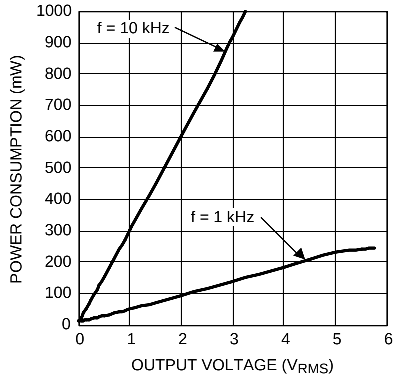

Figure 9.

Power Consumption vs Output Voltage
V_{DD} = 3.6V, Z_L = 2.2µF+15Ω

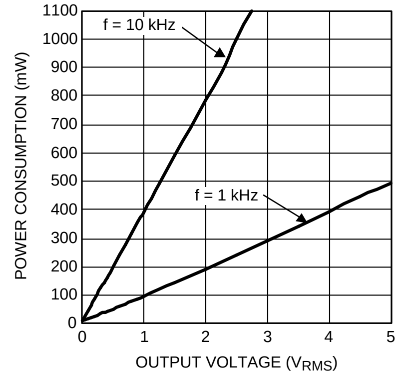

Figure 10.

Power Consumption vs Output Voltage
V_{DD} = 4.2V, Z_L = 1µF+15Ω

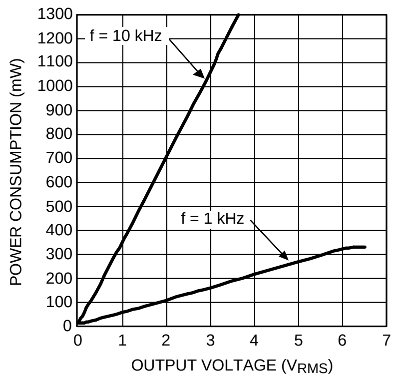

Figure 11.

Power Consumption vs Output Voltage
V_{DD} = 4.2V, Z_L = 2.2µF+15Ω

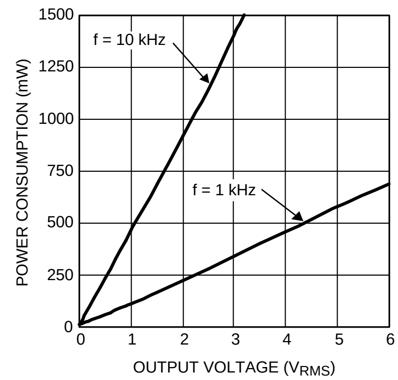

Figure 12.

Output Voltage vs Supply Voltage
Z_L = 1µF+15Ω, THD+N = 1%

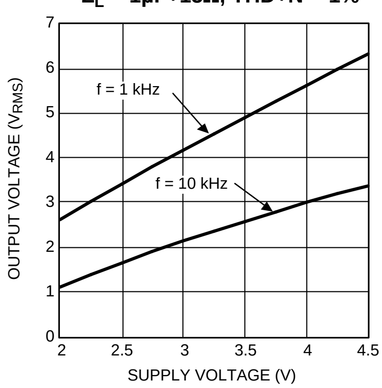

Figure 13.

Output Voltage vs Supply Voltage
Z_L = 2.2µF+15Ω, THD+N = 1%

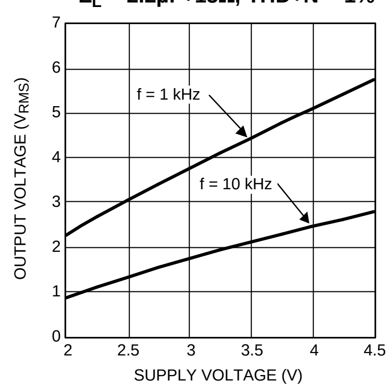

Figure 14.

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

PSRR vs Frequency
V_{DD} = 4.2V, V_{RIPPLE} = 200mV_{P-P}
Z_L = 1μF+15Ω, Input referred

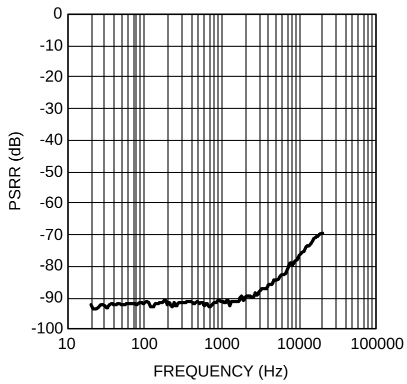

Figure 15.

Supply Current vs Supply Voltage
No Load

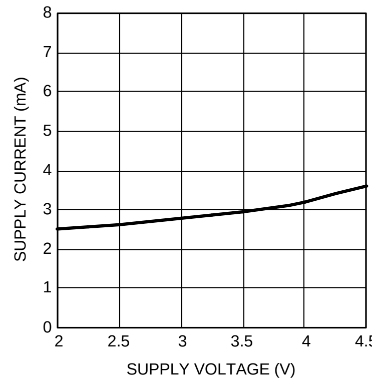

Figure 16.

Shutdown Current vs Supply Voltage
No Load

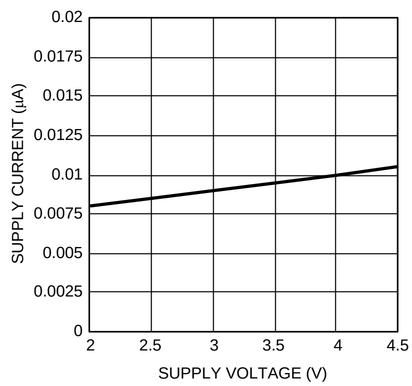

Figure 17.

APPLICATION INFORMATION

I^2C COMPATIBLE INTERFACE

The LM48823 is controlled through an I^2C compatible serial interface that consists of a serial data line (SDA) and a serial clock (SCL). The clock line is uni-directional. The data line is bi-directional (open drain). The LM48823 and the master can communicate at clock rates up to 400kHz. Figure 18 shows the I^2C interface timing diagram. Data on the SDA line must be stable during the HIGH period of SCL. The LM48823 is a transmit/receive slave-only device, reliant upon the master to generate the SCL signal. Each transmission sequence is framed by a START condition and a STOP condition (Figure 19). Each data word, device address and data, transmitted over the bus is 8 bits long and is always followed by an acknowledge pulse (Figure 20). The LM48823 device address is 1110110.

I^2C BUS FORMAT

The I^2C bus format is shown in Figure 20. The START signal, the transition of SDA from HIGH to LOW while SCL is HIGH, is generated, alerting all devices on the bus that a device address is being written to the bus.

The 7-bit device address is written to the bus, most significant bit (MSB) first, followed by the $R/\overline{W}$ bit. $R/\overline{W}$ = 0 indicates the master is writing to the slave device, $R/\overline{W}$ = 1 indicates the master wants to read data from the slave device. Set $R/\overline{W}$ = 0; the LM48823 is a WRITE-ONLY device and will not respond to the $R/\overline{W}$ = 1. The data is latched in on the rising edge of the clock. Each address bit must be stable while SCL is HIGH. After the last address bit is transmitted, the master device releases SDA, during which time, an acknowledge clock pulse is generated by the slave device. If the LM48823 receives the correct address, the device pulls the SDA line low, generating an acknowledge bit (ACK).

Once the master device registers the ACK bit, the 8-bit register data word is sent. Each data bit should be stable while SCL is HIGH. After the 8-bit register data word is sent, the LM48823 sends another ACK bit. Following the acknowledgement of the register data word, the master issues a STOP bit, allowing SDA to go high while SCL is high.

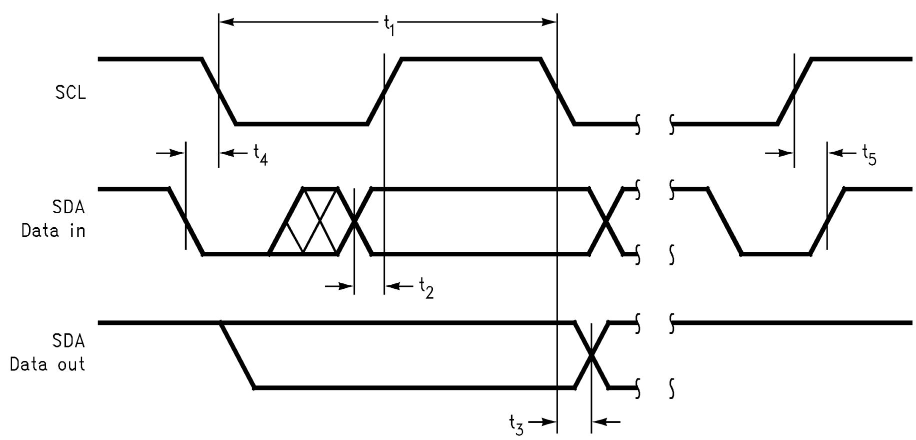

Figure 18. I^2C Timing Diagram

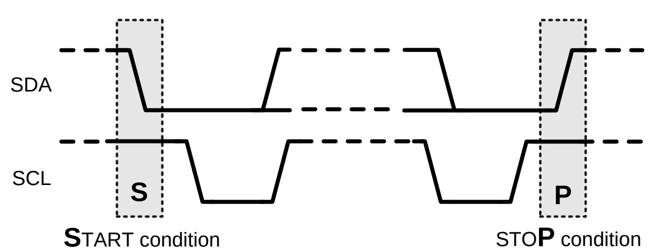

Figure 19. Start and Stop Diagram

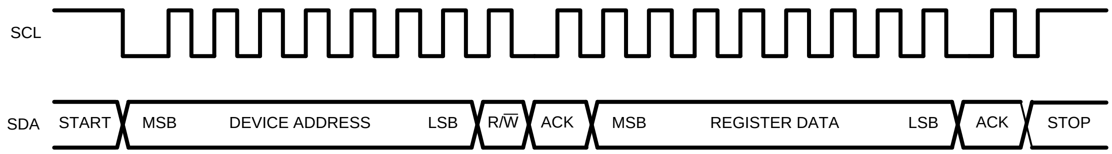

Figure 20. Example Write Sequence

Table 1. Device Address

	B7	B6	B5	B4	B3	B2	B1	B0 R/W
Chip Address	1	1	1	0	1	1	0	0

Table 2. Mode Control Registers

Register Name	B7	B6	B5	B4	B3	B2	B1	B0
Mode Control	VOL4	VOL3	VOL2	VOL1	VOL0	0	ENABLE_A	ENABLE_B

GENERAL AMPLIFIER FUNCTION

The LM48823 is a ceramic speaker driver that utilizes TI's inverting charge pump technology to deliver over $15V_{P-P}$ to a 2.2µF ceramic speaker while operating from a single 4.2V supply. The LM48823 features a unique input stage that converts two single-ended audio signals into a mono BTL output. This stereo to mono conversion is useful in applications where a stereo audio source is driving a single ceramic speaker, such as a ringer on a cellular phone. Connect INA and INB as shown in Figure 21 for the stereo-to-mono conversion. When the LM48823 is used with a single-ended mono audio source, connect both INA and INB to the audio source as shown in Figure 22.

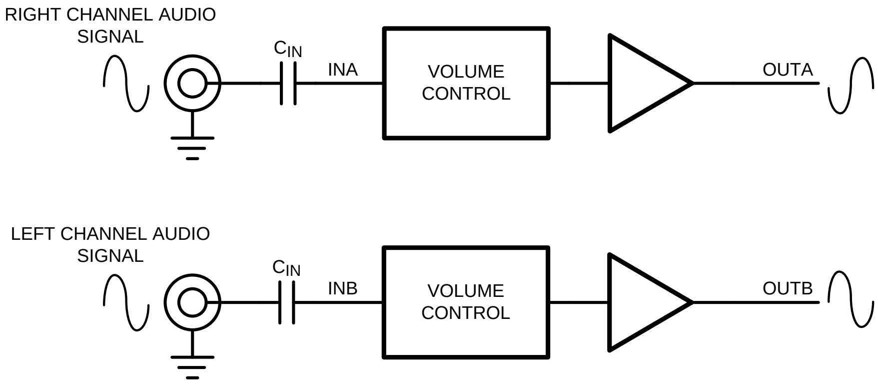

Figure 21. Stereo to Mono Conversion Connection Example

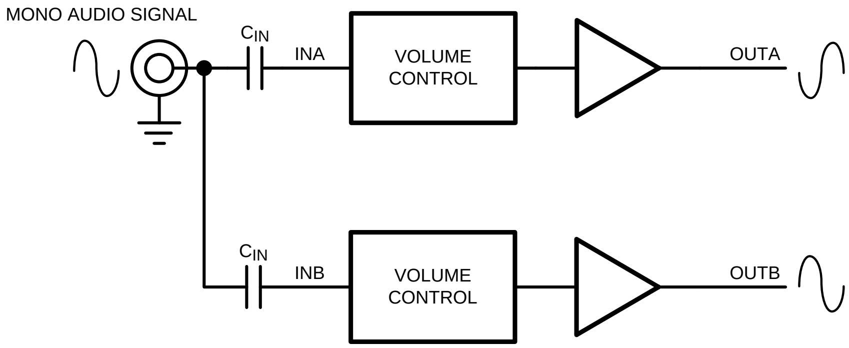

Figure 22. Mono Audio Source Connection Example

VOLUME CONTROL

Table 3. Volume Control

Volume Step	VOL4	VOL3	VOL2	VOL1	VOL0	Gain (dB)
1	0	0	0	0	0	–70
2	0	0	0	0	1	–56
3	0	0	0	1	0	–46
4	0	0	0	1	1	–38
5	0	0	1	0	0	–32
6	0	0	1	0	1	–28
7	0	0	1	1	0	–24
8	0	0	1	1	1	–21
9	0	1	0	0	0	–18
10	0	1	0	0	1	–15
11	0	1	0	1	0	–12
12	0	1	0	1	1	–10
13	0	1	1	0	0	–8
14	0	1	1	0	1	–6
15	0	1	1	1	0	–4
16	0	1	1	1	1	–2
17	1	0	0	0	0	0
18	1	0	0	0	1	2
19	1	0	0	1	0	4
20	1	0	0	1	1	6
21	1	0	1	0	0	8
22	1	0	1	0	1	10
23	1	0	1	1	0	12
24	1	0	1	1	1	14
25	1	1	0	0	0	16
26	1	1	0	0	1	18
27	1	1	0	1	0	19
28	1	1	0	1	1	20
29	1	1	1	0	0	21
30	1	1	1	0	1	22
31	1	1	1	1	0	23
32	1	1	1	1	1	24

SHUTDOWN FUNCTION

The LM48823 features a low-power shutdown mode that disables the device, lowering the quiescent current to 0.01µA. Set bits B1 (ENABLE_A) and B2 (ENABLE_B) to 0 to disable the amplifiers and charge pump. Set both ENABLE_A and ENABLE_B to 1 for normal operation. Shutdown mode does not clear the I^2C register. When re-enabled, the device returns to its previous volume setting. To clear the I^2C register, either remove power from the device, or toggle $\overline{\text{RESET}}$ (see *RESET* section).

$\overline{\text{RESET}}$

The LM48823 features an active low reset input. Driving $\overline{\text{RESET}}$ low clears the I^2C register. Volume control is set to 00000 (-70dB) and both ENABLE_A and ENABLE_B are set to 0, disabling the device. While $\overline{\text{RESET}}$ is low, the LM48823 ignores any I^2C data. After the device is reset, and $\overline{\text{RESET}}$ is driven high, the LM48823 remains in shutdown mode with the volume set to -70dB. Re-enable the device by writing to the I^2C register.

PROPER SELECTION OF EXTERNAL COMPONENTS

Power Supply Bypassing/Filtering

Proper power supply bypassing is critical for low noise performance and high PSRR. Place the supply bypass capacitors as close to the device as possible. Place a 1µF ceramic capacitor from V_{DD} to GND. Additional bulk capacitance may be added as required.

Bypass Capacitor Selection

The BYPASS capacitor, C_{BYPASS}, improves PSRR, noise rejection and output offset. For best results, use a capacitor of identical value to the input coupling capacitors

Charge Pump Capacitor Selection

Use low ESR ceramic capacitors (less than 100mΩ) for optimum performance.

Charge Pump Flying Capacitor (C1)

The flying capacitor (C1) affects the load regulation and output impedance of the charge pump. A C1 value that is too low results in a loss of current drive, leading to a loss of amplifier headroom. A higher valued C1 improves load regulation and lowers charge pump output impedance to an extent. Above 2.2µF, the $R_{DS(ON)}$ of the charge pump switches and the ESR of C1 and C2 dominate the output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Charge Pump Hold Capacitor (C2)

The value and ESR of the hold capacitor (C2) directly affects the ripple on CPV_{SS}. Increasing the value of C2 reduces output ripple. Decreasing the ESR of C2 reduces both output ripple and charge pump output impedance. A lower value capacitor can be used in systems with low maximum output power requirements.

Input Capacitor Selection

Input capacitors block the DC component of the audio signal, eliminating any conflict between the DC component of the audio source and the bias voltage of the LM48823. The input capacitors create a high-pass filter with the input resistors R_{IN}. The -3dB point of the high pass filter is found using Equation 1.

$$f = 1 / 2\pi R_{IN} C_{IN} \quad \text{(Hz)} \tag{1}$$

where

- the value of R_{IN} is given in the Electrical Characteristics table.

High pass filtering the audio signal helps protect the speakers. When the LM48823 is using a single-ended source, power supply noise on the ground is seen as an input signal. Setting the high-pass filter point above the power supply noise frequencies, 217Hz in a GSM phone, for example, filters out the noise such that it is not amplified and heard on the output. Capacitors with a tolerance of 10% or better are recommended for impedance matching and improved CMRR and PSRR.

PCB LAYOUT GUIDELINES

Minimize trace impedance of the power, ground and all output traces for optimum performance. Voltage loss due to trace resistance between the LM48823 and the load results in decreased output power and efficiency. Trace resistance between the power supply and ground has the same effect as a poorly regulated supply, increased ripple and reduced peak output power. Use wide traces for power supply inputs and amplifier outputs to minimize losses due to trace resistance, as well as route heat away from the device. Proper grounding improves audio performance, minimizes crosstalk between channels and prevents switching noise from interfering with the audio signal. Use of power and ground planes is recommended.

Place all digital components and route digital signal traces as far as possible from analog components and traces. Do not run digital and analog traces in parallel on the same PCB layer. If digital and analog signal lines must cross either over or under each other, ensure that they cross in a perpendicular fashion.

LM48823TL DEMOBOARD BILL OF MATERIALS

Designator	Quantity	Description
C1, C2	2	2.2µF ±10% 10V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB1A225K Murata GRM033R6OJ104KE19D
C3 – C5	3	1µF ±10% 10V Tantalum Capacitor (402) AVX TACK105M010QTA
C6	1	4.7µF ±10% 6.3V X5R Ceramic Capacitor (603) Panasonic ECJ-1VB0J475K Murata GRM188R6OJ475KE19D
C7, C8	2	0.1µF ±10% 6.3V X5R Ceramic Capacitor (201) Panasonic ECJ-ZEB0J104K Murata GRM188R61A225KE34D
JU1 – JU5	5	2 Pin Header
JU6, JU7	3	2 Pin Header
J1	1	5-Pin I^{2}C Header
LM4823TL	1	LM48823TL (16-Bump DSBGA)

DEMO BOARD SCHEMATIC

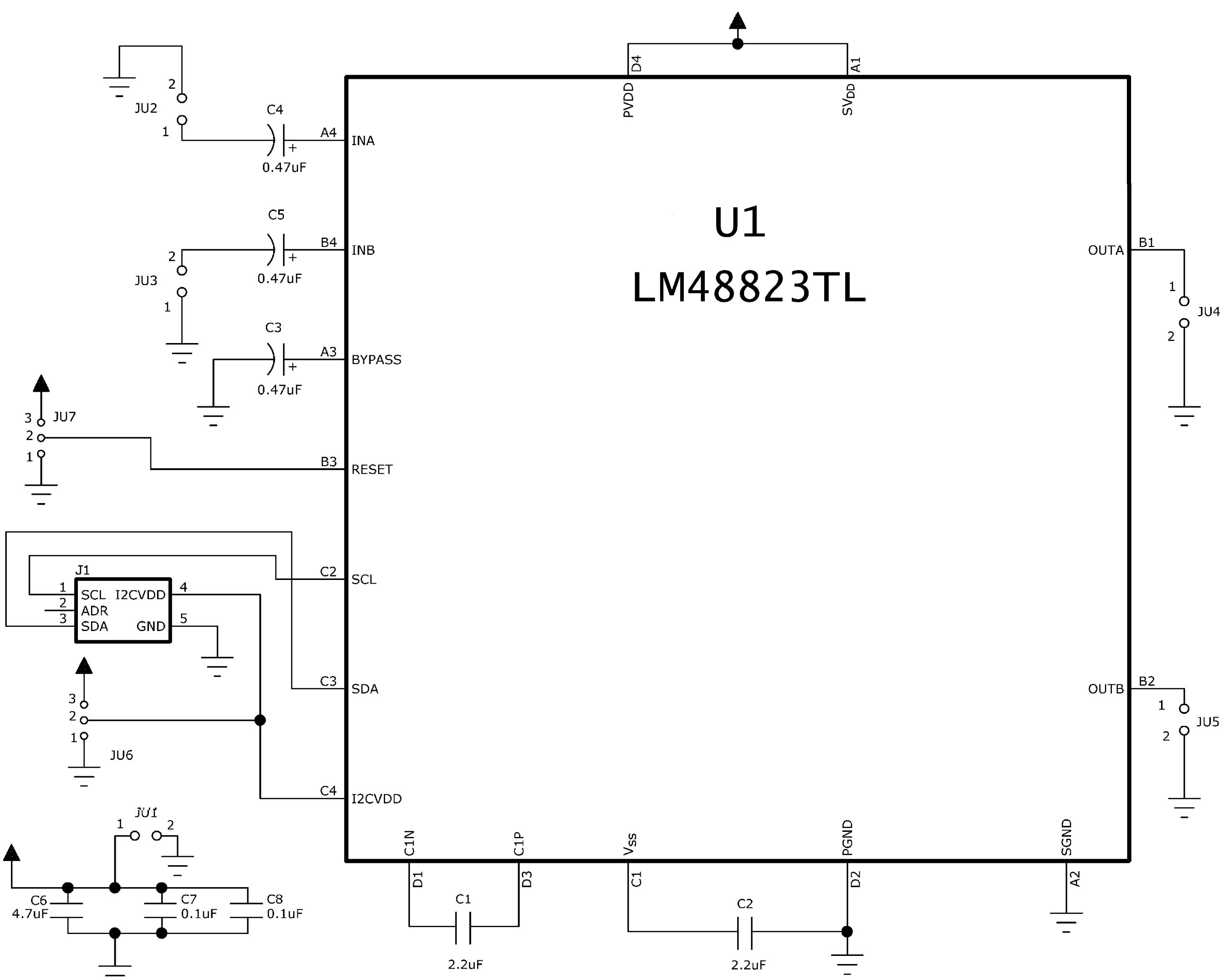

Figure 23. LM48823 Demo Board Schematic

PC BOARD LAYOUT

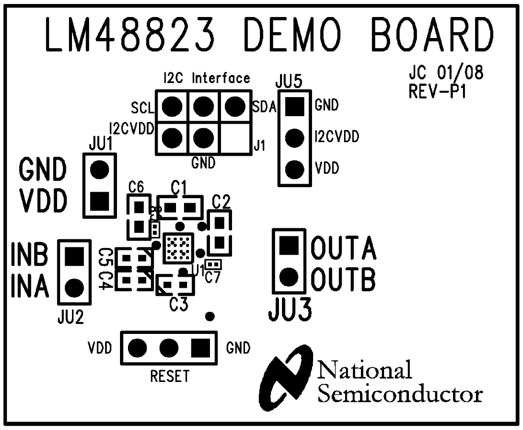

Figure 24. Top Silkscreen Layer

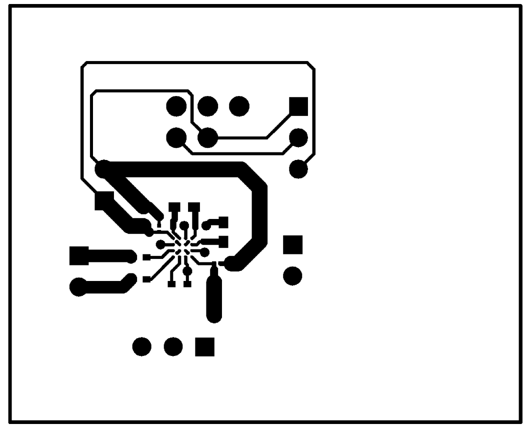

Figure 25. Top Layer

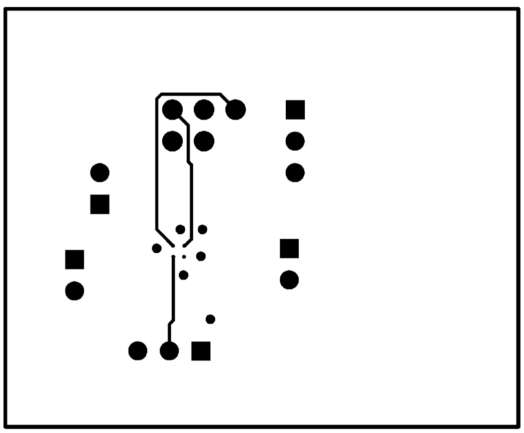

Figure 26. Layer 2

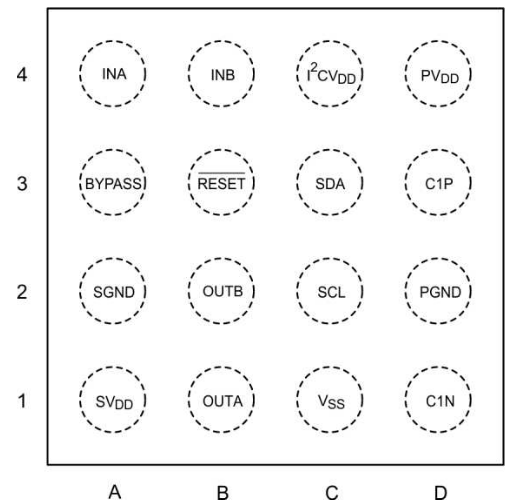

Figure 27. Layer 3

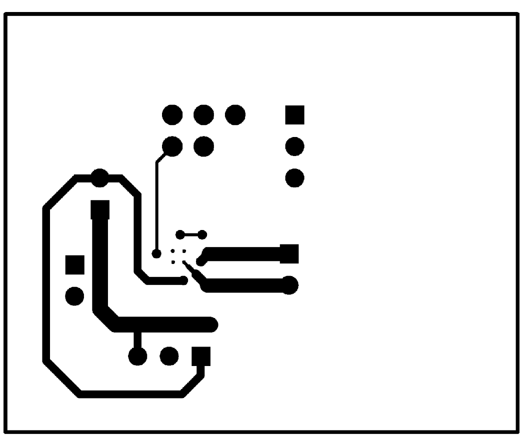

Figure 28. Bottom Layer

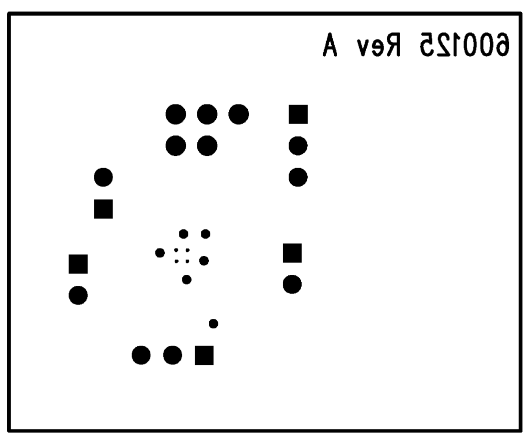

Figure 29. Bottom Silkscreen

REVISION HISTORY

Rev	Date	Description
1.0	06/27/08	Initial release.
1.01	07/15/08	Edited the Ordering Information table.
1.02	10/08/10	Updated some Limits (under Gain) in the Volume Control table.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
LM48823TL/NOPB	ACTIVE	DSBGA	YZR	16	250	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		GK6	Samples
LM48823TLX/NOPB	ACTIVE	DSBGA	YZR	16	3000	Green (RoHS & no Sb/Br)	SNAGCU	Level-1-260C-UNLIM		GK6	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) Only one of markings shown within the brackets will appear on the physical device.

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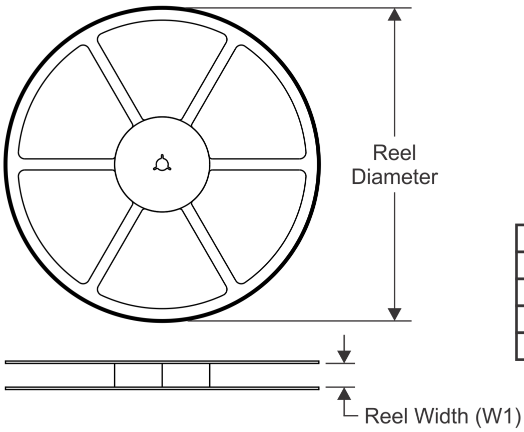
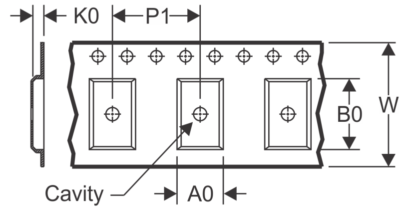
TAPE AND REEL INFORMATION

REEL DIMENSIONS

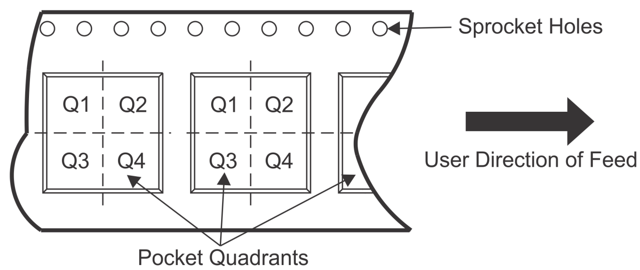


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

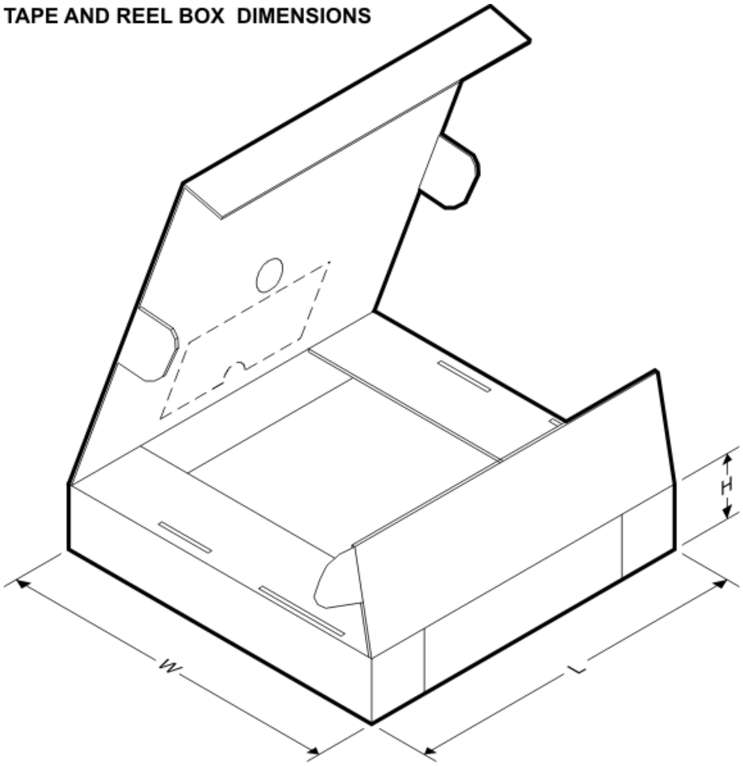
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM48823TL/NOPB	DSBGA	YZR	16	250	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1
LM48823TLX/NOPB	DSBGA	YZR	16	3000	178.0	8.4	2.08	2.08	0.76	4.0	8.0	Q1

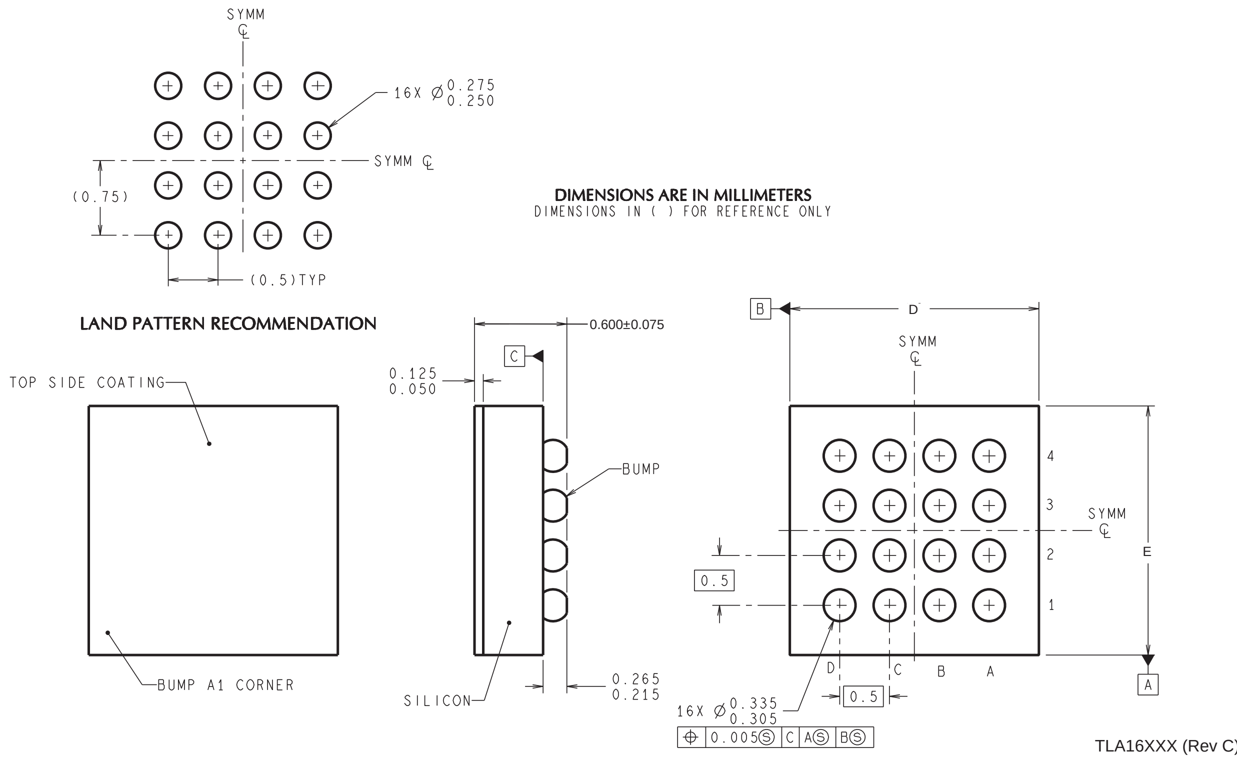
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM48823TL/NOPB	DSBGA	YZR	16	250	210.0	185.0	35.0
LM48823TLX/NOPB	DSBGA	YZR	16	3000	210.0	185.0	35.0

YZR0016



D: Max = 1.99 mm, Min = 1.93 mm

E: Max = 1.99 mm, Min = 1.93 mm

4215051/A 12/12

NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
B. This drawing is subject to change without notice.

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