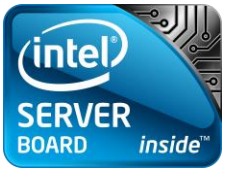
Intel® Server Board S1200KP

Technical Product Specification

Intel order number G38894-002



Revision 1.1

April, 2012

Enterprise Platforms and Services Division – Marketing

Revision History

Date	Revision Number	Modifications
July 2011	1.0	Initial release.
April 2012	1.1	Added info for DBS1200KPR and BBS1200KPR.

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1. Introduction

This Technical Product Specification (TPS) specifies the board layout, components, connectors, power and environmental requirements, and the BIOS for Intel® Server Board S1200KP.

1.1 Intended Audience

The TPS is intended to provide detailed, technical information about Intel® Server Board S1200KP and its components to the vendors, system integrators, and other engineers and technicians who need this level of information. It is specifically not intended for general audiences.

1.2 What This Document Contains

Chapter	Description
1	A description of the hardware used on Intel® Server Board S1200KP.
2	A map of the resources of the Intel® Server Board.
3	The features supported by the BIOS Setup program.
4	Descriptions of the BIOS error messages, beep codes, and POST codes.

1.3 Typographical Conventions

This section contains information about the conventions used in this specification. Not all of these symbols and abbreviations appear in all specifications of this type.

Notes, Cautions, and Warnings

Note: Notes call attention to important information.

CAUTION

Cautions are included to help you avoid damaging hardware or losing data.

Other Common Notation

#	Used after a signal name to identify an active-low signal (such as USBP0#).
GB	Gigabyte (1,073,741,824 bytes).
GB/s	Gigabytes per second.
Gb/s	Gigabits per second.
KB	Kilobyte (1024 bytes).
Kbit	Kilobit (1024 bits).
kbits/s	1000 bits per second.
MB	Megabyte (1,048,576 bytes).
MB/s	Megabytes per second.
Mbit	Megabit (1,048,576 bits).

Mbits/s	Megabits per second.
xxh	An address or data value ending with a lowercase h indicates a hexadecimal value.
x.x V	Volts. Voltages are DC unless otherwise specified.
*	This symbol is used to indicate third-party brands and names that are the property of their respective owners.

2. Product Description

2.1 Overview

2.1.1 Feature Summary

Table 1 summarizes the major features of the board.

Table 1. Feature Summary

Feature	Description
Form Factor	Mini-ITX (6.7 inches by 6.7 inches [170.18 millimeters by 170.18 millimeters])
Processor	▪ Intel® Xeon® E3-1200 Processors, the 2nd Generation Intel® Core™ i3 Processors, Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors with up to 95W TDP in an LGA1155 socket [1, 2] o One PCI Express* 2.0 x16 (with Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors) or PCI Express* 3.0 x 16 (with Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors) graphics interface o Integrated memory controller with dual channel DDR3 memory support o Integrated graphics processing (processors with Intel® Graphics Technology)
Memory	▪ Two 240-pin DDR3 DRAM Dual Inline Memory Module (DIMM) sockets ▪ Support for DDR3 1066/1333 MHz (with Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors) or DDR3 1333/1600 MHz (with Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors) DIMMs ▪ Support for 1Gb, 2Gb, and 4Gb memory technology ▪ Support for up to 16 GB of system memory with two DIMMs using 4 Gb memory technology ▪ Support for ECC and non-ECC memory[3]
Chipset	Intel® C206 Platform Controller Hub (PCH) Chipset
Graphics	▪ Integrated graphics support for processors with Intel® Graphics Technology: o DVI-I ▪ Discrete graphics support for PCI Express* 2.0 x16 (with Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors) or PCI Express* 3.0 x 16 (with Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors) add-in graphics card
Peripheral Interfaces	▪ Eight USB 2.0 ports: o Four ports are implemented with stacked back panel connectors (black) o Four front panel ports implemented through three internal headers ▪ Two SATA 6.0Gb/s interfaces through Intel® C206 Chipset with Intel® Rapid Storage Technology RAID support (blue) ▪ Two SATA 3.0Gb/s interfaces through Intel® C206 Chipset with Intel® Rapid Storage Technology RAID support (black)
Expansion Capabilities	▪ One PCI Express* 2.0 x16 (with Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors) or PCI Express* 3.0 x 16 (with Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors) add-in card connector

Feature	Description
BIOS	▪ Intel® BIOS resident in the Serial Peripheral Interface (SPI) Flash device ▪ Support for Advanced Configuration and Power Interface (ACPI), Plug and Play, and System Management BIOS (SMBIOS)
Instantly Available PC Technology	▪ Support for PCI Express* Revision 2.0 (with Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors) or PCI Express* Revision 3.0 (with Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors) ▪ Suspend to RAM support ▪ Wake on PCI Express*, LAN, front panel, and USB ports
LAN Support	▪ Gigabit (10/100/1000Mbits/s) LAN subsystem using the Intel® 82574 and 82579 Gigabit Ethernet Controller
Legacy I/O Control	▪ Nuvoton* W83677HG-i I/O controller for hardware management support
Hardware Monitor Subsystem	▪ Hardware monitoring through the Nuvoton I/O controller ▪ Voltage sense to detect out of range power supply voltages ▪ Thermal sense to detect out of range thermal values ▪ Two fan headers ▪ Two fan sense inputs used to monitor fan activity ▪ Fan speed control

Notes:

1. Pairing a mini-ITX chassis and more than 65W TDP processor with the supplied standard Intel® thermal solution may not meet Intel®'s thermal requirement standard. Please verify that your thermal solution and chassis will meet the necessary thermal requirements. Failing to do so may cause the processor to throttle, significantly decreasing system performance.
2. The product codes of DBS1200KP and BBS1200KP can only support Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors. The product codes of DBS1200KPR and BBS1200KPR can support Intel® Xeon® E3-1200 Processors, the 2nd Generation Intel® Core™ i3 Processors, Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors.
3. ECC DIMMS are recommended to use for server system.

2.1.2 Board Layout

Following figure shows the location of the major components on Intel® Server Board S1200KP:

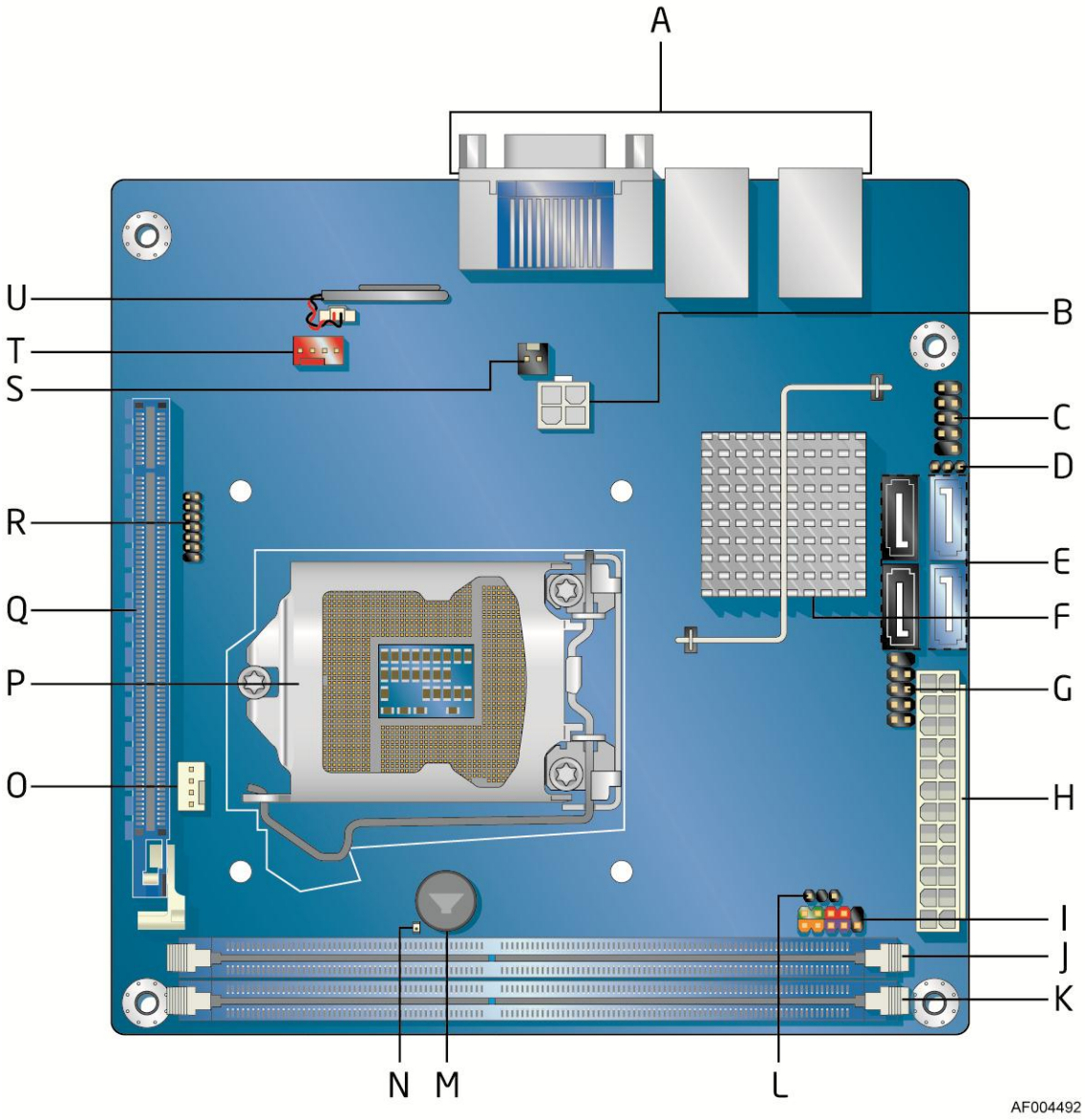


Figure 1. Major Board Components

Table 2 lists the components identified in Figure 1.

Table 2. Components Shown in Figure 1

Item/callout	Description
A	Back panel connectors
B	Processor core power connector (2 x 2)
C	Front panel USB 2.0 header
D	BIOS Setup configuration jumper block
E	SATA connectors
F	Intel® C206 Chipset
G	Front panel USB 2.0 header
H	Main power connector (2 x 12)
I	Front panel header
J	DIMM 1 (Channel A DIMM 1)
K	DIMM 2 (Channel B DIMM 1)
L	Alternate front panel power LED header
M	Piezoelectric speaker
N	Standby power LED
O	Processor fan header
P	LGA1155 processor socket
Q	PCI Express* x16 bus add-in card connector
R	Low Pin Count (LPC) Debug header
S	Chassis intrusion header
T	System fan header
U	Battery

2.1.3 Block Diagram

Figure 2 is a block diagram of the major functional areas of the board.

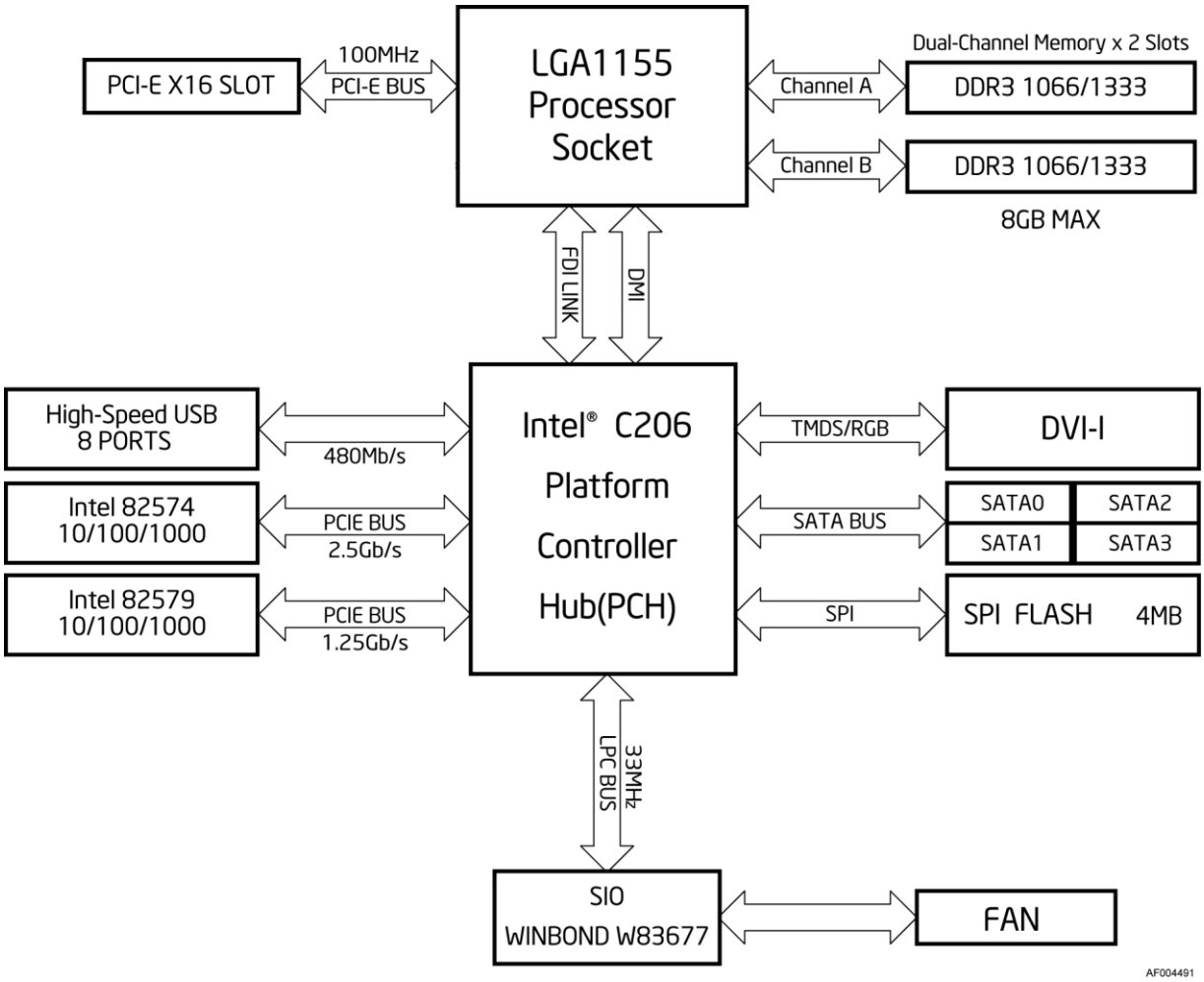


Figure 2. Block Diagram

2.2 Online Support

Table 3. Reference URLs for Online Suppot

To find information about	Visit this World Wide Web site:
Intel® Server Board S1200KP	http://www.intel.com/products/server
Supported processors and tested memory	http://serverconfigurator.intel.com
BIOS and driver updates	http://downloadcenter.intel.com

2.3 Processor

The board is designed to support the Intel® Xeon® E3-1200 Processors, the 2nd Generation Intel® Core™ i3 Processors, Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors in an LGA1155 socket.

Other processors may be supported in the future. This board is designed to support processors with a maximum wattage of 95 W Thermal Design Power (TDP). The processors listed above are only supported when falling within the wattage requirements of Intel® Server Board S1200KP. See the Intel® web site listed below for the most up-to-date list of supported processors.

Table 4. Information on Supported Processors

For information about	Refer to:
Supported processors	http://serverconfigurator.intel.com

CAUTION

Use only the processors listed on the web site above. Use of unsupported processors can damage the board, the processor, and the power supply.

Notes:

1. The product codes of DBS1200KP and BBS1200KP can only support Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors. The product codes of DBS1200KPR and BBS1200KPR can support Intel® Xeon® E3-1200 Processors, the 2nd Generation Intel® Core™ i3 Processors, Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors.
2. This board has specific requirements for providing power to the processor. Refer to Section 3.5.1 on page 40 for information on power supply requirements for this board.
3. Pairing a mini-ITX chassis and more than 65W TDP processor with the supplied standard Intel® thermal solution may not meet Intel®'s thermal requirement standard. Please verify that your thermal solution and chassis will meet the necessary thermal requirements. Failing to do so may cause the processor to throttle, significantly decreasing system performance.

2.3.1 PCI Express* x16 Graphics

The Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors in an LGA1155 socket support discrete add in graphics cards through the PCI Express* 2.0 x16 graphics connector. And the Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors in an LGA1155 socket support discrete add in graphics cards through the PCI Express* 3.0 x16 graphics connector:

- Supports PCI Express* GEN3 frequency of 8 GHz resulting in 8.0 Gb/s each direction (1 GB/s) per lane. The maximum theoretical bandwidth on the interface is 16 GB/s in each direction, simultaneously, for an aggregate of 32 GB/s when operating in x16 GEN3 mode.

- Supports PCI Express* GEN2 frequency of 5 GHz resulting in 5.0 Gb/s each direction (500 MB/s) per lane. The maximum theoretical bandwidth on the interface is 8 GB/s in each direction, simultaneously, for an aggregate of 16 GB/s when operating in x16 GEN2 mode.
- Supports PCI Express* GEN1 frequency of 2.5 GHz resulting in 2.5 Gb/s each direction (250 MB/s) per lane. The maximum theoretical bandwidth on the interface is 4 GB/s in each direction, simultaneously, for an aggregate of 8 GB/s when operating in x16 GEN1 mode.

Table 5. Information on PCI Express* Technology

For information about	Refer to
PCI Express* technology	http://www.pcisig.com

2.4 System Memory

The board has two DIMM sockets and supports the following memory features:

- 1.5 V DDR3 DRAM DIMMs with gold plated contacts.
- Two independent memory channels with interleaved mode support
- Unbuffered, single-sided or double-sided DIMMs with the following restriction:
  Double-sided DIMMs with x16 organization are not supported.
- 16 GB maximum total system memory (with 4 Gb memory technology). Refer to Section 3.1.1 on page 27 for information on the total amount of addressable memory.
- Minimum recommended total system memory: 512 MB
- ECC and Non-ECC DIMMs
- Serial Presence Detect
- Support for DDR3 1066/1333 MHz (with Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors) or DDR3 1333/1600 MHz (with Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors) DIMMs

Notes:

1. To be fully compliant with all applicable DDR DRAM memory specifications, the board should be populated with DIMMs that support the Serial Presence Detect (SPD) data structure. This allows the BIOS to read the SPD data and program the chipset to accurately configure memory settings for optimum performance. If non-SPD memory is installed, the BIOS will attempt to correctly configure the memory settings, but performance and reliability may be impacted or the DIMMs may not function under the determined frequency.
2. ECC DIMMS are recommended to use for server system.

Table 6 lists the supported DIMM configurations.

Table 6. Supported Memory Configurations

DIMM Capacity	Configuration (Note)	DRAM Density	DRAM Organization Front-side/Back-side	Number of DRAM Devices Non-ECC/ECC
512 MB	SS	1 Gbit	1 Gb x16/empty	4/NA
1024 MB	SS	1 Gbit	1 Gb x8/empty	8/9
2048 MB	DS	1 Gbit	1 Gb x8/1 Gb x8	16/18
2048 MB	SS	2 Gbit	2 Gb x8/empty	8/9
4096 MB	DS	2 Gbit	2 Gb x8/2 Gb x8	16/18
8192 MB	DS	4 Gbit	4 Gb x8/4Gb x8	16/18

Note: "DS" refers to double-sided memory modules (containing two rows of DRAM) and "SS" refers to single-sided memory modules (containing one row of DRAM).

Table 7. Information on System Memory

For information about	Refer to:
Tested Memory	http://serverconfigurator.intel.com

2.4.1 Memory Configurations

The Intel® Xeon® E3-1200 Processors, the 2nd Generation Intel® Core™ i3 Processors, Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors in the LGA1155 socket support the following types of memory organization:

- **Dual channel (Interleaved) mode**. This mode offers the highest throughput for real world applications. Dual channel mode is enabled when the installed memory capacities of both DIMM channels are equal. Technology and device width can vary from one channel to the other but the installed memory capacity for each channel must be equal. If different speed DIMMs are used between channels, the slowest memory timing will be used.
- **Single channel (Asymmetric) mode**. This mode is equivalent to single channel bandwidth operation for real world applications. This mode is used when only a single DIMM is installed or the memory capacities are unequal. Technology and device width can vary from one channel to the other. If different speed DIMMs are used between channels, the slowest memory timing will be used.
- **Flex mode**. This mode provides the most flexible performance characteristics. The bottommost DRAM memory (the memory that is lowest within the system memory map) is mapped to dual channel operation; the topmost DRAM memory (the memory that is nearest to the 8 GB address space limit), if any, is mapped to single channel operation. Flex mode results in multiple zones of dual and single channel operation across the whole of DRAM memory. To use flex mode, it is necessary to populate both channels.

Figure 3 illustrates the memory channel and DIMM configuration.

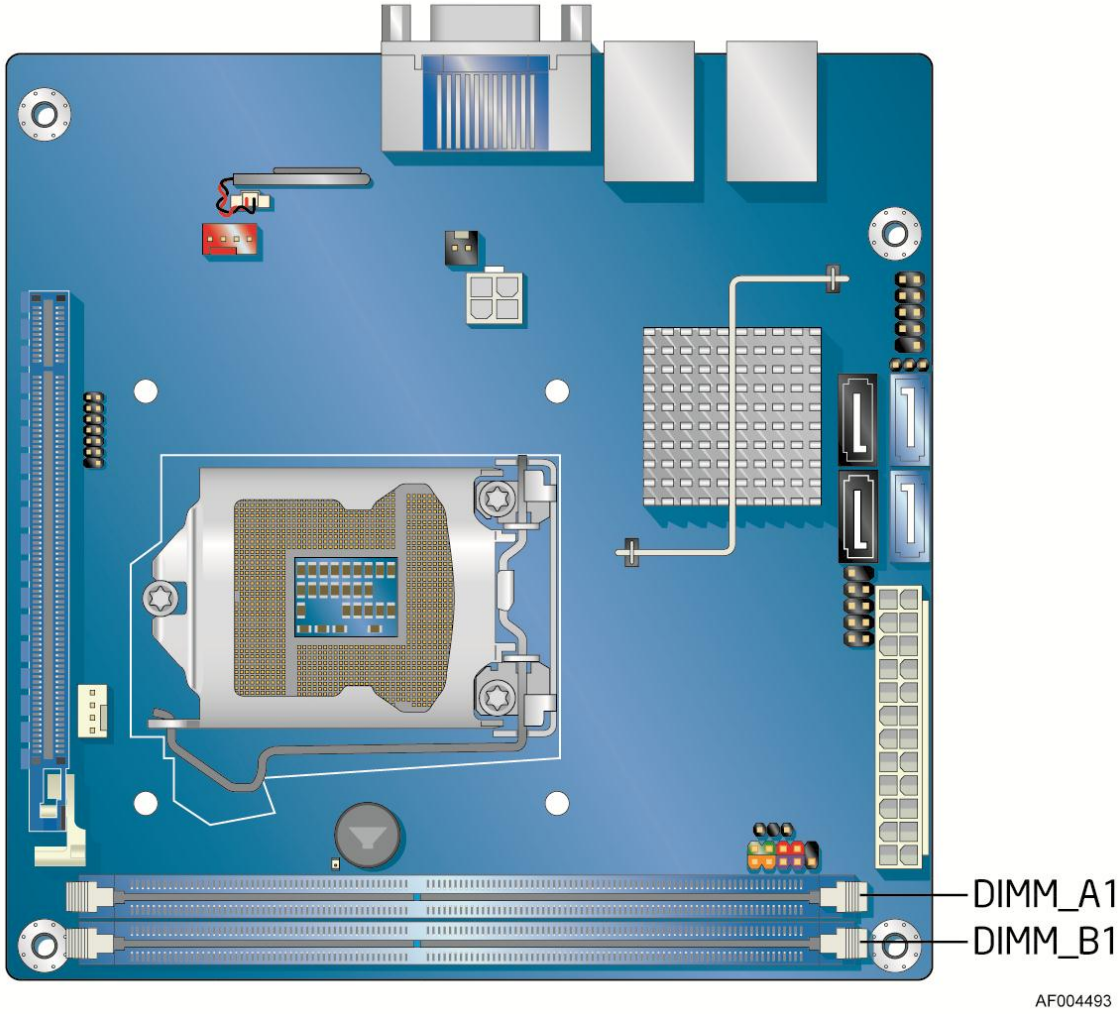


Figure 3. Memory Channel and DIMM Configuration

Note: The Intel® Xeon® E3-1200 Processors, the 2nd Generation Intel® Core™ i3 Processors, Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors require memory to be populated in the DIMM_A1 (Channel A, DIMM 1) socket.

2.5 Intel® C206 Chipset

Intel® C206 Chipset with Direct Media Interface (DMI) interconnect provides interfaces to the processor and the USB, SATA, LPC, LAN and PCI Express* interfaces. The Intel® C206 Chipset is a centralized controller for the board's I/O paths.

Table 8. Information on Resouces Used by the Chipset

For information about	Refer to
Resources used by the chipset	Chapter 2

2.6 Graphics Subsystem

The board supports graphics through either Intel® Graphics Technology or a PCI Express* 2.0 x16 (with Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors) or PCI Express* 3.0 x 16 (with Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors) add-in graphics card.

2.6.1 Integrated Graphics

The board supports integrated graphics through the Intel® Flexible Display Interface (Intel® FDI) for processors with Intel® Graphics Technology.

2.6.1.1 Digital Visual Interface (DVI-I)

The DVI-I port supports both digital and analog DVI displays. The maximum supported resolution is 1900 x 1200 (WUXGA). The DVI port is compliant with the DVI 1.0 specification. DVI analog output can also be converted to VGA using a DVI-VGA converter.

Depending on the type of add-in card installed in the PCI Express* x16 connector, the DVI port will behave as described in Table 9.

Table 9. DVI Port Status Conditions

PCI Express* x16 Connector Status	DVI Digital (DVI-D) Port Status	DVI Analog (DVI-A) Port Status(Note 1)
No add-in card installed	Enabled	Enabled
Non-video PCI Express* x1 add-in card installed	Enabled	Enabled
PCI Express* x16 add-in card installed	Enabled	Enabled (Note 2)

Notes:

1. DVI analog output can also be converted to VGA with a DVI-VGA converter.
2. May require BIOS setup menu changes.

2.6.2 USB

The board supports up to eight USB 2.0 ports.

The Intel® C206 Chipset provides the USB controller for the 2.0 ports. The port arrangement is as follows:

- Four USB 2.0 ports are implemented with stacked back panel connectors (black)
- Four USB 2.0 front panel ports implemented through three internal headers

All eight USB ports are high-speed, full-speed, and low-speed capable.

Note: Computer systems that have an unshielded cable attached to a USB port may not meet FCC Class B requirements, even if no device is attached to the cable. Use a shielded cable that meets the requirements for full-speed devices.

Table 10. Information on USB Connectors

For information about	Refer to
The location of the USB connectors on the back panel	Figure 8, page 30
The location of the front panel USB headers	Figure 9, page 31

2.7 SATA Interfaces

The board provides five SATA connectors through the PCH, which support one device per connector:

- Two internal SATA 6.0 Gb/s connectors (blue)
- Two internal SATA 3.0 Gb/s connectors (black)

The PCH provides independent SATA ports with a theoretical maximum transfer rate of 6 Gb/s for two ports and 3 Gb/s for the other two ports. A point-to-point interface is used for host to device connections.

The underlying SATA functionality is transparent to the operating system. The SATA controller can operate in both legacy and native modes. In legacy mode, standard IDE I/O and IRQ resources are assigned (IRQ 14 and 15). In Native mode, standard PCI Conventional bus resource steering is used. Native mode is the preferred mode for configurations using the Windows 7* operating systems.

Note: Many SATA drives use new low-voltage power connectors and require adapters or power supplies equipped with low-voltage power connectors.

For more information, see: http://www.serialata.org/.

Table 11. Information on SATA Connector Locations

For information about	Refer to
The location of the SATA connectors	Figure 9, page 31

2.7.1.1 SATA RAID

The board supports Intel® Rapid Storage Technology which provides the following RAID (Redundant Array of Independent Drives) levels through the Intel® C206 Chipset:

- RAID 0 - data striping
- RAID 1 - data mirroring

- RAID 0+1 (or RAID 10) - data striping and mirroring
- RAID 5 - distributed parity

2.8 Real-Time Clock Subsystem

A coin-cell battery (CR2032) powers the real-time clock and CMOS memory. When the computer is not plugged into a wall socket, the battery has an estimated life of three years. When the computer is plugged in, the standby current from the power supply extends the life of the battery. The clock is accurate to ± 13 minutes/year at 25 ºC with 3.3 VSB applied through the power supply 5V STBY rail.

Note: If the battery and AC power fail, date and time values will be reset and the user will be notified during the POST.

When the voltage drops below a certain level, the BIOS Setup program settings stored in CMOS RAM (for example, the date and time) might not be accurate. Replace the battery with an equivalent one. Figure 1 on page 5 shows the location of the battery.

2.9 Legacy I/O Controller

The I/O controller provides the following features:

- Serial IRQ interface compatible with serialized IRQ support for PCI systems
- Intelligent power management, including a programmable wake-up event interface
- PCI power management support

The BIOS Setup program provides configuration options for the I/O controller.

2.10 LAN Subsystem

The LAN subsystem consists of the following:

- Intel® 82574L and 82579LM Gigabit Ethernet Controllers (10/100/1000 Mbits/s)
- Intel® C206 Chipset
- RJ-45 LAN connector with integrated status LEDs

Additional features of the LAN subsystem include:

- CSMA/CD protocol engine
- LAN connect interface between the PCH and the LAN controller
- PCI Conventional bus power management
  - ACPI technology support
  - LAN wake capabilities
- LAN subsystem software

Table 12. Information on LAN Software and Drivers

For information about	Refer to
LAN software and drivers	http://downloadcenter.intel.com

2.10.1 Intel® 82574L Gigabit Ethernet Controller

The Intel® 82574L Gigabit Ethernet Controller supports the following features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Dual interconnect between the Integrated LAN Controller and the Physical Layer (PHY):
  - PCI Express*-based interface for active state operation (S0) state
  - SMBUS* for host and management traffic (Sx low power state)
- Compliant to IEEE 802.3x flow control support
- 802.1p and 802.1q
- TCP, IP, and UDP checksum offload (for IPv4 and IPv6)
- Full device driver compatibility

2.10.2 Intel® 82579LM Gigabit Ethernet Controller

The Intel® 82579LM Gigabit Ethernet Controller supports the following features:

- 10/100/1000 BASE-T IEEE 802.3 compliant
- Energy Efficient Ethernet (EEE) IEEE802.3az support [Low Power Idle (LPI) mode]
- Dual interconnect between the Integrated LAN Controller and the Physical Layer (PHY):
  - PCI Express*-based interface for active state operation (S0) state
  - SMBUS* for host and management traffic (Sx low power state)
- Compliant to IEEE 802.3x flow control support

- 802.1p and 802.1q
- TCP, IP, and UDP checksum offload (for IPv4 and IPv6)
- Full device driver compatibility

2.10.3 LAN Subsystem Software

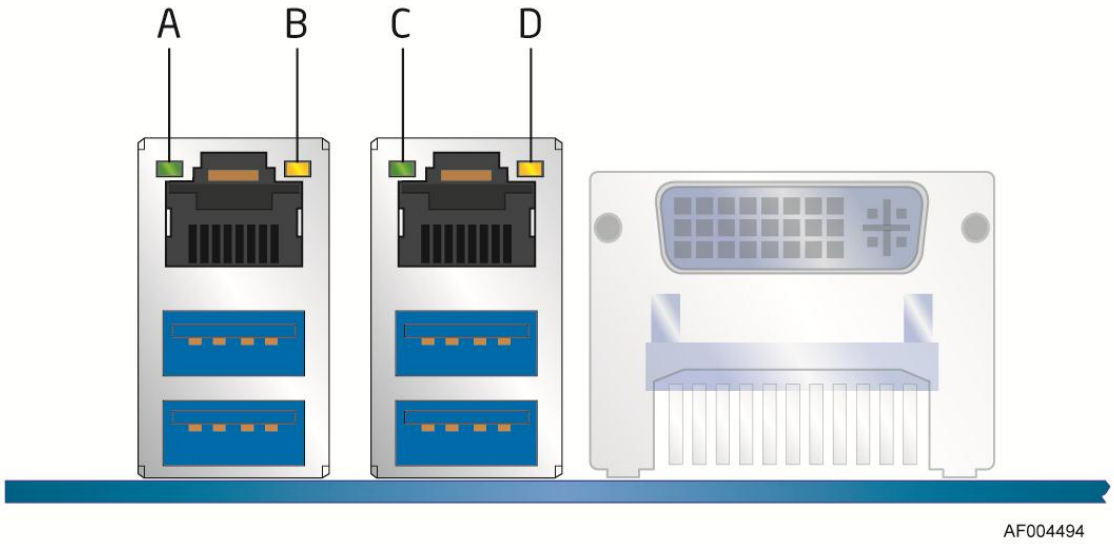
LAN software and drivers are available from Intel®'s World Wide Web site.

Table 13. Information on Obtaining LAN Software and Drivers

For information about	Refer to
Obtaining LAN software and drivers	http://downloadcenter.intel.com

2.10.4 RJ-45 LAN Connector with Integrated LEDs

Two LEDs are built into the RJ-45 LAN connector (shown in Figure 4).



Item	Description
A	Link LED (Green)
B	Data Rate LED (Green/Yellow)
C	Link LED (Green)
D	Data Rate LED (Green/Yellow)

Figure 4. LAN Connector LED Locations

Table 14 describes the LED states when the board is powered up and the LAN subsystem is operating.

Table 14. LAN Connector LED States

LED	LED Color	LED State	Condition
Link	Green	Off	LAN link is not established.
		On	LAN link is established.
		Blinking	LAN activity is occurring.
Data Rate	Green/Yellow	Off	10 Mbits/s data rate is selected.
		Green	100 Mbits/s data rate is selected.
		Yellow	1000 Mbits/s data rate is selected.

2.11 Hardware Management Subsystem

The hardware management features enable the board to be compatible with the Wired for Management (WfM) specification. The board has several hardware management features, including the following:

- Thermal and voltage monitoring
- Chassis intrusion detection

2.11.1 Hardware Monitoring

The hardware monitoring and fan control subsystem is based on the Nuvoton W83677HG-i device, which supports the following:

- Processor and system ambient temperature monitoring
- Chassis fan speed monitoring
- Power monitoring of +12 V, +5 V, V_SM, +3.3 V, and +VCCP
- SMBus* interface

2.11.2 Fan Monitoring

Fan monitoring can be implemented using third-party software.

Table 15. Information on the Function of the Fan Headers

For information about	Refer to
The functions of the fan headers	Section 2.12.2.2, page 22

2.11.3 Chassis Intrusion and Detection

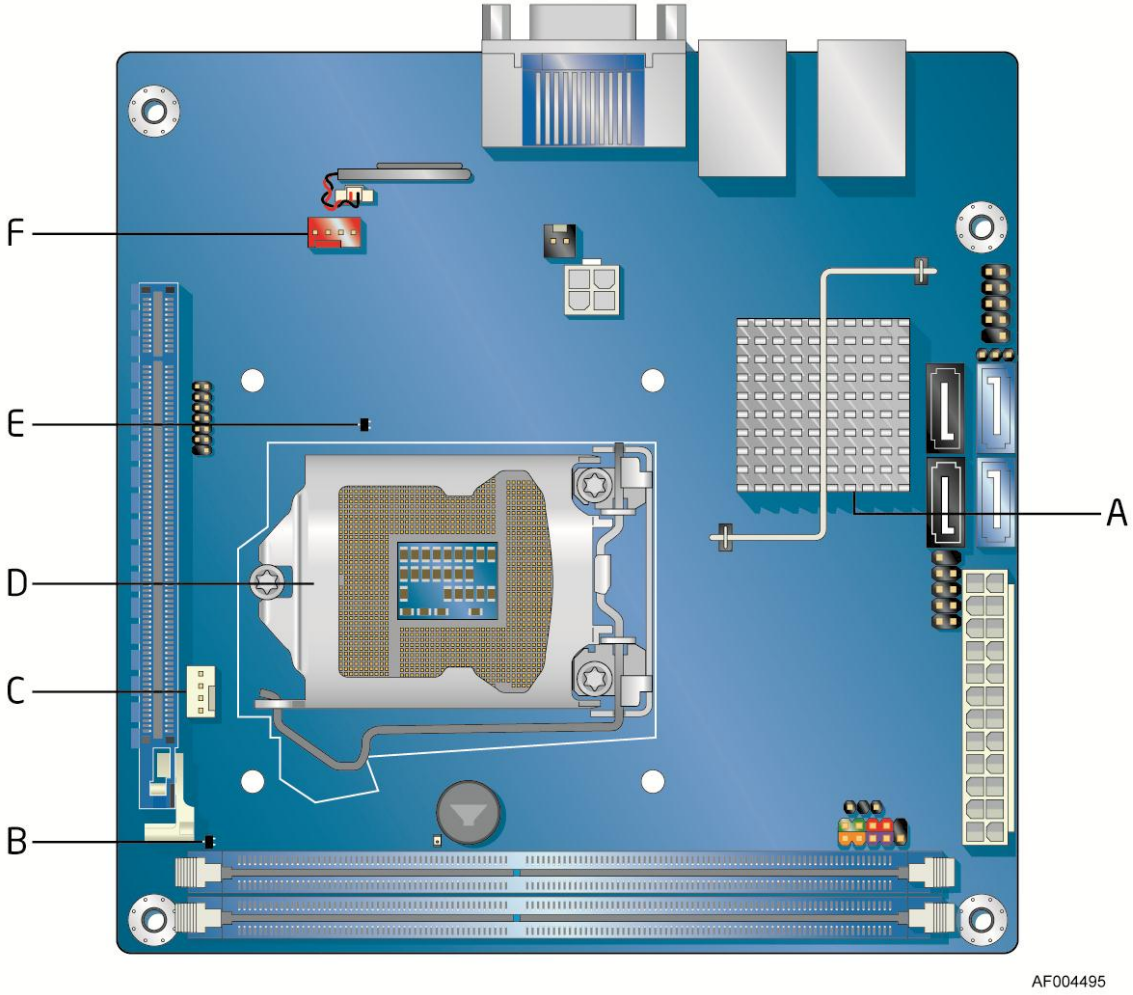
The board supports a chassis security feature that detects if the chassis cover is removed. The security feature uses a mechanical switch on the chassis that attaches to the chassis intrusion header. When the chassis cover is removed, the mechanical switch is in the closed position.

Table 16. Information on the Chassis Intrusion Headers

For information about	Refer to
The location of the chassis intrusion header	Figure 9, page 31

2.11.4 Thermal Monitoring

Figure 5 shows the locations of the thermal sensors and fan headers.



Item	Description
A	Thermal diode, located on the Intel® C206 PCH
B	Remote thermal diode 1
C	Processor fan header
D	Thermal diode, located on the processor die
E	Remote thermal diode 2
F	System fan header

Figure 5. Thermal Sensors and Fan Headers

2.12 Power Management

Power management is implemented at several levels, including:

- Software support through Advanced Configuration and Power Interface (ACPI)
- Hardware support:
  - Power connector
  - Fan headers
  - LAN wake capabilities
  - Instantly Available PC technology
  - Wake from USB
  - PCI Express* WAKE# signal support

2.12.1 ACPI

ACPI gives the operating system direct control over the power management and Plug and Play functions of a computer. The use of ACPI with this board requires an operating system that provides full ACPI support. ACPI features include:

- Plug and Play (including bus and device enumeration)
- Power management control of individual devices, add-in boards (some add-in boards may require an ACPI-aware driver), video displays, and hard disk drives
- Methods for achieving less than 15-watt system operation in the power-on/standby sleeping state
- A Soft-off feature that enables the operating system to power-off the computer
- Support for multiple wake-up events (see Table 19 on page 21)
- Support for a front panel power and sleep mode switch

Table 17 lists the system states based on how long the power switch is pressed, depending on how ACPI is configured with an ACPI-aware operating system.

Table 17. Effects of Pressing the Power Switch

System Status	Power Switch Press Time	State of the System
Off (ACPI G2/G5 – Soft off)	Less than four seconds	Power-on (ACPI G0 – working state)
On (ACPI G0 – working state)	Less than four seconds	Soft-off/Standby (ACPI G1 – sleeping state)
On (ACPI G0 – working state)	More than six seconds	Fail safe power-off (ACPI G2/G5 – Soft off)
Sleep (ACPI G1 – sleeping state)	Less than four seconds	Wake-up (ACPI G0 – working state)
Sleep (ACPI G1 – sleeping state)	More than six seconds	Power-off (ACPI G2/G5 – Soft off)

2.12.1.1 System States and Power States

Under ACPI, the operating system directs all system and device power state transitions. The operating system puts devices in and out of low-power states based on user preferences and knowledge of how devices are being used by applications. Devices that are not being used can

be turned off. The operating system uses information from applications and user settings to put the system as a whole into a low-power state.

Table 18 lists the power states supported by the board along with the associated system power targets. See the ACPI specification for a complete description of the various system and power states.

Table 18. Power States and Targeted System Power

Global States	Sleeping States	Processor States	Device States	Targeted System Power (Note 1)
G0 – working state	S0 – working	C0 – working	D0 – working state.	Full power > 30 W
G1 – sleeping state	S3 – Suspend to RAM. Context saved to RAM.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G1 – sleeping state	S4 – Suspend to disk. Context saved to disk.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G2/S5	S5 – Soft off. Context not saved. Cold boot is required.	No power	D3 – no power except for wake-up logic.	Power < 5 W (Note 2)
G3 – mechanical off AC power is disconnected from the computer.	No power to the system.	No power	D3 – no power for wake-up logic, except when provided by battery or external source.	No power to the system. Service can be performed safely.

Notes:

1. Total system power is dependent on the system configuration, including add-in boards and peripherals powered by the system chassis' power supply.
2. Dependent on the standby power consumption of wake-up devices used in the system.

2.12.1.2 Wake-up Devices and Events

Table 19 lists the devices or specific events that can wake the computer from specific states.

Table 19. Wake-up Devices and Events

These devices/events can wake up the computer...	...from this state
Power switch	S3, S4, S5 (Note 1)
RTC alarm	S3, S4, S5 (Note 1)
LAN	S3, S4, S5 (Note 1)
USB	S3
WAKE#	S3, S4, S5 (Note 1)

Notes:

1. S4 implies operating system support only.
2. Wake from S4 and S5 is recommended by Microsoft.

Note: The use of these wake-up events from an ACPI state requires an operating system that provides full ACPI support. In addition, software, drivers, and peripherals must fully support ACPI wake events.

2.12.2 Hardware Support

CAUTION

Ensure that the power supply provides adequate +5 V standby current if LAN wake capabilities and Instantly Available PC technology features are used. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

The board provides several power management hardware features, including:

- Power connector
- Fan headers
- LAN wake capabilities
- Instantly Available PC technology
- Wake from USB
- WAKE# signal wake-up support
- +5 V Standby Power Indicator LED

LAN wake capabilities and Instantly Available PC technology require power from the +5 V standby line.

Note: The use of Wake from USB from an ACPI state requires an operating system that provides full ACPI support.

2.12.2.1 Power Connector

ATX12V-compliant power supplies can turn off the system power through system control. When an ACPI-enabled system receives the correct command, the power supply removes all non-standby voltages.

When resuming from an AC power failure, the computer returns to the power state it was in before power was interrupted (on or off). The computer's response can be set using the Last Power State feature in the BIOS Setup program's Boot menu.

Table 20. Information on Power Connector Locations

For information about	Refer to
The location of the main power connector	Figure 9, page 31
The signal names of the main power connector	Table 29, page 33

2.12.2.2 Fan Headers

The function/operation of the fan headers is as follows:

- The fans are on when the board is in the S0 state
- The fans are off when the board is off or in the S3, S4, or S5 state

- Each fan header is wired to a fan tachometer input of the hardware monitoring and fan control ASIC
- All fan headers support closed-loop fan control that can adjust the fan speed or switch the fan on or off as needed
- All fan headers have a +12 V DC connection
- 4-pin fan headers are controlled by Pulse Width Modulation

Table 21. Information of the Fan Headers' Locations

For information about	Refer to
The location of the fan headers	Figure 9, page 31
The location of the fan headers and sensors for thermal monitoring	Figure 5, page 19

2.12.2.3 LAN Wake Capabilities

CAUTION

For LAN wake capabilities, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing LAN wake capabilities can damage the power supply.

LAN wake capabilities enable remote wake-up of the computer through a network. The LAN subsystem PCI bus network adapter monitors network traffic at the Media Independent Interface. Upon detecting a Magic Packet* frame, the LAN subsystem asserts a wake-up signal that powers up the computer. Depending on the LAN implementation, the board supports LAN wake capabilities with ACPI in the following ways:

- The PCI Express* WAKE# signal
- The onboard LAN subsystem

2.12.2.4 Instantly Available PC Technology

CAUTION

For Instantly Available PC technology, the +5 V standby line for the power supply must be capable of providing adequate +5 V standby current. Failure to provide adequate standby current when implementing Instantly Available PC technology can damage the power supply.

Instantly Available PC technology enables the board to enter the ACPI S3 (Suspend-to-RAM) sleep-state. While in the S3 sleep-state, the computer will appear to be off (the power supply is off, and the front panel LED is amber if dual colored, or off if single colored.) When signaled by a wake-up device or event, the system quickly returns to its last known wake state. Table 19 on page 21 lists the devices and events that can wake the computer from the S3 state.

The use of Instantly Available PC technology requires operating system support and PCI Express* add-in cards and drivers.

2.12.2.5 Wake from USB

USB bus activity wakes the computer from an ACPI S3 state.

Note: Wake from USB requires the use of a USB peripheral that supports Wake from USB.

2.12.2.6 WAKE# Signal Wake-up Support

When the WAKE# signal on the PCI Express* bus is asserted, the computer wakes from an ACPI S3, S4, or S5 state.

2.12.2.7 Wake from S5

When the RTC Date and Time is set in the BIOS, the computer will automatically wake from an ACPI S5 state.

2.12.2.8 +5 V Standby Power Indicator LED

The +5 V standby power indicator LED shows that power is still present even when the computer appears to be off. Figure 6 shows the location of the standby power LED.

CAUTION

If AC power has been switched off and the standby power indicator is still lit, disconnect the power cord before installing or removing any devices connected to the board. Failure to do so could damage the board and any attached devices.

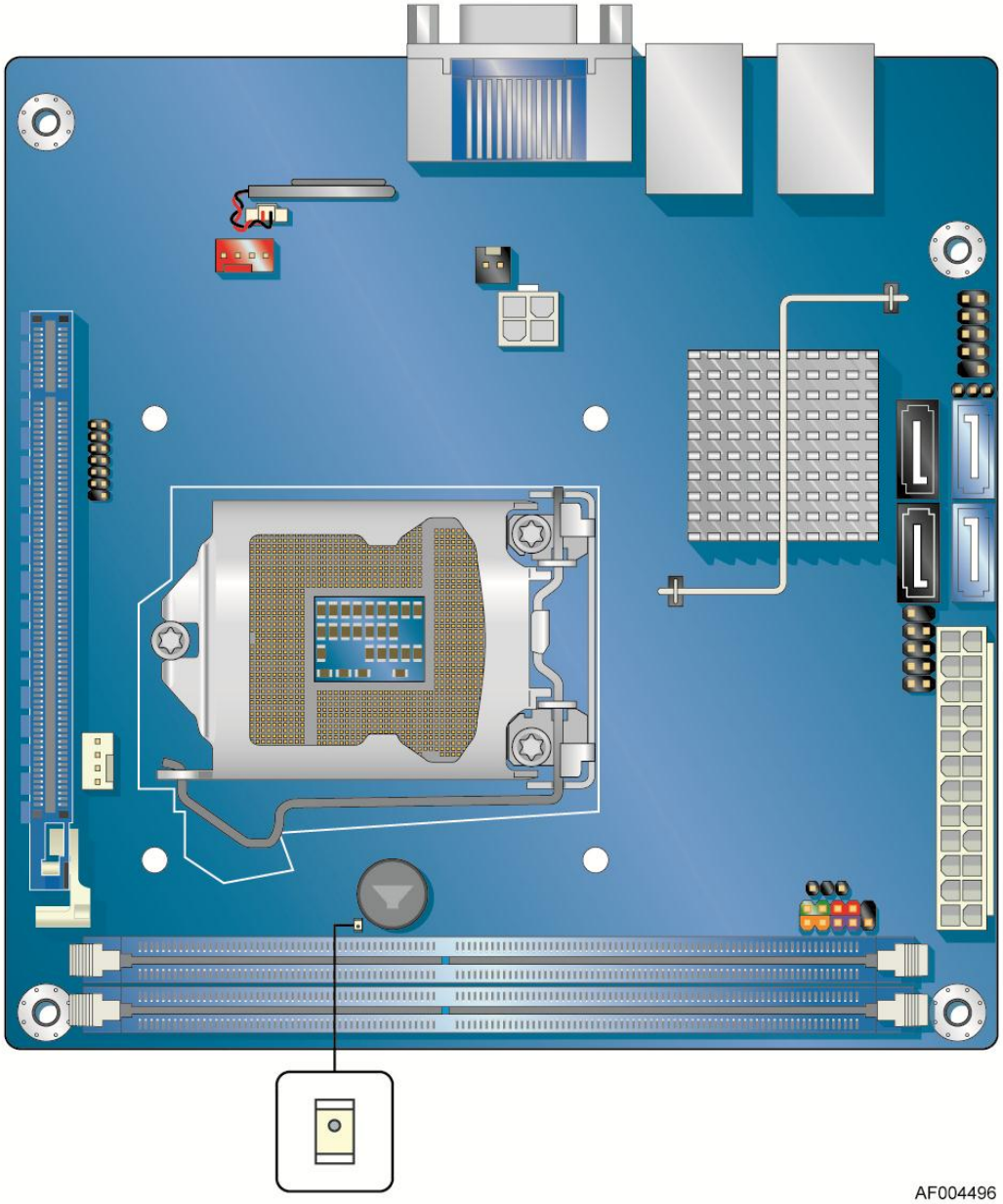


Figure 6. Location of the Standby Power LED

3. Technical Reference

3.1 Memory Resources

3.1.1 Addressable Memory

The board utilizes 16 GB of addressable system memory. Typically the address space that is allocated for PCI Conventional bus add-in cards, PCI Express* configuration space, BIOS (SPI Flash device), and chipset overhead resides above the top of DRAM (total system memory). On a system that has 16 GB of system memory installed, it is not possible to use all of the installed memory due to system address space being allocated for other system critical functions. These functions include the following:

- BIOS/SPI Flash device (16 Mbit)
- Local APIC (19 MB)
- Direct Media Interface (40 MB)
- Front side bus interrupts (17 MB)
- PCI Express* configuration space (256 MB)
- PCH base address registers PCI Express* ports (up to 256 MB)
- Memory-mapped I/O that is dynamically allocated for PCI Express* add-in cards (256 MB)

The board provides the capability to reclaim the physical memory overlapped by the memory mapped I/O logical address space. The board remaps physical memory from the top of usable DRAM boundary to the 4 GB boundary to an equivalent sized logical address range located just above the 4 GB boundary. Figure 7 shows a schematic of the system memory map. All installed system memory can be used when there is no overlap of system addresses.

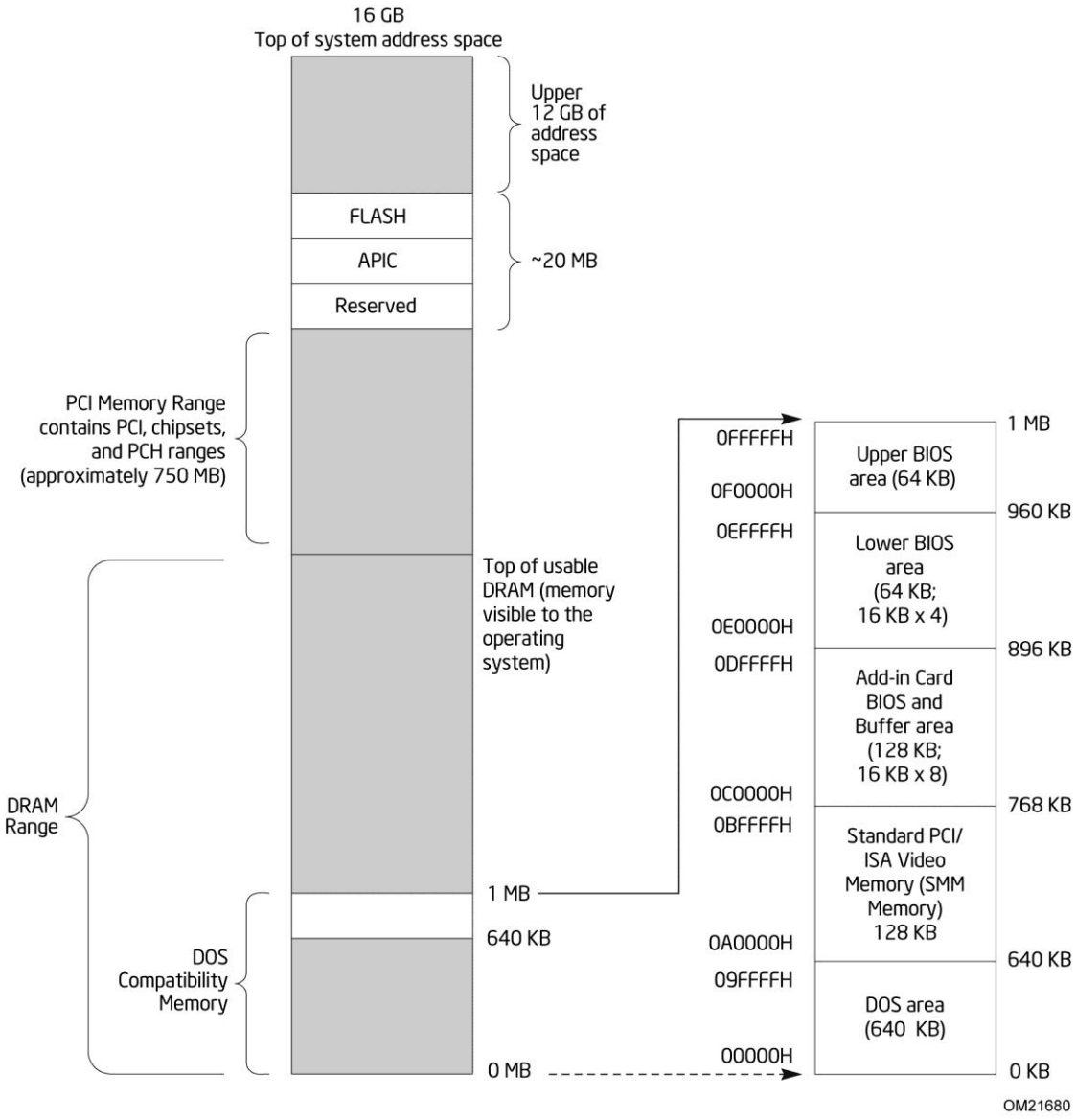


Figure 7. Detailed System Memory Address Map

3.1.2 Memory Map

Table 22 lists the system memory map.

Table 22. System Memory Map

Address Range (decimal)	Address Range (hex)	Size	Description
1024 K - 16777216K K	100000 – 400000000	16382 MB	Extended memory
960 K - 1024 K	F0000 - FFFFF	64 KB	Runtime BIOS
896 K - 960 K	E0000 - EFFFF	64 KB	Reserved
800 K - 896 K	C8000 - DFFFF	96 KB	Potential available high DOS memory (open to the PCI Conventional bus). Dependent on video adapter used.
640 K - 800 K	A0000 - C7FFF	160 KB	Video memory and BIOS
639 K - 640 K	9FC00 - 9FFFF	1 KB	Extended BIOS data (movable by memory manager software)
512 K - 639 K	80000 - 9FBFF	127 KB	Extended conventional memory
0 K - 512 K	00000 - 7FFFF	512 KB	Conventional memory

3.2 Connectors and Headers

CAUTION

Only the following connectors and headers have over-current protection: back panel and front panel USB.

The other internal connectors and headers are not over-current protected and should connect only to devices inside the computer's chassis, such as fans and internal peripherals. Do not use these connectors or headers to power devices external to the computer's chassis. A fault in the load presented by the external devices could cause damage to the computer, the power cable, and the external devices themselves.

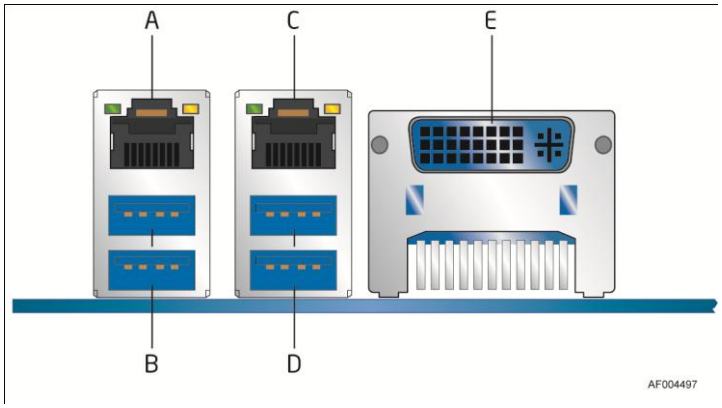
Furthermore, improper connection of USB header single wire connectors may eventually overload the over-current protection and cause damage to the board.

This section describes the board's connectors. The connectors can be divided into these groups:

- Back panel I/O connectors
- Component-side I/O connectors and headers (see page 30)

3.2.1 Back Panel Connectors

Figure 8 shows the location of the back panel connectors for the board.



Item	Description
A	LAN port (82574L)
B	USB 2.0 ports
C	LAN port (82579LM)
D	USB 2.0 ports
E	DVI-I connector

Figure 8. Back Panel Connectors

3.2.2 Component-side Connectors and Headers

Figure 9 shows the locations of the component-side connectors and headers.

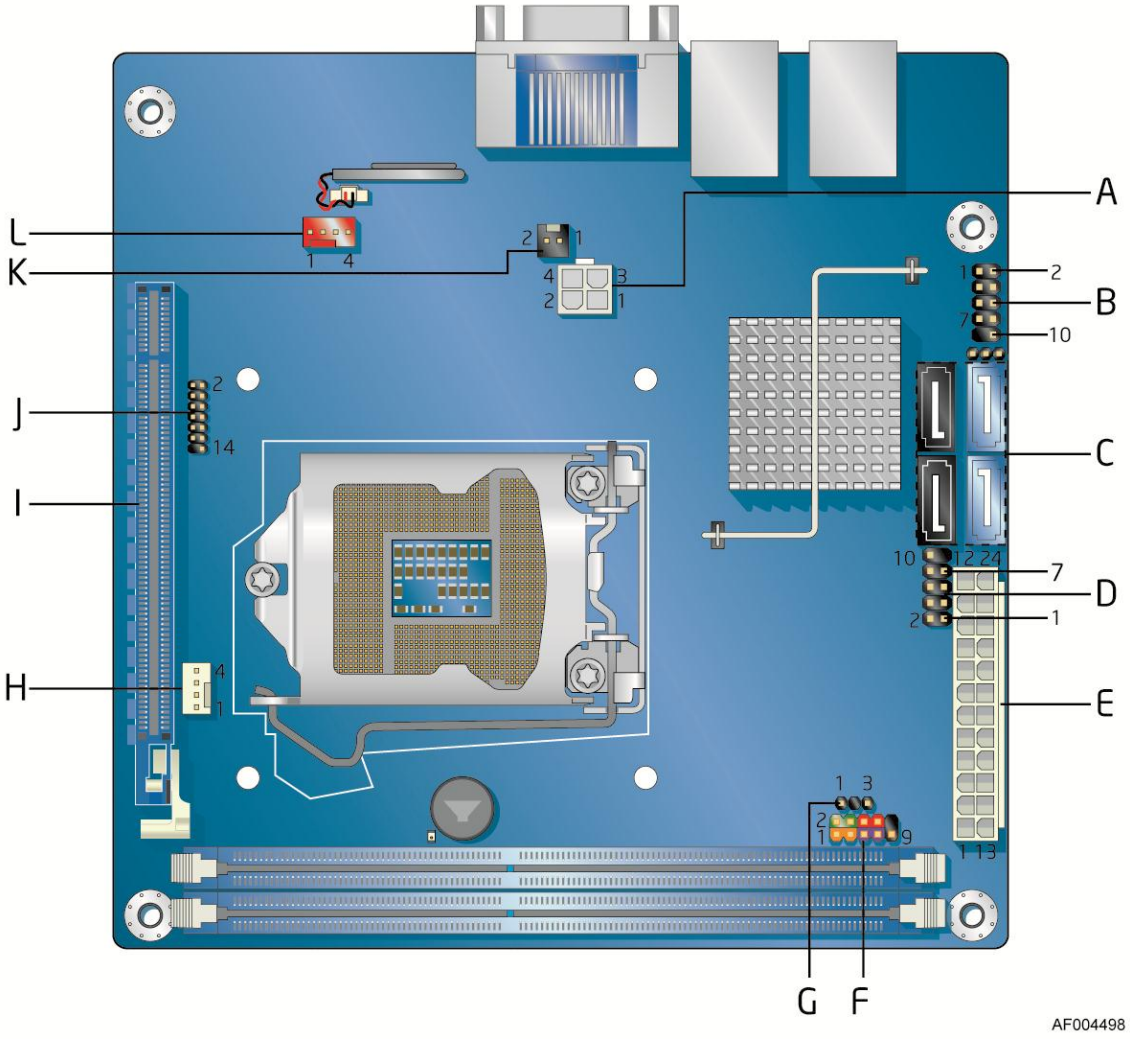


Figure 9. Component-side Connectors and Headers

Table 23 lists the component-side connectors and headers identified in Figure 9.

Table 23. Component-side Connectors and Headers Shown in Figure 9

Item/callout	Description
A	Processor core power connector (2 x 2)
B	Front panel USB header
C	SATA connectors
D	Front panel USB header
E	Main power connector (2 X 12)
F	Front panel header
G	Alternate front panel power LED header
H	Processor fan header
I	PCI Express* x16 bus add-in card connector
J	LPC Debug header
K	Chassis intrusion header
L	System fan header

3.2.2.1 Signal Tables for the Connectors and Headers

Table 24. Front Panel USB 2.0 Headers

Pin	Signal Name	Pin	Signal Name
1	+5 V DC	2	+5 V DC
3	D-	4	D-
5	D+	6	D+
7	Ground	8	Ground
9	KEY (no pin)	10	No Connect

Table 25. SATA Connectors

Pin	Signal Name
1	Ground
2	TXP
3	TXN
4	Ground
5	RXN
6	RXP
7	Ground

Table 26. Chassis Intrusion Header

Pin	Signal Name
1	Intruder#
2	Ground

Table 27. Processor and System (4-Pin) Fan Headers

Pin	Signal Name
1	Ground (Note)
2	+12 V
3	FAN_TACH
4	FAN_CONTROL
5	Jack detect 2

Note: These fan headers use Pulse Width Modulation control for fan speed.

3.2.2.2 Add-in Card Connector

The board has one PCI Express* 2.0 x16 (with Intel® Xeon® E3-1200 Processors or the 2nd Generation Intel® Core™ i3 Processors) or PCI Express* 3.0 x 16 (with Intel® Xeon® E3-1200 V2 Processors or the 3rd Generation Intel® Core™ i3 Processors) connector supporting simultaneous transfer speeds up to 16 GB/s of peak bandwidth per direction and up to 32 GB/s concurrent bandwidth.

3.2.2.3 Power Supply Connectors

The board has the following power supply connectors:

- **Main power** – a 2 x 12 connector. The board supports the use of ATX12V power supplies with either 2 x 10 or 2 x 12 main power cables. When using a power supply with a 2 x 10 main power cable, attach that cable on the leftmost pins of the main power connector, leaving pins 11, 12, 23, and 24 unconnected.
- **Processor core power** – a 2 x 2 connector. This connector provides power directly to the processor voltage regulator and must always be used. Failure to do so will prevent the board from booting.

Table 28. Processor Core Power Connector

Pin	Signal Name	Pin	Signal Name
1	Ground	2	Ground
3	+12 V	4	+12 V

Table 29. Main Power Connector

Pin	Signal Name	Pin	Signal Name
1	+3.3 V	13	+3.3 V
2	+3.3 V	14	-12 V

Pin	Signal Name	Pin	Signal Name
3	Ground	15	Ground
4	+5 V	16	PS-ON# (power supply remote on/off)
5	Ground	17	Ground
6	+5 V	18	Ground
7	Ground	19	Ground
8	PWRGD (Power Good)	20	No connect
9	+5 V (Standby)	21	+5 V
10	+12 V	22	+5 V
11	+12 V (Note)	23	+5 V (Note)
12	2 x 12 connector detect (Note)	24	Ground (Note)

Note: When using a 2 x 10 power supply cable, this pin will be unconnected.

For information about	Refer to
Power supply considerations	Section 3.5.1 on page 40

3.2.2.4 Front Panel Header

This section describes the functions of the front panel header. Table 30 lists the signal names of the front panel header. Figure 10 is a connection diagram for the front panel header.

Table 30. Front Panel Header

Pin	Signal Name	Description	Pin	Signal Name	Description
1	HDD_POWER_LED	Pull-up resistor (750 Ω) to +5V	2	POWER_LED_MAIN	[Out] Front panel LED (main color)
3	HDD_LED#	[Out] Hard disk activity LED	4	POWER_LED_ALT	[Out] Front panel LED (alt color)
5	GROUND	Ground	6	POWER_SWITCH#	[In] Power switch
7	RESET_SWITCH#	[In] Reset switch	8	GROUND	Ground
9	+5V_DC	Power	10	Key	No pin

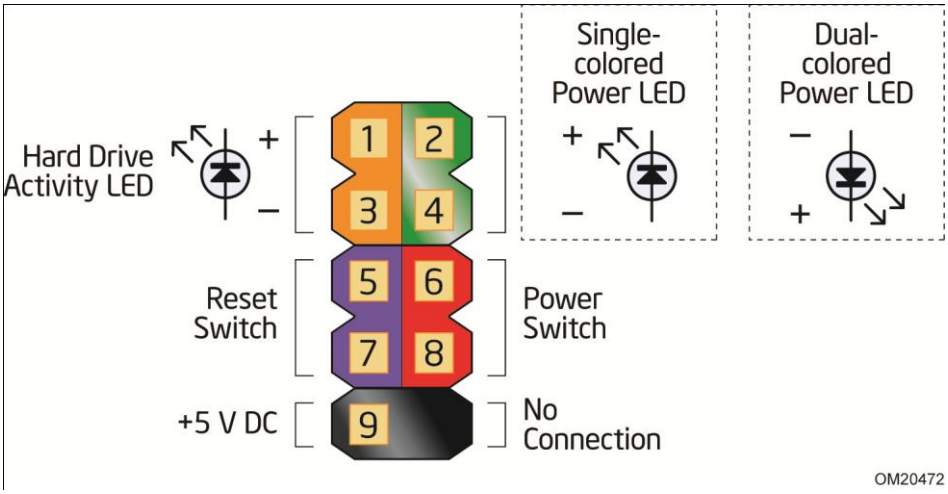


Figure 10. Connection Diagram for Front Panel Header

3.2.2.4.1 Hard Drive Activity LED Header

Pins 1 and 3 can be connected to an LED to provide a visual indicator that data is being read from or written to a hard drive. Proper LED function requires a SATA hard drive or optical drive connected to an onboard SATA connector.

3.2.2.4.2 Reset Switch Header

Pins 5 and 7 can be connected to a momentary single pole, single throw (SPST) type switch that is normally open. When the switch is closed, the board resets and runs the POST.

3.2.2.4.3 Power/Sleep LED Header

Pins 2 and 4 can be connected to a one- or two-color LED. Table 31 shows the possible states for a one-color LED. Table 32 shows the possible states for a two-color LED.

Table 31. States for a One-Color Power LED

LED State	Description
Off	Power off/sleeping
Steady Green	Running

Table 32. States for a Two-Color Power LED

LED State	Description
Off	Power off
Steady Green	Running
Steady Yellow	Sleeping

Note: The colors listed in Table 31 and Table 32 are suggested colors only. Actual LED colors are chassis-specific.

3.2.2.4.4 Power Switch Header

Pins 6 and 8 can be connected to a front panel momentary-contact power switch. The switch must pull the SW_ON# pin to ground for at least 50 ms to signal the power supply to switch on or off. (The time requirement is due to internal debounce circuitry on the board.) At least two seconds must pass before the power supply will recognize another on/off signal.

3.2.2.5 Alternate Front Panel Power/Sleep LED Header

Pins 1 and 3 of this header duplicate the signals on pins 2 and 4 of the front panel header.

Table 33. Alternate Front Panel Power/Sleep LED Header

Pin	Signal Name	Description
1	POWER_LED_MAIN	[Out] Front panel LED (main color)
2	Key (no pin)	
3	POWER_LED_ALT	[Out] Front panel LED (alt color)

3.2.2.6 Front Panel USB 2.0 Headers

Figure 11 is a connection diagram for the front panel USB 2.0 headers.

Note: The +5 V DC power on the USB headers is fused. Use only a front panel USB connector that conforms to the USB 2.0 specification for high-speed USB devices.

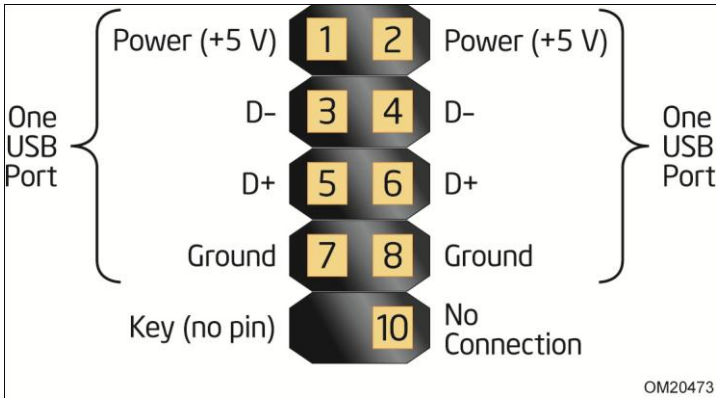


Figure 11. Connection Diagram for Front Panel USB 2.0 Headers

3.2.2.7 Low Pin Count (LPC) Debug header

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires a POST card that can interface with the Low Pin Count (LPC) Debug header. The POST card can decode the port and display the contents on a medium such as a seven-segment display.

Table 34. LPC Debug Header

Pin	Signal Name	Pin	Signal Name
1	CK_33M_DEBUG	2	GND
3	PLTRST#	4	LFRAME#
5	LAD0	6	LAD1
7	LAD2	8	LAD3
9	GND	10	GND
11	+3.3 V	12	+3.3 V
13	Not Connected	14	+3.3 V

3.3 Jumper Block

CAUTION

Do not move the jumper with the power on. Always turn off the power and unplug the power cord from the computer before changing a jumper setting. Otherwise, the board could be damaged.

Figure 12 shows the location of the jumper block. The 3-pin jumper block determines the BIOS Setup program's mode. Table 35 describes the jumper settings for the three modes: normal, configure, and recovery. When the jumper is set to configure mode and the computer is powered-up, the BIOS compares the processor version and the microcode version in the BIOS and reports if the two match.

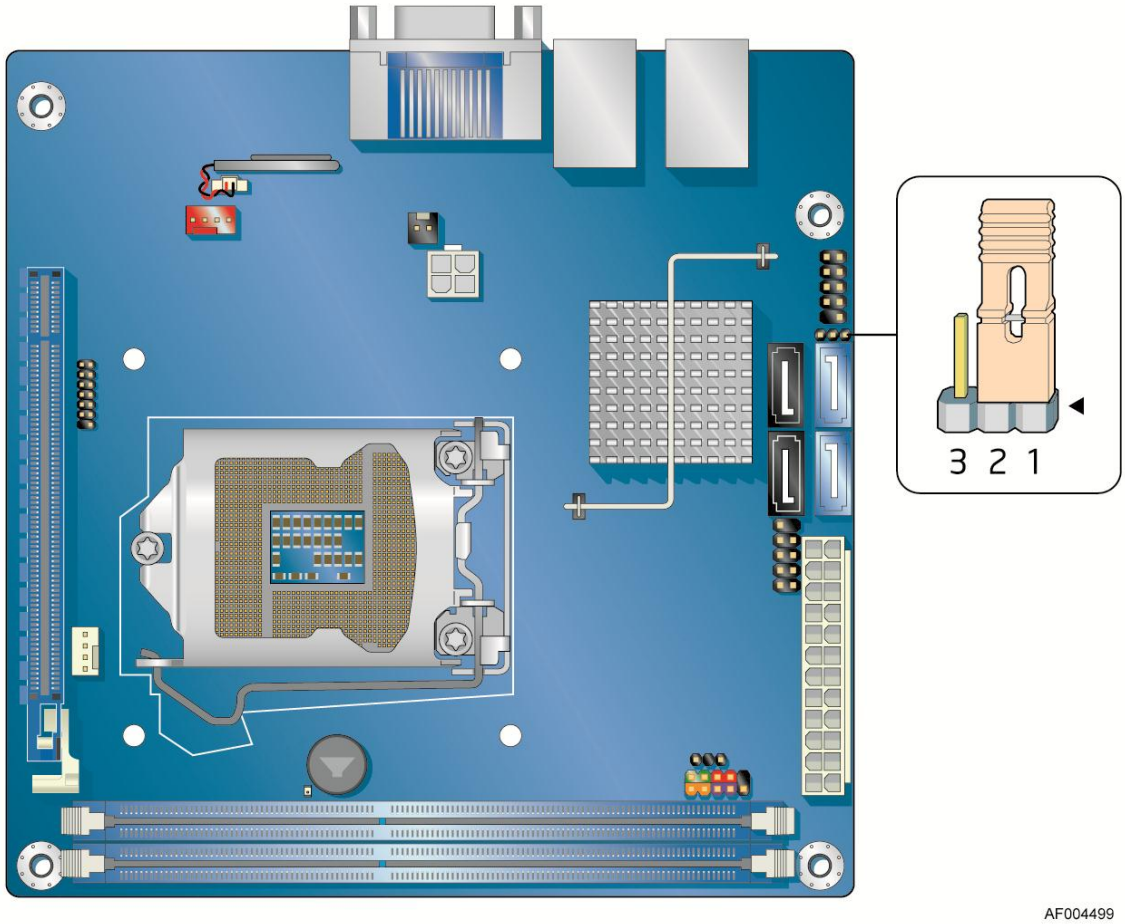
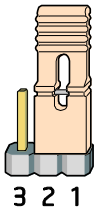
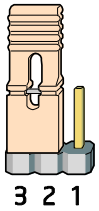
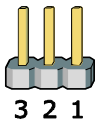


Figure 12. Location of the Jumper Block

Table 35. BIOS Setup Configuration Jumper Settings

Function/Mode	Jumper Setting		Configuration
Normal	1-2		The BIOS uses current configuration information and passwords for booting.
Configure	2-3		After the POST runs, Setup runs automatically. The maintenance menu is displayed. Note that this Configure mode is the only way to clear the BIOS/CMOS settings. Press F9 (restore defaults) while in Configure mode to restore the BIOS/CMOS settings to their default values.
Recovery	None		The BIOS attempts to recover the BIOS configuration. A recovery CD or flash drive is required.

3.4 Mechanical Considerations

3.4.1 Form Factor

The board is designed to fit into a Mini-ITX form-factor chassis. Figure 13 illustrates the mechanical form factor for the board. Dimensions are given in inches [millimeters]. The outer dimensions are 6.7 inches by 6.7 inches [170.18 millimeters by 170.18 millimeters]. Location of the I/O connectors and mounting holes are in compliance with the ATX specification.

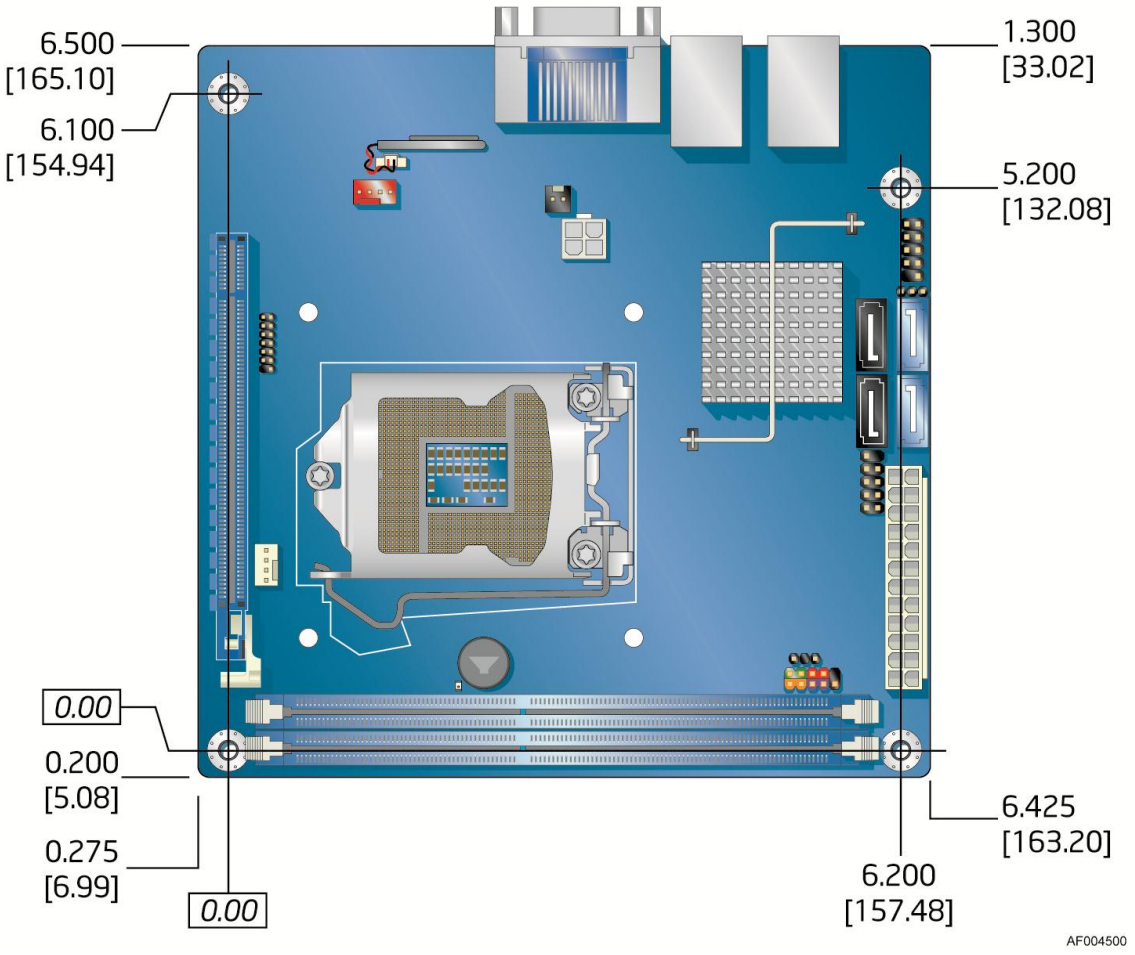


Figure 13. Board Dimensions

3.5 Electrical Considerations

3.5.1 Power Supply Considerations

CAUTION

The +5 V standby line from the power supply must be capable of providing adequate +5 V standby current. Failure to do so can damage the power supply. The total amount of standby current required depends on the wake devices supported and manufacturing options.

Additional power required will depend on configurations chosen by the integrator.

The power supply must comply with the indicated parameters of the ATX form factor specification.

- The potential relation between 3.3 V DC and +5 V DC power rails
- The current capability of the +5 VSB line

- All timing parameters
- All voltage tolerances

For example, for a system consisting of a supported 95 W processor (see Section 2.3 on page 8 for a list of supported processors), 1 GB DDR3 RAM, one high end video card, one hard disk drive, one optical drive, and all board peripherals enabled, the minimum recommended power supply is 350 W. Table 36 lists the recommended power supply current values.

Table 36. Recommended Power Supply Current Values

Output Voltage	3.3 V	5 V	12 V1	12 V2	-12 V	5 VSB
Current	17 A	18 A	12 A	18 A	0.8 A	2 A

3.5.2 Fan Header Current Capability

CAUTION

The processor fan must be connected to the processor fan header, not to a chassis fan header. Connecting the processor fan to a chassis fan header may result in onboard component damage that will halt fan operation.

Table 37 lists the current capability of the fan headers.

Table 37. Fan Header Current Capability

Fan Header	Maximum Available Current
Processor fan	2.0 A
System fan	1.5 A

3.5.3 Add-in Board Considerations

The board is designed to provide 2 A (average) of current for each add-in board from the +5 V rail. The total +5 V current draw for add-in boards for a fully loaded board (one expansion slot filled) must not exceed the system's power supply +5 V maximum current or 14 A in total.

3.6 Thermal Considerations

CAUTION

A chassis with a maximum internal ambient temperature of 38º C at the processor fan inlet is a requirement. Use a processor heat sink that provides omni-directional airflow to maintain required airflow across the processor voltage regulator area.

CAUTION

Failure to ensure appropriate airflow may result in reduced performance of both the processor and/or voltage regulator or, in some instances, damage to the board. For a list of chassis that have been tested with Intel® server boards please refer to the product support web page.

All responsibility for determining the adequacy of any thermal or system design remains solely with the reader. Intel® makes no warranties or representations that merely following the instructions presented in this document will result in a system with adequate thermal performance.

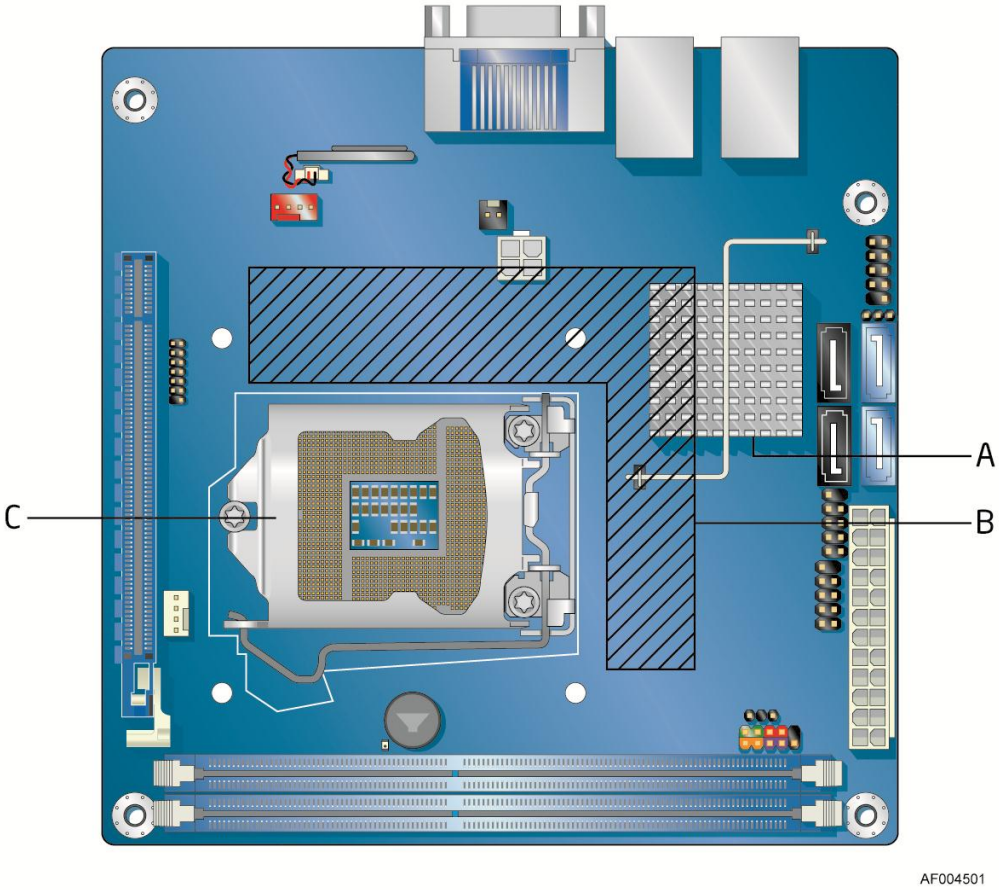
CAUTION

Ensure that the ambient temperature does not exceed the board's maximum operating temperature. Failure to do so could cause components to exceed their maximum case temperature and malfunction. For information about the maximum operating temperature, see the environmental specifications in Section 3.8.

CAUTION

Ensure that proper airflow is maintained in the processor voltage regulator circuit. Failure to do so may result in damage to the voltage regulator circuit. The processor voltage regulator area (shown in Figure 14) can reach a temperature of up to 120 C in an open chassis.

Figure 14 shows the locations of the localized high temperature zones.



Item	Description
A	Intel® C206 Chipset
B	Processor voltage regulator area
C	Processor

Figure 14. Localized High Temperature Zones

Table 38 provides maximum case temperatures for the components that are sensitive to thermal changes. The operating temperature, current load, or operating frequency could affect case temperatures. Maximum case temperatures are important when considering proper airflow to cool the board.

Table 38. Thermal Considerations for Components

Component	Maximum Case Temperature
Processor	For processor case temperature, see processor datasheets and processor specification updates
Intel® C206 Express Chipset	104°C

To ensure functionality and reliability, the component is specified for proper operation when Case Temperature is maintained at or below the maximum temperature listed in Table 39. This is a requirement for sustained power dissipation equal to Thermal Design Power (TDP is specified as the maximum sustainable power to be dissipated by the components). When the component is dissipating less than TDP, the case temperature should be below the Maximum Case Temperature. The surface temperature at the geometric center of the component corresponds to Case Temperature.

It is important to note that the temperature measurement in the system BIOS is a value reported by embedded thermal sensors in the components and does not directly correspond to the Maximum Case Temperature. The upper operating limit when monitoring this thermal sensor is Tcontrol.

Table 39. Tcontrol Values for Components

Component	Tcontrol
Processor	For processor case temperature, see processor datasheets and processor specification updates
Intel® C206 Express Chipset	104°C

3.7 Reliability

The Mean Time Between Failures (MTBF) prediction is calculated using component and subassembly random failure rates. The calculation is based on the Telcordia SR-332, Method I Case 1 50% electrical stress, 55 ºC ambient. The MTBF prediction is used to estimate repair rates and spare parts requirements. The MTBF data is calculated from predicted data at 55 ºC. The MTBF for the board is 255,227 hours.

3.8 Environmental

Table 40 lists the environmental specifications for the board.

Table 40. Environmental Specifications

Parameter	Specification		
Temperature			
Non-Operating	-20 °C to +70 °C		
Operating	0 °C to +55 °C		
Shock			
Unpackaged	50 g trapezoidal waveform		
	Velocity change of 170 inches/s²		
Packaged	Half sine 2 millisecond		
	Product Weight (pounds)	Free Fall (inches)	Velocity Change (inches/s²)
	<20	36	167
	21-40	30	152
	41-80	24	136
	81-100	18	118
Vibration			
Unpackaged	5 Hz to 20 Hz: 0.01 g² Hz sloping up to 0.02 g² Hz		
	20 Hz to 500 Hz: 0.02 g² Hz (flat)		
Packaged	5 Hz to 40 Hz: 0.015 g² Hz (flat)		
	40 Hz to 500 Hz: 0.015 g² Hz sloping down to 0.00015 g² Hz		

4. Overview of BIOS Features

4.1 Introduction

The board uses an Intel® BIOS that is stored in the Serial Peripheral Interface Flash Memory (SPI Flash) and can be updated using a disk-based program. The SPI Flash contains the BIOS Setup program, POST, the PCI auto-configuration utility, LAN EEPROM information, and Plug and Play support.

The BIOS displays a message during POST identifying the type of BIOS and a revision code.

When the BIOS Setup configuration jumper is set to configure mode and the computer is powered-up, the BIOS compares the CPU version and the microcode version in the BIOS and reports if the two match.

The BIOS Setup program can be used to view and change the BIOS settings for the computer. The BIOS Setup program is accessed by pressing the <F2> key after the Power-On Self-Test (POST) memory test begins and before the operating system boot begins. The menu bar is shown below.

Maintenance	**Main**	**Configuration**	**Performance**	**Security**	**Power**	**Boot**	**Exit**

Note: The maintenance menu is displayed only when the board is in configure mode. Section 3.3 on page 38 shows how to put the board in configure mode.

Table 41 lists the BIOS Setup program menu features.

Table 41. BIOS Setup Program Menu Bar

Maintenance	Main	Configuration	Performance	Security	Power	Boot	Exit
Clears passwords and displays processor information	Displays processor and memory configuration	Configures advanced features available through the chipset	Configures Processor overrides	Sets passwords and security features	Configures power management features and power supply controls	Selects boot options	Saves or discards changes to Setup program options

Table 42 lists the function keys available for menu screens.

Table 42. BIOS Setup Program Function Keys

BIOS Setup Program Function Key	Description
<←> or <→>	Selects a different menu screen (Moves the cursor left or right)
<↑> or <↓>	Selects an item (Moves the cursor up or down)
<Tab>	Selects a field (Not implemented)
<Enter>	Executes command or selects the submenu

BIOS Setup Program Function Key	Description
<F9>	Load the default configuration values for the current menu
<F10>	Save the current values and exits the BIOS Setup program
<Esc>	Exits the menu

4.2 BIOS Flash Memory Organization

The Serial Peripheral Interface Flash Memory (SPI Flash) includes a 32 Mbit (4096 KB) flash memory device.

4.3 System Management BIOS (SMBIOS)

SMBIOS is a Desktop Management Interface (DMI) compliant method for managing computers in a managed network.

The main component of SMBIOS is the Management Information Format (MIF) database, which contains information about the computing system and its components. Using SMBIOS, a system administrator can obtain the system types, capabilities, operational status, and installation dates for system components. The MIF database defines the data and provides the method for accessing this information. The BIOS enables applications such as third-party management software to use SMBIOS. The BIOS stores and reports the following SMBIOS information:

- BIOS data, such as the BIOS revision level
- Fixed-system data, such as peripherals, serial numbers, and asset tags
- Resource data, such as memory size, cache size, and processor speed
- Dynamic data, such as event detection and error logging

Non-Plug and Play operating systems require an additional interface for obtaining the SMBIOS information. The BIOS supports an SMBIOS table interface for such operating systems. Using this support, an SMBIOS service-level application running on a non-Plug and Play operating system can obtain the SMBIOS information. Additional board information can be found in the BIOS under the Additional Information header under the Main BIOS page.

4.4 Legacy USB Support

Legacy USB support enables USB devices to be used even when the operating system's USB drivers are not yet available. Legacy USB support is used to access the BIOS Setup program, and to install an operating system that supports USB. By default, Legacy USB support is set to Enabled.

Legacy USB support operates as follows:

1. When you apply power to the computer, legacy support is disabled.
2. POST begins.
3. Legacy USB support is enabled by the BIOS allowing you to use a USB keyboard to enter and configure the BIOS Setup program and the maintenance menu.
4. POST completes.

5. The operating system loads. While the operating system is loading, USB keyboards and mice are recognized and may be used to configure the operating system. (Keyboards and mice are not recognized during this period if Legacy USB support was set to Disabled in the BIOS Setup program.)
6. After the operating system loads the USB drivers, all legacy and non-legacy USB devices are recognized by the operating system, and Legacy USB support from the BIOS is no longer used.
7. Additional USB legacy feature options can be access by using Intel® Integrator Toolkit.

To install an operating system that supports USB, verify that Legacy USB support in the BIOS Setup program is set to Enabled and follow the operating system's installation instructions.

4.5 BIOS Updates

The BIOS can be updated using either of the following utilities, which are available on the Intel® World Wide Web site:

- Intel® Flash Memory Update Utility, which requires booting from DOS. Using this utility, the BIOS can be updated from a file on a hard disk, a USB drive (a flash drive or a USB hard drive), or a CD-ROM.
- Intel® F7 switch during POST allows a user to select where the BIOS .bio file is located and perform the update from that location/device. Similar to performing a BIOS Recovery without removing the BIOS configuration jumper.

Both utilities verify that the updated BIOS matches the target system to prevent accidentally installing an incompatible BIOS.

Note: Review the instructions distributed with the upgrade utility before attempting a BIOS update.

4.5.1 Language Support

The BIOS Setup program and help messages are supported in US English. Check the Intel® web site for support.

4.5.2 Custom Splash Screen

During POST, an Intel® splash screen is displayed by default. This splash screen can be augmented with a custom splash screen. The Intel® Integrator's Toolkit that is available from Intel® can be used to create a custom splash screen.

Note: If you add a custom splash screen, it will share space with the Intel® branded logo.

Table 43. Information on Integrator Toolkit and Software Tools

For information about	Refer to
Intel® Integrator Toolkit	http://developer.intel.com/design/motherbd/software/itk/
Additional Intel® software tools	http://developer.intel.com/design/motherbd/software.htm

4.6 BIOS Recovery

It is unlikely that anything will interrupt a BIOS update; however, if an interruption occurs, the BIOS could be damaged. Table 44 lists the drives and media types that can and cannot be used for BIOS recovery. The BIOS recovery media does not need to be made bootable.

Table 44. Acceptable Drives/Media Types for BIOS Recovery

Media Type	Can be used for BIOS recovery?
CD-ROM drive connected to the SATA interface	Yes
USB removable drive (a USB Flash Drive, for example)	Yes
USB diskette drive (with a 1.44 MB diskette)	No
USB hard disk drive	No

4.6.1 Recovery with USB Thumb Drive or CD-ROM

1. Download and save the Recovery BIOS file to a temporary directory.
2. Copy the recovery file (*.BIO) to a USB thumb drive or a CD.
3. Plug the thumb drive into a USB port of the target computer, or place the CD in the CD-ROM drive of the target computer.
4. Shut down the computer and unplug the AC power adapter.
5. Open the chassis and remove the BIOS Configuration Jumper. Please refer to section 2.3 for details including the location of this jumper.
6. Power the computer on.
7. Wait 2-5 minutes for the update to complete.
8. The computer will either turn off when the recovery process is completed or it will prompt you to turn it off.
9. Remove the thumb drive or the CD.
10. Replace the BIOS Configuration Jumper.
11. Close the chassis.
12. Restart the computer.

4.7 Boot Options

In the BIOS Setup program, the user can choose to boot from a hard drive, optical drive, removable drive, or the network. The default setting is for the optical drive to be the first boot device, the hard drive second, removable drive third, and the network fourth.

4.7.1 Optical Drive Boot

Booting from the optical drive is supported in compliance to the El Torito bootable CD-ROM format specification. Under the Boot menu in the BIOS Setup program, the optical drive is listed as a boot device. Boot devices are defined in priority order. Accordingly, if there is not a bootable CD in the optical drive, the system will attempt to boot from the next defined drive.

4.7.2 Network Boot

The network can be selected as a boot device. This selection allows booting from the onboard LAN or a network add-in card with a remote boot ROM installed.

Pressing the <F12> key during POST automatically forces booting from the LAN. To use this key during POST, the User Access Level in the BIOS Setup program's Security menu must be set to Full.

4.7.3 Booting Without Attached Devices

For use in embedded applications, the BIOS has been designed so that after passing the POST, the operating system loader is invoked even if the following devices are not present:

- Video adapter
- Keyboard
- Mouse

4.7.4 Changing the Default Boot Device During POST

Pressing the <F10> key during POST causes a boot device menu to be displayed. This menu displays the list of available boot devices. Table 45 lists the boot device menu options.

Table 45. Boot Device Menu Options

Boot Device Menu Function Keys	Description
<↑> or <↓>	Selects a default boot device
<Enter>	Exits the menu, and boots from the selected device
<Esc>	Exits the menu and boots according to the boot priority defined through BIOS setup

4.8 Adjusting Boot Speed

These factors affect system boot speed:

- Selecting and configuring peripherals properly
- Optimized BIOS boot parameters
- Enabling the new Hyperboot feature

4.8.1 Peripheral Selection and Configuration

The following techniques help improve system boot speed:

- Choose a hard drive with parameters such as “power-up to data ready” in less than eight seconds that minimizes hard drive startup delays.

- Select a CD-ROM drive with a fast initialization rate. This rate can influence POST execution time.
- Eliminate unnecessary add-in adapter features, such as logo displays, screen repaints, or mode changes in POST. These features may add time to the boot process.
- Try different monitors. Some monitors initialize and communicate with the BIOS more quickly, which enables the system to boot more quickly.

4.8.2 BIOS Boot Optimizations

Use of the following BIOS Setup program settings reduces the POST execution time.

- In the Boot Menu, set the hard disk drive as the first boot device. As a result, the POST does not first seek a diskette drive, which saves about one second from the POST execution time.
- In the Peripheral Configuration submenu, disable the LAN device if it will not be used. This can reduce up to four seconds of option ROM boot time.

Note: It is possible to optimize the boot process to the point where the system boots so quickly that the Intel® logo screen (or a custom logo splash screen) will not be seen. Monitors and hard disk drives with minimum initialization times can also contribute to a boot time that might be so fast that necessary logo screens and POST messages cannot be seen.

This boot time may be so fast that some drives might be not be initialized at all. If this condition should occur, it is possible to introduce a programmable delay ranging from zero to 30 seconds by 5 second increments (using the Hard Disk Pre-Delay feature of the Advanced Menu in the Drive Configuration Submenu of the BIOS Setup program).

4.9 BIOS Security Features

The BIOS includes security features that restrict access to the BIOS Setup program and who can boot the computer. A supervisor password and a user password can be set for the BIOS Setup program and for booting the computer, with the following restrictions:

- The supervisor password gives unrestricted access to view and change all the Setup options in the BIOS Setup program. This is the supervisor mode.
- The user password gives restricted access to view and change Setup options in the BIOS Setup program. This is the user mode.
- If only the supervisor password is set, pressing the <Enter> key at the password prompt of the BIOS Setup program allows the user restricted access to Setup.
- If both the supervisor and user passwords are set, users can enter either the supervisor password or the user password to access Setup. Users have access to Setup respective to which password is entered.
- Setting the user password restricts who can boot the computer. The password prompt will be displayed before the computer is booted. If only the supervisor password is set, the computer boots without asking for a password. If both passwords are set, the user can enter either password to boot the computer.
- For enhanced security, use different passwords for the supervisor and user passwords.
- Valid password characters are A-Z, a-z, and 0-9. Passwords may be up to 16 characters in length.

Table 46 shows the effects of setting the supervisor password and user password. This table is for reference only and is not displayed on the screen.

Table 46. Supervisor and User Password Functions

Password Set	Supervisor Mode	User Mode	Setup Options	Password to Enter Setup	Password During Boot
Neither	Can change all options (Note)	Can change all options (Note)	None	None	None
Supervisor only	Can change all options	Can change a limited number of options	Supervisor Password	Supervisor	None
User only	N/A	Can change all options	Enter Password Clear User Password	User	User
Supervisor and user set	Can change all options	Can change a limited number of options	Supervisor Password Enter Password	Supervisor or user	Supervisor or user

Note: If no password is set, any user can change all Setup options.

5. Error Messages and Beep Codes

5.1 Speaker

The board-mounted speaker provides audible error code (beep code) information during POST.

Table 47. Information about Onboard Speaker

For information about	Refer to
The location of the onboard speaker	Figure 1, page 5

5.2 BIOS Beep Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's speaker to beep an error message describing the problem (see Table 48).

Table 48. BIOS Beep Codes

Type	Pattern	Frequency
F2 Setup/F10 Boot Menu Prompt	One 0.5 second beep when BIOS is ready to accept keyboard input	932 Hz
BIOS update in progress	None	
Video error	On-off (1.0 second each) two times, then 2.5-second pause (off), entire pattern repeats (beeps and pause) once and the BIOS will continue to boot.	932 Hz When no VGA option ROM is found.
Memory error	On-off (1.0 second each) three times, then 2.5-second pause (off), entire pattern repeats (beeps and pause) until the system is powered off.	932 Hz
Thermal trip warning	Alternate high and low beeps (1.0 second each) for eight beeps, followed by system shut down.	High beep 2000 Hz Low beep 1500 Hz

5.3 Front-panel Power LED Blink Codes

Whenever a recoverable error occurs during POST, the BIOS causes the board's front panel power LED to blink an error message describing the problem (see Table 49).

Table 49. Front-panel Power LED Blink Codes

Type	Pattern	Note
F2 Setup/F10 Boot Menu Prompt	None	
BIOS update in progress	Off when the update begins, then on for 0.5 seconds, then off for 0.5 seconds. The pattern repeats until the BIOS update is complete.	
Video error	On-off (1.0 second each) two times, then 2.5-second pause (off), entire pattern repeats (blink and pause) until the system is powered off.	When no VGA option ROM is found.
Memory error	On-off (1.0 second each) three times, then 2.5-second pause (off), entire pattern repeats (blinks and pause) until the system is powered off.	
Thermal trip warning	Each beep will be accompanied by the following blink pattern: .25 seconds on, .25 seconds off, .25 seconds on, .25 seconds off. This will result in a total of 16 blinks.	

5.4 BIOS Error Messages

Table 50 lists the error messages and provides a brief description of each.

Table 50. BIOS Error Messages

Error Message	Explanation
CMOS Battery Low	The battery may be losing power. Replace the battery soon.
CMOS Checksum Bad	The CMOS checksum is incorrect. CMOS memory may have been corrupted. Run Setup to reset values.
Memory Size Decreased	Memory size has decreased since the last boot. If no memory was removed, then memory may be bad.
No Boot Device Available	System did not find a device to boot.

5.5 Port 80h POST Codes

During the POST, the BIOS generates diagnostic progress codes (POST codes) to I/O port 80h. If the POST fails, execution stops and the last POST code generated is left at port 80h. This code is useful for determining the point where an error occurred.

Displaying the POST codes requires a POST card that can interface with the Low Pin Count (LPC) Debug header. The POST card can decode the port and display the contents on a

medium such as a seven-segment display. Refer to the location of the LPC Debug header in Figure 1.

The following tables provide information about the POST codes generated by the BIOS:

- Table 51 lists the Port 80h POST code ranges
- Table 52 lists the Port 80h POST codes themselves
- Table 53 lists the Port 80h POST sequence

Note: In the tables listed above, all POST codes and range values are listed in hexadecimal.

Table 51. Port 80h POST Code Ranges

Range	Subsystem
0x00 – 0x05	Entering SX states S0 to S5.
0x10, 0x20, 0x30, 0x40, 0x50	Resuming from SX states. 0x10 –0x20 – S2, 0x30 – S3, and so on.
0x08 – 0x0F	Security (SEC) phase
0x11 0x1F	PEI phase pre MRC execution
0x21 – 0x29	MRC memory detection
0x2A – 0x2F	PEI phase post MRC execution
0x31 – 0x35	Recovery
0x36 – 0x3F	Platform DXE driver
0x41 – 0x4F	CPU Initialization (PEI, DXE, SMM)
0x50 – 0x5F	I/O Buses: PCI, USB, ATA and so on. 0x5F is an unrecoverable error. Start with PCI.
0x60 – 0x6F	BDS
0x70 – 0x7F	Output devices: All output consoles.
0x80 – 0x8F	For future use
0x90 – 0x9F	Input devices: Keyboard/Mouse.
0xA0 – 0xAF	For future use
0xB0 – 0xBF	Boot Devices: Includes fixed media and removable media. Not that critical since consoles should be up at this point.
0xC0 – 0xCF	For future use
0xD0 – 0xDF	For future use

Table 52. Port 80h POST Codes

Port 80 Code	Progress Code Enumeration
	ACPI S States
0x00,0x01,0x02,0x03,0x04,0x05	Entering S0, S2, S3, S4, or S5 state
0x10,0x20,0x30,0x40,0x50	Resuming from S2, S3, S4, S5
	Security Phase (SEC)
0x08	Starting BIOS execution after CPU BIST
0x09	SPI prefetching and caching
0x0A	Load BSP microcode

Port 80 Code	Progress Code Enumeration
0x0B	Load APs microcodes
0x0C	Platform program baseaddresses
0x0D	Wake Up All APs
0x0E	Initialize NEM
0x0F	Pass entry point of the PEI core
	PEI before MRC
	PEI Platform driver
0x11	Set bootmode, GPIO init
0x12	Early chipset register programming including graphics init
0x13	Basic PCH init, discrete device init (1394, SATA)
0x14	LAN init
0x15	Exit early platform init driver
	PEI SMBUS*
0x16	SMBUSriver init
0x17	Entry to SMBUS* execute read/write
0x18	Exit SMBUS* execute read/write
	PEI CK505 Clock Programming
0x19	Entry to CK505 programming
0x1A	Exit CK505 programming
	PEI Over-Clock Programming
0x1B	Entry to entry to PEI over-clock programming
0x1C	Exit PEI over-clock programming
	Memory
0x21	MRC entry point
0x23	Reading SPD from memory DIMMs
0x24	Detecting presence of memory DIMMs
0x27	Configuring memory
0x28	Testing memory
0x29	Exit MRC driver
	PEI after MRC
0x2A	Start to Program MTRR Settings
0x2B	Done Programming MTRR Settings
	PEIMs/Recovery
0x31	Crisis Recovery has initiated
0x33	Loading recovery capsule
0x34	Start recovery capsule/valid capsule is found
	CPU Initialization
	CPU PEI Phase
0x41	Begin CPU PEI Init
0x42	XMM instruction enabling
0x43	End CPU PEI Init
	CPU PEI SMM Phase

Port 80 Code	Progress Code Enumeration
0x44	Begin CPU SMM Init smm relocate bases
0x45	Smm relocate bases for APs
0x46	End CPU SMM Init
	CPU DXE Phase
0x47	CPU DXE Phase begin
0x48	Refresh memory space attributes according to MTRRs
0x49	Load the microcode if needed
0x4A	Initialize strings to HII database
0x4B	Initialize MP support
0x4C	CPU DXE Phase End
	CPU DXE SMM Phase
0x4D	CPU DXE SMM Phase begin
0x4E	Relocate SM bases for all APs
0x4F	CPU DXE SMM Phase end
	I/O BUSES
0x50	Enumerating PCI buses
0x51	Allocating resources to PCI bus
0x52	Hot Plug PCI controller initialization
	USB
0x58	Resetting USB bus
0x59	Reserved for USB
	ATA/ATAPI/SATA
0x5A	Resetting PATA/SATA bus and all devices
0x5B	Reserved for ATA
	BDS
0x60	BDS driver entry point initialize
0x61	BDS service routine entry point (can be called multiple times)
0x62	BDS Step2
0x63	BDS Step3
0x64	BDS Step4
0x65	BDS Step5
0x66	BDS Step6
0x67	BDS Step7
0x68	BDS Step8
0x69	BDS Step9
0x6A	BDS Step10
0x6B	BDS Step11
0x6C	BDS Step12
0x6D	BDS Step13
0x6E	BDS Step14
0x6F	BDS return to DXE core (should not get here)
	Keyboard (PS/2 or USB)

Port 80 Code	Progress Code Enumeration
0x90	Resetting keyboard
0x91	Disabling the keyboard
0x92	Detecting the presence of the keyboard
0x93	Enabling the keyboard
0x94	Clearing keyboard input buffer
0x95	Instructing keyboard controller to run Self Test (PS/2 only)
	Mouse (PS/2 or USB)
0x98	Resetting mouse
0x99	Detecting mouse
0x9A	Detecting presence of mouse
0x9B	Enabling mouse
	Fixed Media
0xB0	Resetting fixed media
0xB1	Disabling fixed media
0xB2	Detecting presence of a fixed media (IDE hard drive detection and so on.)
0xB3	Enabling/configuring a fixed media
	Removable Media
0xB8	Resetting removable media
0xB9	Disabling removable media
0xBA	Detecting presence of a removable media (IDE, CDROM detection and so on.)
0xBB	Enabling/configuring a removable media
	DXE Core
0xE4	Entered DXE phase
	BDS
0xE7	Waiting for user input
0xE8	Checking password
0xE9	Entering BIOS setup
0xEB	Calling Legacy Option ROMs
	Runtime Phase/EFI OS Boot
0xF8	EFI boot service ExitBootServices ( ) has been called
0xF9	EFI runtime service SetVirtualAddressMap ( ) has been called

Table 53. Typical Port 80h POST Sequence

POST Code	Description
21	Initializing a chipset component
22	Reading SPD from memory DIMMs
23	Detecting presence of memory DIMMs
25	Configuring memory

POST Code	Description
28	Testing memory
34	Loading recovery capsule
E4	Entered DXE phase
12	Starting application processor initialization
13	SMM initialization
50	Enumerating PCI busses
51	Allocating resourced to PCI bus
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
95	Keyboard Self Test
EB	Calling Video BIOS
58	Resetting USB bus
5A	Resetting PATA/SATA bus and all devices
92	Detecting the presence of the keyboard
90	Resetting keyboard
94	Clearing keyboard input buffer
5A	Resetting PATA/SATA bus and all devices
28	Testing memory
90	Resetting keyboard
94	Clearing keyboard input buffer
E7	Waiting for user input
01	INT 19
00	Ready to boot

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