TAS5518-5261K2EVM

This user's guide describes the operation of the evaluation module for the TAS5518 Digital Audio PWM Processor and the TAS5261 Digital Amplifier Power Output Stage from Texas Instruments.

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1 Overview

The TAS5518-5261K2EVM PurePath Digital™ customer evaluation amplifier module demonstrates the two audio integrated circuits TAS5518 and TAS5261 from Texas Instruments (TI).

TAS5518PAG is a high-performance, 32-bit (24-bit input) multichannel PurePath Digital™ pulse width modulator (PWM) based on Equibit™ technology with fully symmetrical AD modulation scheme. It accepts input sample rates from 32 kHz to 192 kHz. The device also has digital audio processing (DAP) that provides 48-bit signal processing, advanced performance, and a high level of system integration. The device has interfaces for headphone output and power supply volume control (PSVC).

The TAS5261 is a high-performance, integrated mono digital amplifier power stage designed to drive 4-Ω to 8-Ω speakers with low harmonic distortion. This system requires only a simple, passive demodulation filter to deliver high-quality, high-efficiency audio amplification.

This EVM, together with a TI input-USB board, is a complete 2-channel stereo digital audio amplifier system which includes digital input (S/PDIF), analog inputs, interface to PC, and DAP features like digital volume control, input and output mixers, automute, tone controls, loudness, EQ filters, and dynamic range compression (DRC). Configuration options include power-stage failure protection and a mini-jack connector for headphone.

This stereo system is designed for home theater applications such as A/V receivers.

1.1 TAS5518-5261K2EVM Features

- Two-channel PurePath Digital™ evaluation module.
- Self-contained protection system (short circuit and thermal).
- Standard I^2S and I^2C/control connector for TI input board
- Double-sided plated-through PCB layout.

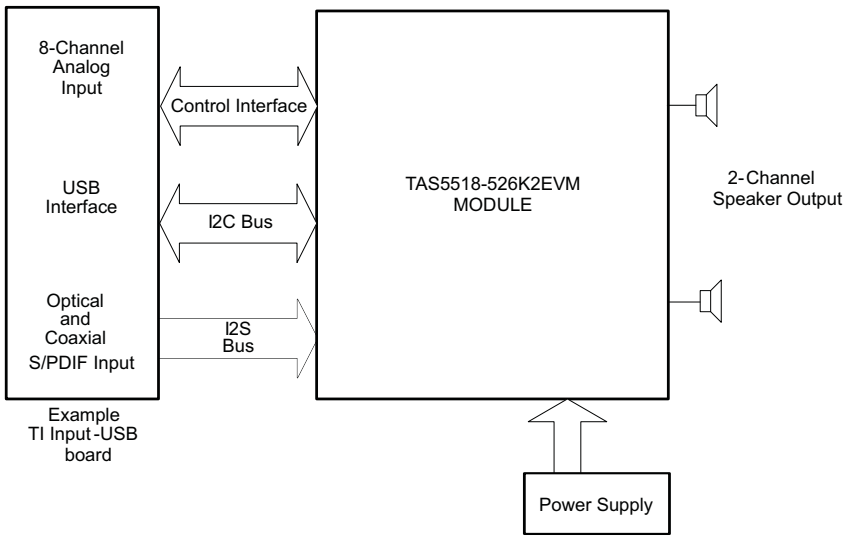

Figure 1. Integrated PurePath Digital™ Amplifier System

1.2 PCB Key Map

Physical structure for the TAS5518-5261K2EVM is illustrated in Figure 2.

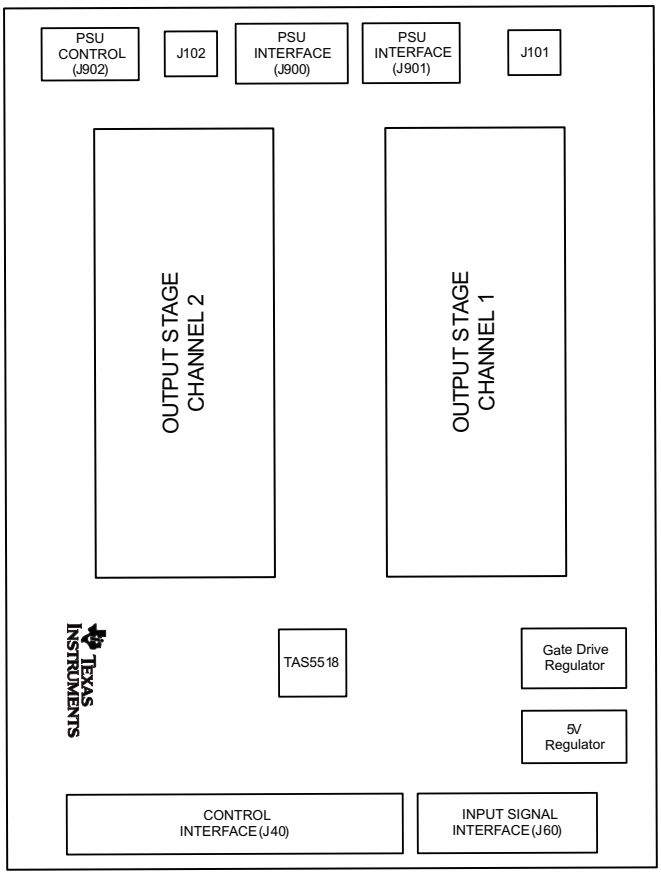

Figure 2. Physical Structure for the TAS5518-5261K2EVM (Approximate Layout)

2 Quick Setup Guide

This section describes the TAS5518-5261K2EVM board in regards to power supplies and system interfaces. The section provides information regarding handling and unpacking, absolute operating conditions, and a description of the factory default switch and jumper configuration.

This section provides a step-by-step guide to configuring the TAS5518-5261K2EVM for device evaluation.

2.1 Electrostatic Discharge Warning

Many of the components on the TAS5518-5261K2EVM are susceptible to damage by electrostatic discharge (ESD). Customers are advised to observe proper ESD handling precautions when unpacking and handling the EVM, including the use of a grounded wrist strap at an approved ESD workstation.

CAUTION

Failure to observe ESD handling procedures can result in damage to EVM components.

2.2 Unpacking the EVM

On opening the TAS5518-5261K2EVM package, ensure that the following items are included:

- 1 pc. TAS5518-5261K2EVM board using one TAS5518PAG and two TAS5261DKD.
- 1 pc. TI Input-USB board for interfacing TAS5518-5261K2EVM w. SPDIF/analog sources and PC for control.
- 1 pc. Signal Interface IDC cable for connection to a I2S front-end like the attached TI Input-USB board.
- 1 pc. Control Interface IDC cable for connection to a I2C front-end like the attached TI Input-USB board.
- 1 pc Cable for connecting Input-USB board to a USB port on a PC for TAS5518 control by software.
- 1 pc. Power supply cable for two regulated power supplies (H-bridge and system supply).
- 1 pc. Power supply cable for one regulated power supply (H-bridge supply).
- 2 pc. Cables for speaker connection.
- 1 pc. PurePath Digital™ CD-ROM:

If any of these items is missing, contact the Texas Instruments Product Information Center nearest you to inquire about a replacement.

Connect Input-USB board to TAS5518-5261K2EVM using the two delivered IDC cables.

2.3 Power Supply Setup

To power up the EVM, two power supplies are needed: one for system power, logic and gate drive, and one for output stage supply. Power supplies are connected to the EVM using delivered power cable red/black, white/black.

Table 1. Recommended Supply Voltages

Description	Voltage Limitations	Current Requirement	Cable
System power supply	15–20 V	0.3 A	Red/black
Output stage power supply	0–50 V	5 A (10-A peak)	White/black

CAUTION

Applying voltage above the limitations given in Table 1 can cause permanent damage to your hardware.

2.4 GUI Software Installation

The TAS5518 GUI provide easy control of all registers in TAS5518. To install the GUI, run the setup file from the PurePath Digital™ CD-ROM.

After installation, turn on the power supplies and connect the USB cable to the Input-USB board.

Start the GUI program from the Windows™ menu. The start-up of the GUI takes a few seconds.

Figure 3. TAS5518 GUI Window

From the files menu, load the configuration file:

TAS5518-5261K2EVM Configuration (2.00).CFG

The file is located on the PurePath Digital™ CD-ROM. This file contains all settings for a default setup of the EVM.

For easy access of the file, it is recommended to copy the files into the directory where the GUI is installed. Default is C:\Program Files\Texas Instruments Inc\TAS5518\

For more advanced use of the GUI, see the GUI user's guide and data sheet for the TAS5518.

3 System Interfaces

This section describes the TAS5518-5261K2EVM board in regards to power supplies and system interfaces.

3.1 Power Supply (PSU) Interface (J901 and J900)

The TAS5518-5261K2EVM module must be powered from external power supplies. High-end audio performance requires a stabilized power supply with low ripple voltage and low output impedance.

Note: The length of power supply cable must be minimized. Increasing the length of the PSU cable is equal to increasing the distortion for the amplifier at high output levels and low frequencies.

Maximum output stage supply voltage depends on the speaker load resistance. Check the recommended maximum supply voltage in the TAS5261 data sheet.

Table 2. Recommended Supply Voltages

Description	Voltage Limitations (4-Ω Load)	Current Recommendations
System power supply	15–20 V	0.3 A
Output stage power supply	0–50 V	5 A (10-A peak)(1)

(1) The rated current corresponds to a 2-channel full scale (125 W each), which most likely is adequate for a standard 2-channel amplifier design. For 2-channel, continuously running 125 W at 500 Hz or below the peak current requirement is double – 10 A.

The recommended TAS5261 power-up sequence is shown in Figure 4. For proper TAS5261 operation, the $\overline{\text{RESET}}$ signal should be kept low during power up. $\overline{\text{RESET}}$ is pulled low during power up for 200 ms by the onboard reset generator (U904).

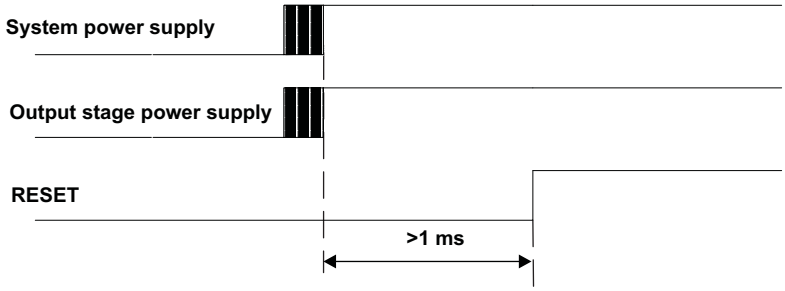

Figure 4. Recommended Power-Up Sequence

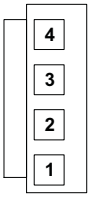

Figure 5. J901 and J900 Pin Numbers

Table 3. J901 Pin Description

Pin	Net-Name on Schematics	Description
1	PVDD	Output stage power supply
2	SYSTEM	System Power Supply
3	GND	Ground
4	GND	Ground

Table 4. J900 Pin Description

Pin	Net-Name on Schematics	Description
1	PVDD	Extra Output stage power supply
2	PVDD	Extra Output stage power supply
3	GND	Extra Ground
4	GND	Extra Ground

3.2 PSU Control Interface (J902)

This interface is used for onboard sensing of output supply voltage and for the power supply volume control (PSVC) signal.

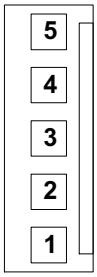

Figure 6. J902 Pin Numbers

Table 5. J900 Pin Description

Pin	Net-Name on Schematics	Description
1	–	Reserved for future use
2	PVDD	Sense of output power supply
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bi-directional)
5	PSVC	Power Supply Volume Control Signal

3.3 Loudspeaker Connectors (J100 and J200)

CAUTION

Both positive and negative speaker outputs are floating and may not be connected to ground (e.g., through an oscilloscope).

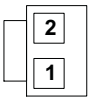

Figure 7. J100 and J200 Pin Numbers

Table 6. J100 and J200 Pin Description

Pin	Net-Name on Schematics	Description
1	OUT-1	Speaker negative output
2	OUT-2	Speaker positive output

3.4 Control Interface (J40)

This interface connects the TAS5518-5261K2EVM board to a TI input-USB board.

Table 7. J40 Pin Description

Pin	Net-Name on Schematics	Description
1	GND	Ground
2	RESERVED	—
3	GND	Ground
4	$\overline{\text{RESET}}$	System reset (bi-directional). Activate $\overline{\text{MUTE}}$ before $\overline{\text{RESET}}$ for quiet reset
5	RESERVED	—
6	$\overline{\text{MUTE}}$	Ramp volume from any setting to noiseless soft mute. Mute can also be activated by I2C
7	RESERVED	—
8	RESERVED	—
9	RESERVED	—
10	SDA	I2C data clock
11	GND	Ground
12	SCL	I2C bit clock
13	RESERVED	—
14	RESERVED	—
15	RESERVED	—
16	RESERVED	—
17	GND	Ground
18	RESERVED	—
19	RESERVED	—
20	$\overline{\text{SD}}$	Shutdown reporting. Activated if one or more TAS5261 has high current or high temperature. See section 3: Protection
21	RESERVED	—
22	$\overline{\text{OTW}}$	Temperature warning. Activated if one or more TAS5261 has reached temperature warning level
23	RESERVED	—
24	RESERVED	—
25	GND	Ground
26	GND	Ground
27	RESERVED	—
28	RESERVED	—
29	RESERVED	—
30	RESERVED	—
31	GND	Ground
32	GND	Ground
33	+5V	+5-Vdc power supply (output)
34	+5V	+5-Vdc power supply (output)

3.5 Digital Audio Interface (J60)

The digital audio interface contains digital audio signal data (I2S), clocks etc. See the TAS5518 data sheet (SLES115) for signal timing and details not explained in this document.

Table 8. J60 Pin Description

Pin	Net-Name on Schematics	Description
1	GND	Ground
2	MCLK	Master Clock input. Low jitter system clock for PWM generation and reclocking. Ground connection from source to TAS5518 must be a low-impedance connect
3	GND	Ground
4	SDIN1	I2S Data 1, Channel 1 and 2
5	SDIN2	I2S Data 2, Channel 3 and 4
6	SDIN3	I2S Data 3, Channel 5 and 6
7	SDIN4	I2S Data 4, Channel 7 and 8
8	—	Reserved
9	—	Reserved
10	GND	Ground
11	SCLK	I2S bit clock
12	GND	Ground
13	LRCLK	I2S left-right clock
14	GND	Ground
15	—	Reserved
16	GND	Ground

4 Protection

This section describes the short-circuit protection and fault-reporting circuitry of the TAS5261 device.

4.1 Short-Circuit Protection and Fault-Reporting Circuitry

Overcurrent, overtemperature, and undervoltage protections are built into the TAS5261 device, safeguarding the H-bridge and speakers against output short-circuit conditions, overtemperature conditions, and other fault conditions that could damage the system.

4.2 Fault Reporting

4.2.1 Overcurrent Protection (OCP)

To protect the power stage from damage due to high currents, a VDS sensing system is implemented in the TAS5261 device. Based on RDS(on) of the power MOSFETs and the maximum allowed current in the MOSFET, a voltage threshold can be calculated which, when exceeded, triggers the protection. The detector outputs are monitored closely by two protection systems. The first protection system controls the power stage in order to prevent the output current from further increasing For instance, it performs a current-limiting function rather than prematurely shutting down during combinations of high-level music transients and extreme speaker load impedance drops. If the high-current situation persists, i.e., the power stage is being overloaded, a second protection system triggers a latching shutdown, resulting in the power stage being set in the high-impedance (Hi-Z) state.

4.2.2 Overtemperature Protection (OTP)

TAS5261 has an on-chip temperature-sensing system. If the chip temperature reaches a critical temperature, the overtemperature warning pin goes low. If the chip temperature continue to increase, the TAS5261 protects itself by shutting down the power stage. In this case, both $\overline{OTW}$ and $\overline{SD}$ are low.

The shutdown signals together with the temperature warning signal give chip-state information as described in Table 9. Device fault-reporting outputs are open-drain outputs.

The $\overline{OTW}$ and $\overline{SD}$ outputs from TAS5261 indicate fault conditions. See the TAS5261 data sheet for a description of these pins.

Table 9. TAS5621 Warning/Error Signal Decoding

$\overline{OTW}$	$\overline{SD}$	Device Condition
0	0	High-temperature error and/or high-current error
0	1	High-temperature warning
1	0	Undervoltage lockout or high-current error
1	1	Normal operation, no errors/warnings

The temperature warning signals at the TAS5518-5621K2EVM board are wired-OR to one temperature warning signal ($\overline{OTW}$– pin 22 in control interface connector). Shutdown signals are wired-OR into one shutdown signal ($\overline{SD}$– pin 20 in control interface connector).

The shutdown signals together with the temperature warning signal give chip-state information as described in Table 9. Device fault-reporting outputs are open-drain outputs.

5 Related Documentation from Texas Instruments

The following table contains a list of documents that have detailed descriptions of the integrated circuits used in the design of the TAS5518-5261K2EVM. These documents can be obtained at the TI Web site http://www.ti.com.

Table 10. Related Documentation From Texas Instruments

Part Number	Literature Number
TAS5518	SLES115
TAS5261	SLES188
UA78M12	SLVS059
TPS79133	SLVS325
TPS3825-33	SLVS165
TPS62112	SLVS585

5.1 Additional Documentation

- TAS5518-5261K2EVM Application Report (SLAA332)
- PC Configuration Tool for TAS5518 (TAS5518 GUI ver. 4.0 or later)

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EVM WARNINGS AND RESTRICTIONS

It is important to operate this EVM within the input voltage range of 0 V to 50 V for the output stage and 15 V to 20 V for the system supply and the output voltage range of 0 V to 50 V.

Exceeding the specified input range may cause unexpected operation and/or irreversible damage to the EVM. If there are questions concerning the input range, please contact a TI field representative prior to connecting the input power.

Applying loads outside of the specified output range may result in unintended operation and/or possible permanent damage to the EVM. Please consult the EVM User's Guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative.

During normal operation, some circuit components may have case temperatures greater than 75°C. The EVM is designed to operate properly with certain components above 75°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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