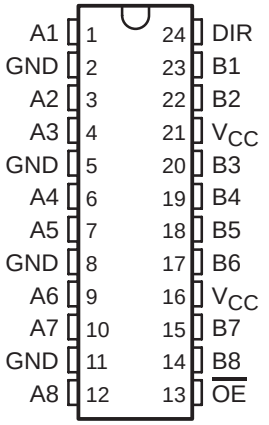
- **State-of-the-Art BiCMOS Design Significantly Reduces I_{CCZ}**
- **Designed to Facilitate Incident-Wave Switching for Line Impedances of 25 Ω or Greater**
- **Distributed V_{CC} and GND Pins Minimize Noise Generated by the Simultaneous Switching of Outputs**
- **Data Flow-Through Pinout (All Inputs on Opposite Side From Outputs)**
- **High-Impedance State During Power Up and Power Down**
- **ESD Protection Exceeds 2000 V Per MIL-STD-883C, Method 3015**
- **Package Options Include Plastic Small-Outline (DW) Packages and Standard Plastic 300-mil DIPs (NT)**

DW OR NT PACKAGE
(TOP VIEW)



description

The SN64BCT25245 is a 25-Ω octal bus transceiver designed for asynchronous communication between data buses. It improves both the performance and density of 3-state memory address drivers, clock drivers, and bus-oriented transceivers.

The device allows data transmission from the A bus to the B bus or from the B bus to the A bus depending upon the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can disable the device so that both buses are effectively isolated.

This transceiver is capable of sinking 188-mA I_{OL}, which facilitates switching 25-Ω transmission lines on the incident wave. The distributed V_{CC} and GND pins minimize switching noise for more reliable system operation.

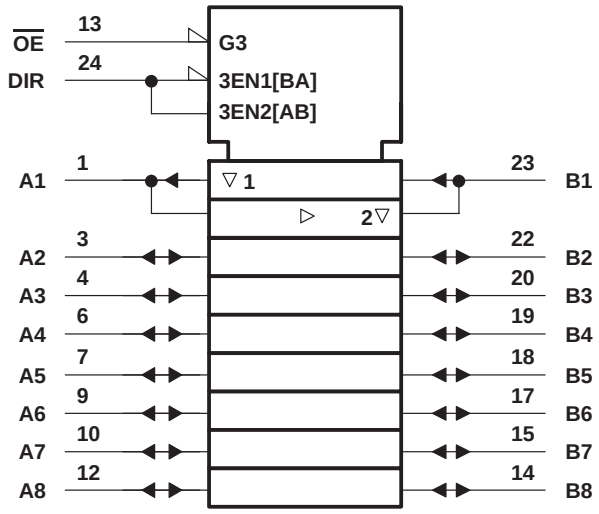
The outputs are in a high-impedance state during power up and power down while the supply voltage is less than approximately 3 V.

The SN64BCT25245 is characterized for operation from −40°C to 85°C and 0°C to 70°C.

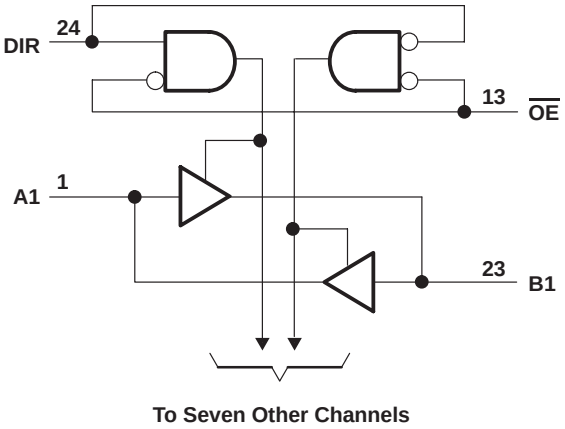
FUNCTION TABLE

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

logic symbol†



logic diagram (positive logic)



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)‡

Supply voltage range, V_{CC} . . . . . −0.5 V to 7 V
Input voltage range, V_I (see Note 1): Control inputs . . . . . −0.5 V to 7 V
I/O ports . . . . . −0.5 V to 5.5 V
Voltage range applied to any output in the disabled or power-off state, V_O . . . . . −0.5 V to 7 V
Voltage range applied to any output in the high state, V_O (B port) . . . . . −0.5 V to V_{CC}
Input clamp current, I_{IK} . . . . . −30 mA
Current into any output in the low state, I_O: A port . . . . . 376 mA
B port . . . . . 48 mA
Operating free-air temperature range . . . . . −40°C to 85°C
Storage temperature range . . . . . −65°C to 150°C

‡ Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{IK}	Input clamp current				−18	mA
I_{OH}	High-level output current	A port			−80	mA
		B port			−3	
I_{OL}	Low-level output current	A port			188	mA
		B port			24	
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}	A port	V_{CC} = 4.75 V,	I_{OH} = − 3 mA		2.7			V
		V_{CC} = 4.5 V,	I_{OH} = −80 mA		2			
	B port	V_{CC} = 4.5 V,	I_{OH} = −3 mA		2.4	3.3		
V_{OL}	A port	V_{CC} = 4.5 V	I_{OL} = 94 mA			0.42	0.55	V
			I_{OL} = 188 mA				0.7	
	B port	V_{CC} = 4.5 V,	I_{OL} = 24 mA			0.35	0.5	
I_{OZ}		V_{CC} = 0 to 2.3 V (power up)	V_O = 2.7 V	$\overline{OE}$ at 0.8 V			70	µA
			V_O = 0.5 V				−0.6	mA
		V_{CC} = 1.8 V to 0 (power down)	V_O = 2.7 V	$\overline{OE}$ at 0.8 V			70	µA
			V_O = 0.5 V				−0.6	mA
I_I	A and B ports	V_{CC} = 0 to 5.5 V,	V_I = 5.5 V				0.25	mA
	DIR and $\overline{OE}$						0.1	
I_{IH}‡	A and B ports	V_{CC} = 5.5 V,	V_I = 2.7 V				70	µA
	DIR and $\overline{OE}$						20	
I_{IL}‡	A and B ports	V_{CC} = 5.5 V,	V_I = 0.5 V				−0.6	mA
	DIR and $\overline{OE}$							
I_{OS}§	B port¶	V_{CC} = 5.5 V,	V_O = 0		−60		−150	mA
I_{CCL}	A to B port	V_{CC} = 5.5 V				48	60	mA
	B to A port					95	125	
I_{CCH}	A to B port	V_{CC} = 5.5 V				36	46	mA
	B to A port					63	80	
I_{CCZ}		V_{CC} = 5.5 V				12	16	mA
C_i	$\overline{OE}$ and DIR	V_{CC} = 5.5 V,	V_I = 2.5 V to 0.5 V			8		pF
C_{io}	A port	V_{CC} = 5.5 V,	V_I = 2.5 V to 0.5 V			18		pF
	B port					8		

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state outputs current.
§ Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
¶ Testing for this parameter on the A port is not recommended.

switching characteristics (see Note 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω, T_A = 25°C			V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R1 = 500 Ω, R2 = 500 Ω				UNIT
						T_A = −40°C to 85°C		T_A = 0°C to 70°C		
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	1.2	3.3	5.1	1.2	5.7	1.2	5.7	ns
t_{PHL}			1.9	4.3	6.7	1.9	7.3	1.9	7.2	
t_{PLH}	B	A	1.2	3.3	4.8	1.2	5.5	1.2	5.5	ns
t_{PHL}			2.1	4	5.6	2.1	6.3	2.1	6.2	
t_{PZH}	$\overline{OE}$	A	3.7	6.3	8.4	3.7	9.7	3.7	9.6	ns
t_{PZL}			4.5	7.4	9.2	4.5	10.6	4.5	10.3	
t_{PHZ}	$\overline{OE}$	A	1.8	3.7	5.5	1.8	6.2	1.8	6.2	ns
t_{PLZ}			3.3	5.1	7.2	3.3	8.8	3.3	8.3	
t_{PZH}	$\overline{OE}$	B	3.4	5.7	7.9	3.4	8.9	3.4	8.9	ns
t_{PZL}			4.3	6.6	8.7	4.3	9.9	4.3	9.7	
t_{PHZ}	$\overline{OE}$	B	2.7	4.5	6.3	2.7	6.9	2.7	6.9	ns
t_{PLZ}			1.7	4.5	6.8	1.7	7.7	1.7	7.5	

NOTE 2: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN64BCT25245DW	ACTIVE	SOIC	DW	24	25	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	6BCT25245	Samples
SN64BCT25245DWE4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		Samples
SN64BCT25245DWG4	ACTIVE	SOIC	DW	24		TBD	Call TI	Call TI	-40 to 85		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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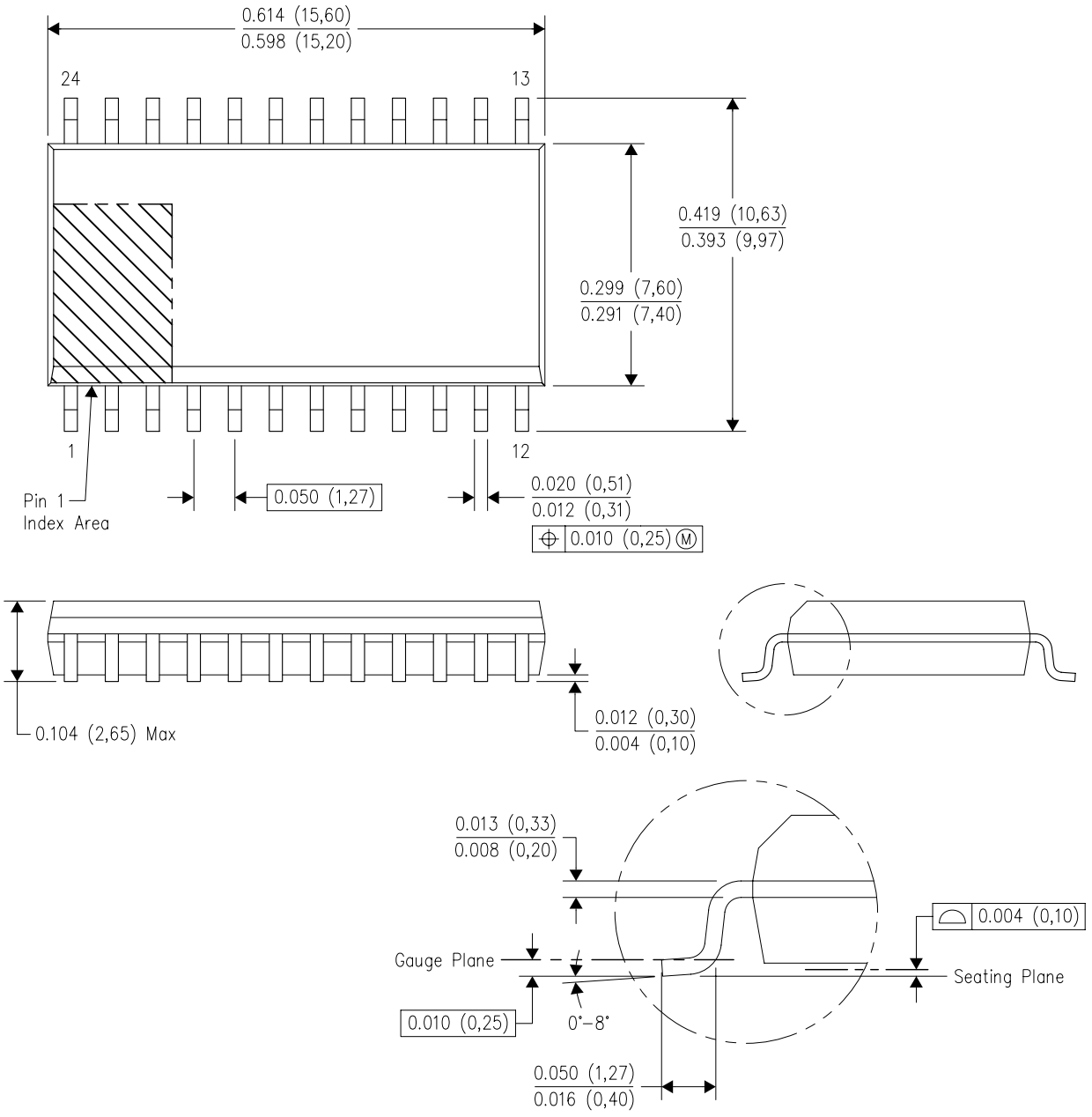
DW (R–PDSO–G24) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters). Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
D. Falls within JEDEC MS–013 variation AD.

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