IEEE 802.3af POWER INTERFACE SWITCH FOR POWER OVER ETHERNET (PoE) POWERED DEVICES

FEATURES

- **Integrated Power Interface Switch for IEEE 802.3af Powered Devices (PDs)**
- **Provides PD Detection Signature**
- **Provides PD Classification Signature (Class 0−4)**
- **Programmable Inrush Current Limit**
- **Internal 0.3-Ω Low-Side FET**
- **Interfaces to DC/DC Soft-Start for DC/DC Enable**
- **Internal Thermal Protection – Disconnects PD Load**
- **Minimal External Parts Count**
- **8-Pin SOIC, 8-Pin TSSOP Packages**

APPLICATIONS

- **VoIP Phones**
- **Internet Appliances**
- **Wireless LAN Access Points**
- **Bluetooth™ Access Points**

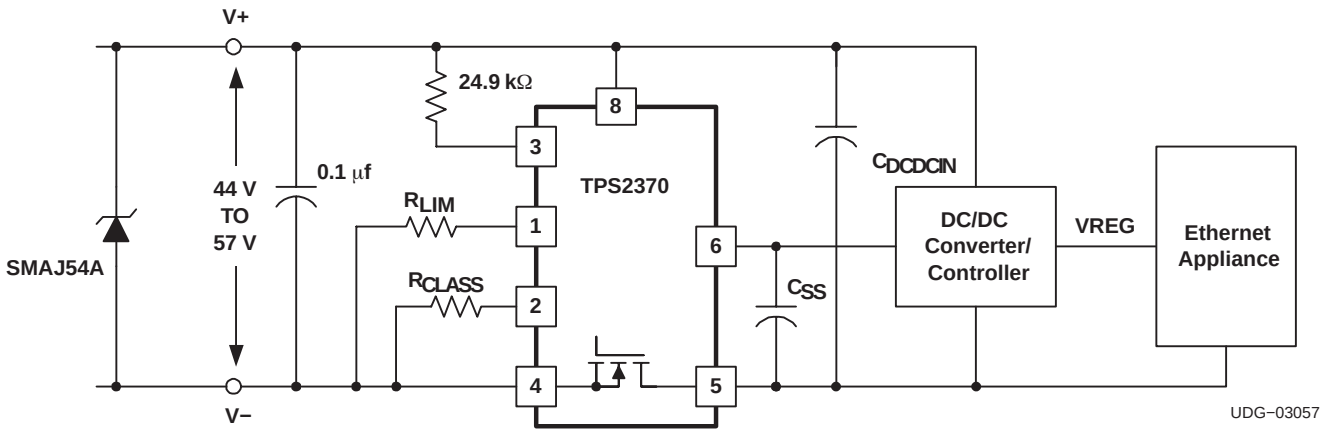
DESCRIPTION

Acting as an interface between the power sourcing equipment (PSE) and the powered device (PD), the TPS2370 performs all detection, classification, inrush current limiting, and switch FET control that is necessary for compliance with the IEEE 802.3af Standard. An internal 0.3-Ω FET provides maximum power delivery. As an additional feature, the TPS2370 interfaces with the enable/soft-start signal of a dc-to-dc converter, eliminating the need to have an accurate UVLO in the dc-to-dc converter.

At low input voltages (1.8 V to 10 V), the TPS2370 draws less than 12 μA, allowing accurate sensing of the external 24.9-kΩ discovery resistor. At input voltages between 15 V and 20 V, an external resistor sets the level of current to be drawn during classification mode. TPS2370 is compatible with current as well as voltage measurement schemes for classification. Above 20-V input, the classification current is shut off, reducing internal power dissipation.

The TPS2370 drives an internal low-side FET for control of the return side of the power path. The internal FET is turned on when the input voltage reaches 40 V and above. When the input voltage decreases, the FET remains on until the input voltage drops to below 30 V.

TYPICAL APPLICATION



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DESCRIPTION (CONTINUED)

During initial turnon of the switch (inrush mode), an external resistor is used to program the inrush current, allowing a wide range of capacitor values to be used at the load. According to IEEE 802.3af specification, inrush current of 400 mA is allowed only for 50 ms, limiting the load capacitor to approximately 180 μF. A programmable inrush current limit removes this limitation, allowing a larger capacitor to be used with a lower inrush current limit.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGE(1)	PART NUMBER
0°C to 70°C	Plastic TSSOP (PW)	TPS2370PW
	Plastic SOIC (D)	TPS2370D

(1) The PW and D packages are also available taped and reeled. Add an R suffix to the device type (i.e., TPS2370PWR).

ABSOLUTE MAXIMUM RATINGS

Over operating free-air temperature range unless otherwise noted (2)

		TPS2370	UNIT
Input voltage range, wrt V_{EE}	ILIM	4	V
	CLASS	12	
	DET, RTN, EN_DC, VDD	68	
	EN_DC (wrt RTN)	5	
Operating junction temperature range, T_J		−55 to 150	°C
Storage temperature, T_{stg}		−65 to 150	°C
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	°C

(2) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Input voltage, V_I		48	57	V
Operating junction temperature, T_J	0		70	°C

DISSIPATION RATINGS(3)(4)

PACKAGE	THERMAL IMPEDANCE JUNCTION-TO-AMBIENT	T_A < 25°C POWER RATING	T_A = 25°C DERATING FACTOR	T_A = 70°C POWER RATING
8-Pin Plastic TSSOP (PW)	258.5°C/W	464 mW	3.9 mW/°C	290 mW
8-Pin Plastic SOIC (D)	176.0°C/W	682 mW	5.7 mW/°C	426 mW

(3) Test board conditions:
1. 3” x 3”, 4 layers, thickness: 0.062”
2. 1.5 oz. copper traces located on the top of the PCB
3. 1.5 oz. copper ground plane on the bottom of the PCB
4. 0.5 oz. copper ground planes on the 2 internal layers
5. 12 thermal vias

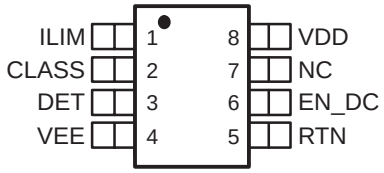
(4) Maximum power dissipation may be limited by overcurrent protection.

ELECTRICAL CHARACTERISTICS

V_{DD} = 48 V; T_A = 0°C to 70°C; all voltages and currents are with respect to VEE; (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
	Offset current	VDD = 1.8 V, DET = OPEN			3	µA
I_{DD}	Sleep current	1.8 V ≤ VDD < 10 V, DET = OPEN		5	12	µA
I_{DET}	Detection load current	R_{DET} = 24.9 kΩ, VDD = 1.8 V	70	73	76	µA
		R_{DET} = 24.9 kΩ, VDD = 9.5 V	380	390	400	µA
	Classification current threshold	Turn on	10.0	12.5	14.0	V
		Turn off	21.5	22.5	23.5	V
	VDD current class 0	0.44 W ≤ P_{PoE} ≤ 12.95 W, 15 V ≤ VDD ≤ 20 V, R_{CLASS} = 4.42 kΩ	2.2	2.5	2.8	mA
	VDD current class 1	0.44 W ≤ P_{PoE} ≤ 3.84 W, 15 V ≤ VDD ≤ 20 V, R_{CLASS} = 953 Ω	10.4	10.8	11.5	mA
	VDD current class 2	3.84 W ≤ P_{PoE} ≤ 6.49 W, 15 V ≤ VDD ≤ 20 V, R_{CLASS} = 549 Ω	18.1	18.6	19.5	mA
	VDD current class 3	6.49 W ≤ P_{PoE} ≤ 12.95 W, 15 V ≤ VDD ≤ 20 V, R_{CLASS} = 357 Ω	27.7	28.4	29.9	mA
	VDD current class 4	Reserved for future use, 15 V ≤ VDD ≤ 20 V, R_{CLASS} = 255 Ω	38.5	39.6	42.0	mA
	VDD quiescent current	30 V ≤ VDD ≤ 57 V, R_{CLASS} = 255 Ω		500	800	µA
	Input UVLO threshold	Turn on	38.6	40.2	41.8	V
		Turn off	30.2	31.4	32.6	V
	UVLO hysteresis		7.8	8.8	9.8	V
	EN_DC sink current		40	80	200	µA
	RTN threshold for EN_DC		1.2	1.5	1.8	V
	DMOS $R_{DS(on)}$	I_{RTN} = 200 mA	0.15	0.30	0.60	Ω
	Full load current limit	V_{RTN} < 1.5 V	405	455	505	mA
	ILIM current limit programming	R_{LIM} = 125 kΩ, V_{RTN} > 1.5 V during startup	180	250	300	mA
	Thermal shutdown temperature			144		°C
	Thermal shutdown hysteresis			20		°C

D OR PW PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

TERMINAL NAME	TERMINAL NO.	I/O	DESCRIPTION
CLASS	2	O	Sets classification level with a single resistor to VEE. A precision voltage of 10 V is applied to this pin during classification. R_{CLASS} values listed in Table 1.
DET	3	O	Connect the 24.9-kΩ detection resistor (R_{DET}) between this pin and VDD.
EN_DC	6	O	Ties to dc-to-dc converter's shutdown or soft-start pin. Sinks 80 μA until the load capacitor is fully charged.
ILIM	1	O	Sets start-up current limit level with a resistor to VEE. If using $C_{DC2DCIN}$ > 180 μF, I_{RUSH} must be less than 400 mA. Extra capacitance on ILIM pin can cause oscillations in the current waveform.
RTN	5	O	Return pin. Connect this pin to input return side of the dc-to-dc converter.
VDD	8	I	Connection to PD input port positive voltage.
VEE	4	I	Input side power return for the controller.

(1) $I_{INRUSH} = 450\ mA - \left(\frac{25\ k\Omega}{R_{LIM}}\right) \times (1\ A)$

DETAILED PIN DESCRIPTIONS

ILIM (Pin 1)

Inrush current limiting pin. This pin is used to program the inrush current of the device. By placing a resistor to VEE from this pin, the inrush current into the load is limited via the following equation:

$$I_{INRUSH} = 450\ mA - \left(\frac{25\ k\Omega}{R_{LIM}}\right) \times (1\ A) \quad (1)$$

CLASS (Pin 2)

Classification pin. The PD can be optionally classified by adding a resistor from this pin to ground. The resistor specific to each class is given in *Table 1: PoE Classification Resistance Values*.

DET (Pin3)

Detection pin. This pin is used to set up the detection resistance during PD detection. By tying a resistor, R_{DET}, from this pin to VDD, the user sets the detection resistance. It should be noted that the device itself looks like approximately 1 MΩ of resistance in parallel with R_{DET}.

VEE (Pin 4)

Negative supply to the device.

RET (Pin 5)

Negative supply to the load. This pin is the drain side of a FET between the RET pin and the VEE pin, providing hot swap capabilities to the load. When the FET is switched on, there is approximately 300 mΩ between this pin and VEE.

EN_DC (Pin 6)

Enable pin for the load. This pin is intended to be used with a dc-to-dc coverter with a soft start capacitor. When power is not available to the dc-to-dc converter, this pin sinks 80 μA and holds off the soft-start capacitor on the dc-to-dc converter. Once the voltage across the load is within 1.5 V of its final value, the EN_DC pin stops drawing current and becomes high impedance, allowing the dc-to-dc converter to soft start normally.

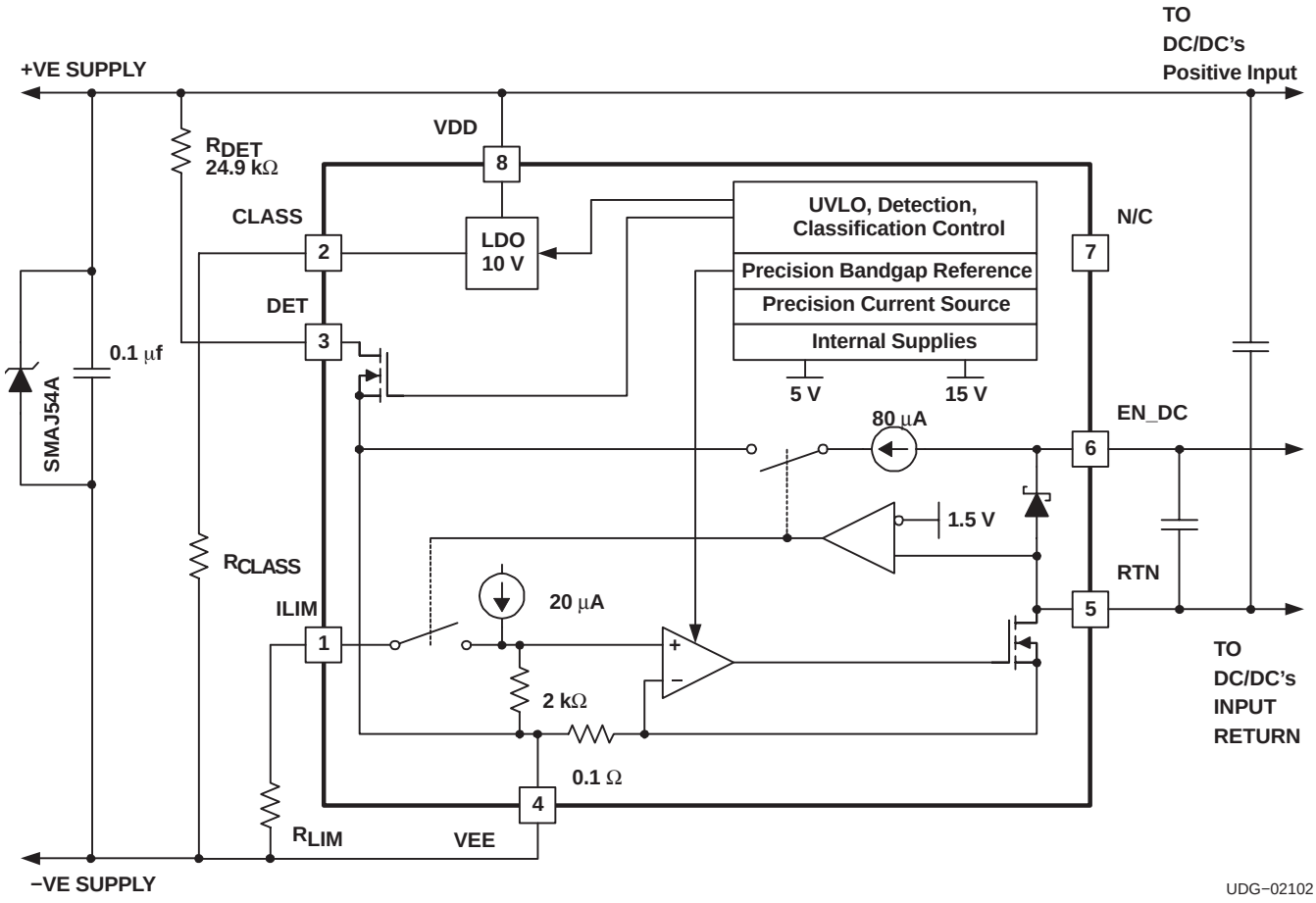
VDD (Pin 8)

Positive supply to the device.

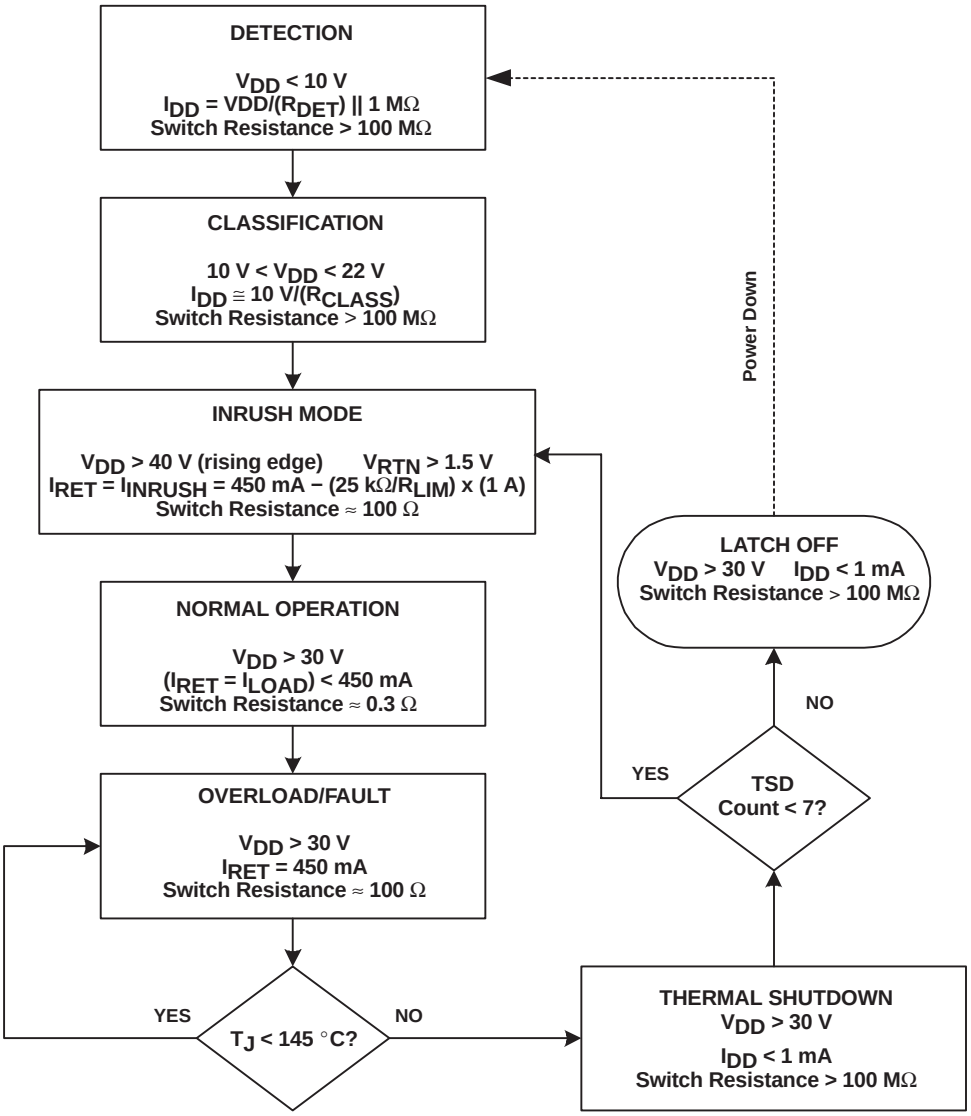
Table 1. PoE Classification Resistance Values

CLASS	RESISTANCE (R_{CLASS}) VALUE (Ω)	POWERED DEVICES (PDs) Power (W)	CLASSIFICATION CURRENT (mA)
0	4420	0.44 − 12.95	2.5
1	953	0.44 − 3.84	10.8
2	549	3.84 − 6.49	18.6
3	357	6.49 − 12.95	28.4
4	255	reserved for future use	39.6

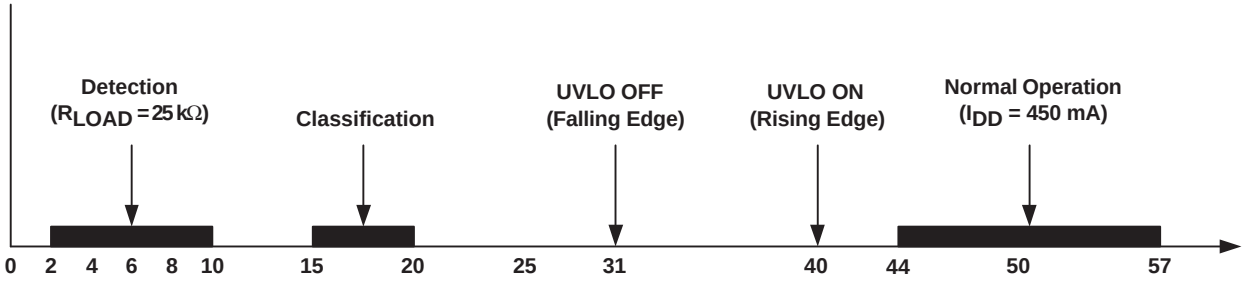
INTERNAL BLOCK DIAGRAM



STATE DIAGRAM



MACHINE STATE



APPLICATION INFORMATION

OVERVIEW

With the addition of power via media-dependent interface (MDI) to the IEEE 802.3af Standard, all data terminal equipment (DTE) now has the option to receive power over existing cabling that is used for data transmission. The IEEE 802.3af Standard defines the requirements associated with providing and receiving power over the existing cabling. The power sourcing equipment (PSE) provides the power on the cable and the powered device (PD) receives the power. As part of the IEEE 802.3af Standard, the interface between the PSE and PD is defined as it relates to the detection and classification protocol.

POWER SOURCING EQUIPMENT DETECTION OF A POWERED DEVICE

A powered device (PD) draws power or requests power by participating in a PD detection algorithm. This algorithm requires the power sourcing equipment (PSE) to probe the link looking for a valid PD. The PSE probes the link by sending out a voltage between 2.8 V and 10 V across the power lines. A valid PD detects this voltage and places a resistance of between 23.75 kΩ and 26.25 kΩ across the power lines. Naturally, the current varies depending on the input voltage. On detecting this current, the PSE concludes that a valid PD is connected at the end of the ethernet cable and is requesting power.

If the powered device (PD) is in a state in which it does not accept power, the PD is required to place a resistance above or below the values listed for a valid PD. On the lower end, a range between 12 kΩ and 23.75 kΩ signifies that the PD does not require power. On the higher end, the range is defined to be between 26.25 kΩ and 45 kΩ . Any resistance value less than 12 kΩ and greater than 45 kΩ, is interpreted by the PSE as a nonvalid PD detection signature.

The TPS2370 participates in the detection algorithm by activating an internal FET, which connects the DET pin of the device to VEE. As a result, any resistance connected between VDD and the DET pin of the TPS2370 is, in effect, across the power lines. This internal FET is active only when input power to the PD is between 2.8 V and 10 V.

POWER SOURCING EQUIPMENT CLASSIFICATION OF A POWERED DEVICE

After the detection phase, the PSE can optionally initiate a classification of the PD. The classification of a PD is used by the PSE to determine the maximum power required by the PD during normal operation. Five different levels of classification are defined by the IEEE 802.3af Standard. These levels are shown in Table 2.

Table 2. Powered Device Classification Levels

CLASS	USAGE	POWER DEVICE POWER (W)		CLASSIFICATION CURRENT (mA)	
		MIN	MAX	MIN	MAX
0	Default	0.44	12.95	0	4
1	Optional	0.44	3.84	9	12
2	Optional	3.84	6.49	17	20
3	Optional	6.49	12.95	26	30
4	Not allowed	reserved for future use		36	44

Classification of the PD is optionally performed by the PSE only after a valid PD has been detected. To determine PD classification, the PSE increases the voltage across the power lines to between 15.5 V and 20.5 V. The amount of current drawn by the PD determines the classification (see Table 2).

When the input voltage to the TPS2370 is between 14.0 V and 20.5 V, the TPS2370 uses an internal regulator to generate a fixed voltage on the CLASS pin. A resistor connected between the CLASS pin and VEE draws a fixed amount of current and thereby defines the classification level of the PD.

APPLICATION INFORMATION

POWER SOURCING EQUIPMENT POWER TO THE POWERED DEVICE

On completion of the detection and optional classification phases, the PSE ramps its output voltage above 42 V . Once the UVLO threshold has been reached, the internal FET is turned on. At this point, the PD begins to operate normally and it continues to operate normally as long as the input voltage remains above 30 V. For most PDs, this input voltage is down-converted using an onboard dc-to-dc converter to generate the required voltages.

The TPS2370 is designed to apply the PSE output voltage of 36 V to 57 V across the input of the onboard dc-to-dc converter. This is accomplished on the TPS2370 by turning on an internal pass FET located across the power return.

PROGRAMMING THE INRUSH CURRENT

During the initial turnon of the pass FET, an inrush current is created from the charging of the capacitance at the input of the dc-to-dc converter. According to the IEEE 802.3af specification, if the input capacitance is less than 180 μF, the PSE limits the inrush current. If the input capacitance is greater than 180 μF, the IEEE 802.3af specification requires the PD to limit the inrush current to less than 400 mA.

In order to satisfy the IEEE 802.3af requirements, the TPS2370 has been designed for a typical current limit of 450 mA. This current limit setting satisfies the normal operation requirements as well as the inrush requirements for a capacitive load of 180 μF or less. If a larger load capacitor is desired, the TPS2370 has been designed with a programmable inrush current limit feature. This feature allows the designer the option of using a capacitor larger than 180 μF. Note that the inrush current feature may also be used to lower voltage drops in the cabling between the PSE and the PD during start-up.

The programmable inrush current limit has a range of 50 mA to 449 mA. The limit is set by connecting an external resistor from ILIM (pin 1) to VEE (pin 4) of the TPS2370. Equation (1) shows the calculation for the programmable inrush current limit.

$$I_{INRUSH} = 450\ mA - \left(\frac{25\ k\Omega}{R_{LIM}}\right) \times (1\ A) \qquad (2)$$

where R_{LIM} is a value between 63.5 kΩ and 25 MΩ.

USING EN_DC AS A SOFT-START OR A POWER-GOOD FUNCTION

The EN_DC pin is an output intended for use as a soft-start for a dc-to-dc converter. During the initial turnon of the pass FET, an internal 80-μA current sink is enabled on the EN_DC pin. This internal current sink is removed only after the load capacitance has been charged to within 1.5-V of the supply voltage. By connecting the EN_DC output to the soft-start capacitor of a dc-to-dc converter, the internal current sink keeps the dc-to-dc converter off during start-up. Once the voltage across the converter has reached within 1.5 V of full voltage, the dc-to-dc converter is allowed to soft start.

For operation as a power-good output, the EN_DC requires an external pull-up resistor. A 1-MΩ resistor is recommended. The EN_DC output also requires a clamp to limit the output voltage to within recommended operating levels. A 5-V zener diode connected between EN_DC and RTN (pin 5 of the TPS2370) is recommended. This configuration allows the EN_DC pin to act as an open-drain output with which many designers are more familiar.

APPLICATION INFORMATION

SURGE SUPPRESSION

As specified in the *Absolute Maximum Ratings* table, the absolute maximum input voltage of the TPS2370 is 68 V. The IEEE 802.3af Power-over-Ethernet Standard specifies the voltage range of PSE output as between 44 V and 57 V. This PSE output voltage range would be reduced by cable, connector, and other IR drops between the PSE and the TPS2370 in the PD. However, the use of extended cable lengths and transformers in some applications may induce transients in excess of 68 V during a hot plug event. To manage these transient events and keep them from significantly exceeding the application's maximum voltage, a transorb such as the SMAJ54A should be placed between the positive input supply, VDD (pin 8), and the negative input supply, VEE (pin 4). This, combined with a 0.1-μF bypass capacitor in parallel with the transorb, helps to protect the TPS2370 from damage caused by transients during hot plug events. The transorb or zener diode should be selected such that it does not zener below the maximum required application voltage of 57 V, but before reaching the 68-V absolute maximum rating. For layout purposes, the 0.1-μF capacitor should be placed as close as possible to the device; the transorb or zener diode should be placed as close to the supply connector as possible. Based on the nature of the PD application, these measures should be considered an implementation requirement.

USE OF BARREL RECTIFIERS

Many applications use barrel rectifiers after the RJ-45 connector in order to be polarity insensitive. Barrel rectifiers in front of the TPS2370 cause the voltages at the device to be lower than the voltages at the RJ-45. The TPS2370 allows for this and is IEEE802.3af compliant during the detection and classification phases. For the detection phase, the device begins detection for voltages as low as 1.3 V across the supply pins. For the optional classification phase, the device is guaranteed to start classification below 14 V across the supply pins. Once classification has been engaged, it becomes latched-in and further voltage drops due to cable resistance and class current does not cause it to switch out of classification. Thus, the TPS2370 allows for at least a 1.5-V drop between the RJ-45 and the TPS2370 due to barrel rectifiers during both detection and classification phases.

However, in cases where the PSE is operating at the minimum class voltage (15.5 V) and there is a 20-Ω, 100-m cable between the PSE and the PD, class 3 devices may not classify correctly when using barrel rectifiers. Class 3 device designs should include Schottky diodes to handle all corner cases, or switch to class 0 devices when using barrel rectifiers.

THERMAL SHUTDOWN

In the event of a short circuit or overload condition, the TPS2370 begins to heat up until thermal shutdown is reached. Once thermal shutdown is reached, the internal FET is switched off, removing the load from the supply. After the device has cooled sufficiently, it retries by restarting the internal FET. If the overload or short is not removed, the device cycles thermal shutdown seven times before latching the internal FET off. Once the internal FET is latched off, power needs to be cycled to reset the latch.

APPLICATION INFORMATION

Figure 1 shows an application where 40 V < V_{IN} < 57 V. In this case, the brick supply is greater then 40 V and goes through TPS2370.

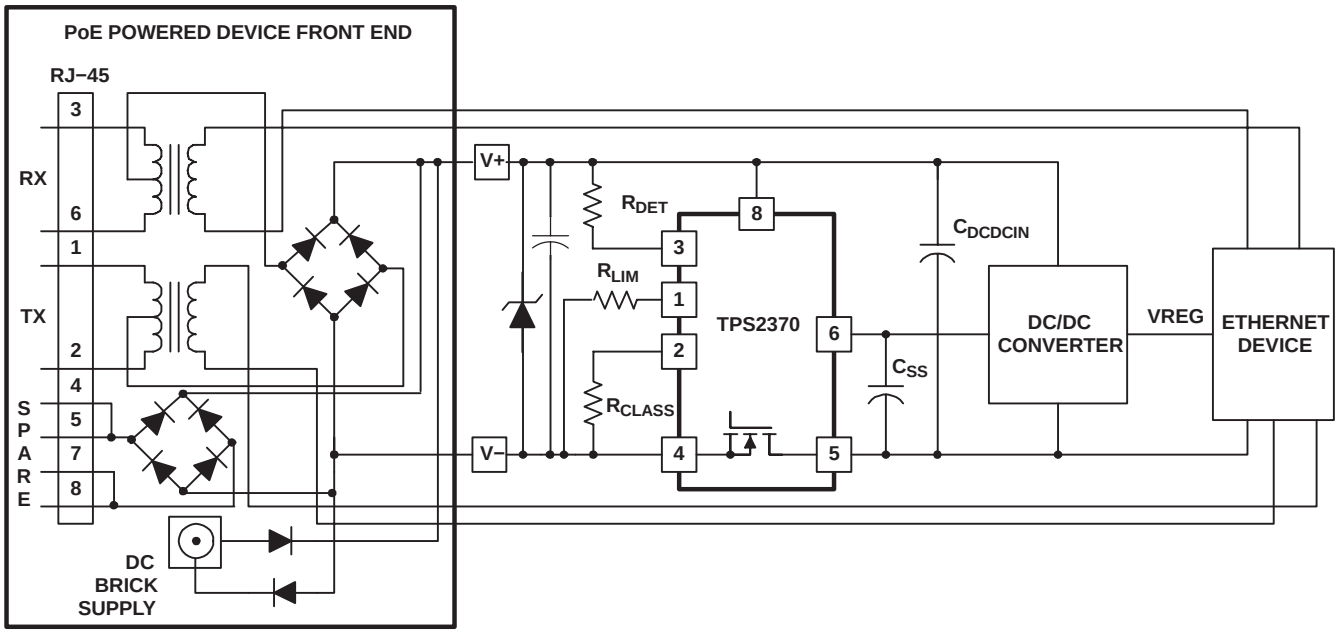


Figure 1. For Applications 40 V < V_{IN} < 57 V.

Figure 2 shows an application where V_{IN} < 40 V. In this application, the brick supply is bypassing the switch. Consequently, the dc-to-dc converter can operate from any voltage. However, for V_{BRICK} < 23 V, a class 0 resistor (R_{CLASS} = 4.42 kΩ) is recommended. This minimizes the power dissipation in TPS2370 if V_{BRICK} falls in the classification voltage range (15 V to 20 V). The 80-µA current sink on EN_DC pin is enabled only if VDD > 40 V.

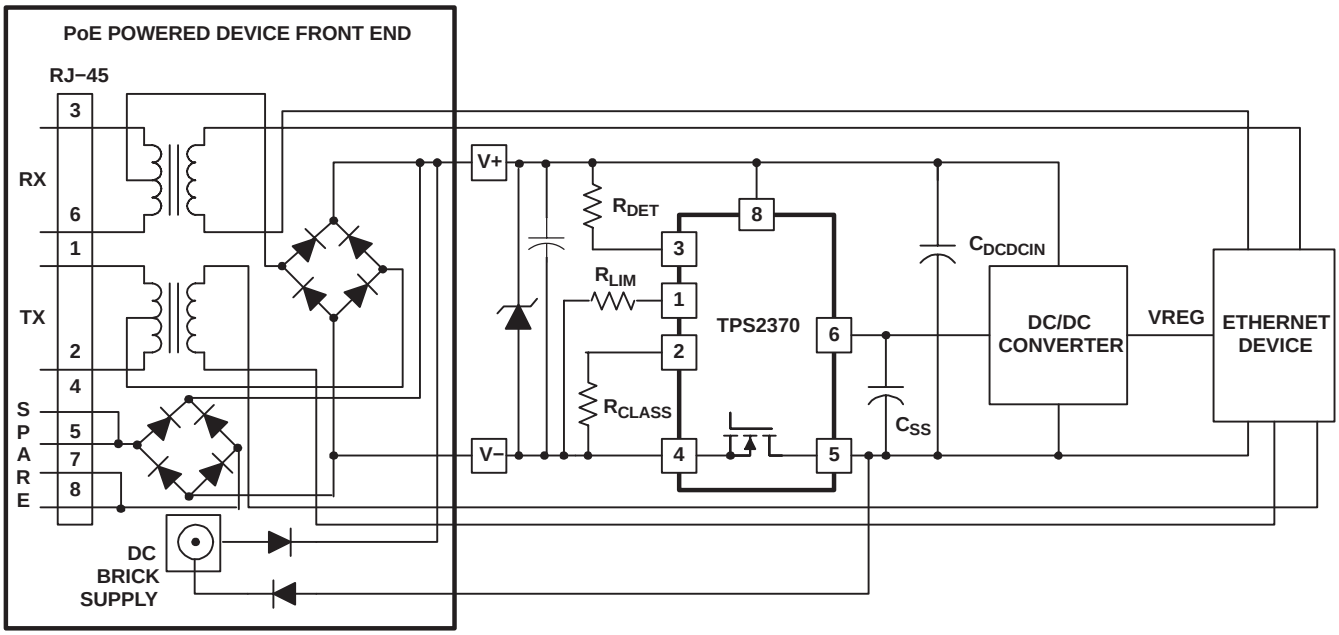


Figure 2. For Applications V_{IN} < 40 V.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS2370PW	NRND	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2370
TPS2370PW.A	NRND	Production	TSSOP (PW) | 8	150 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2370
TPS2370PWR	NRND	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2370
TPS2370PWR.A	NRND	Production	TSSOP (PW) | 8	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	0 to 70	2370

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

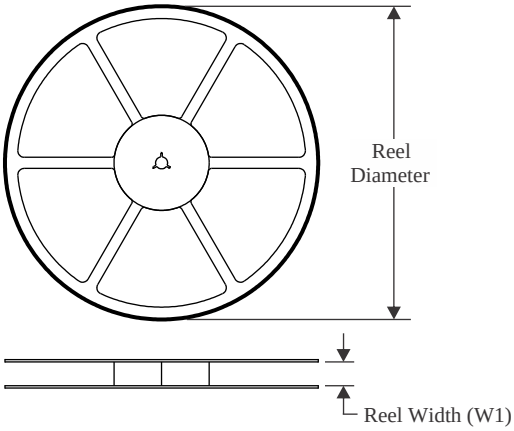
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

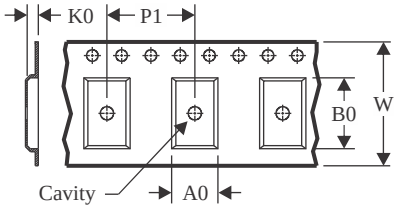
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

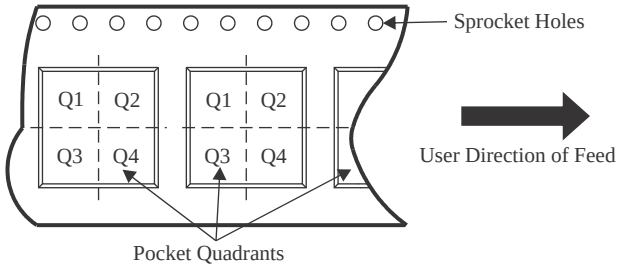


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

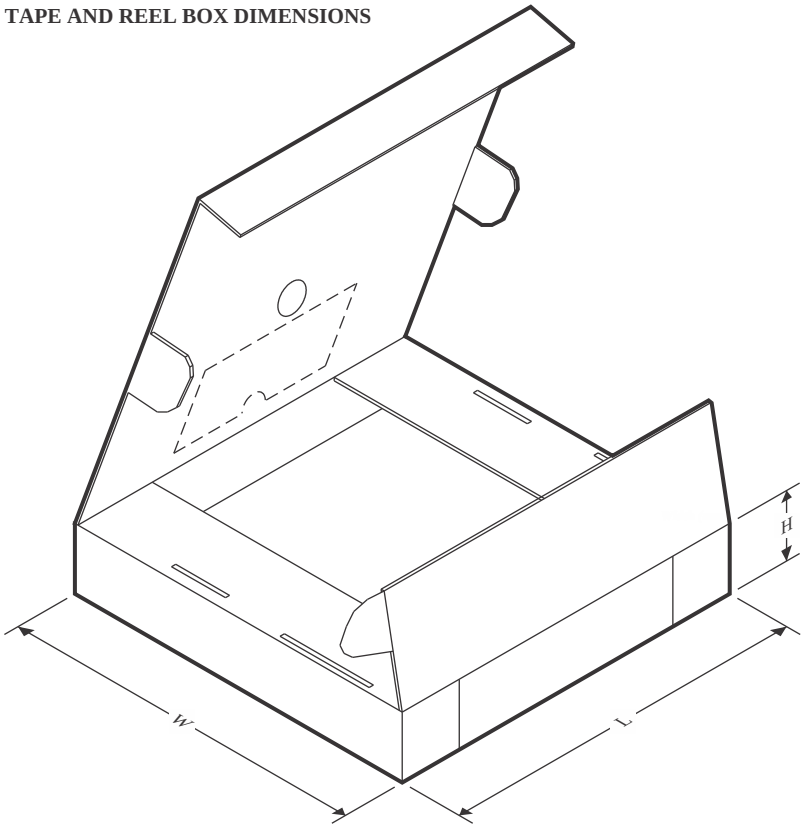
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS2370PWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1

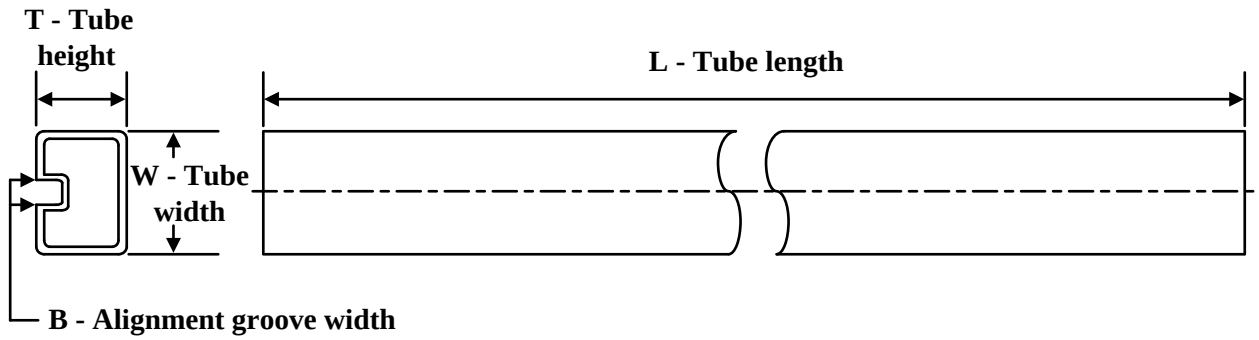
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS2370PWR	TSSOP	PW	8	2000	353.0	353.0	32.0

TUBE



*All dimensions are nominal

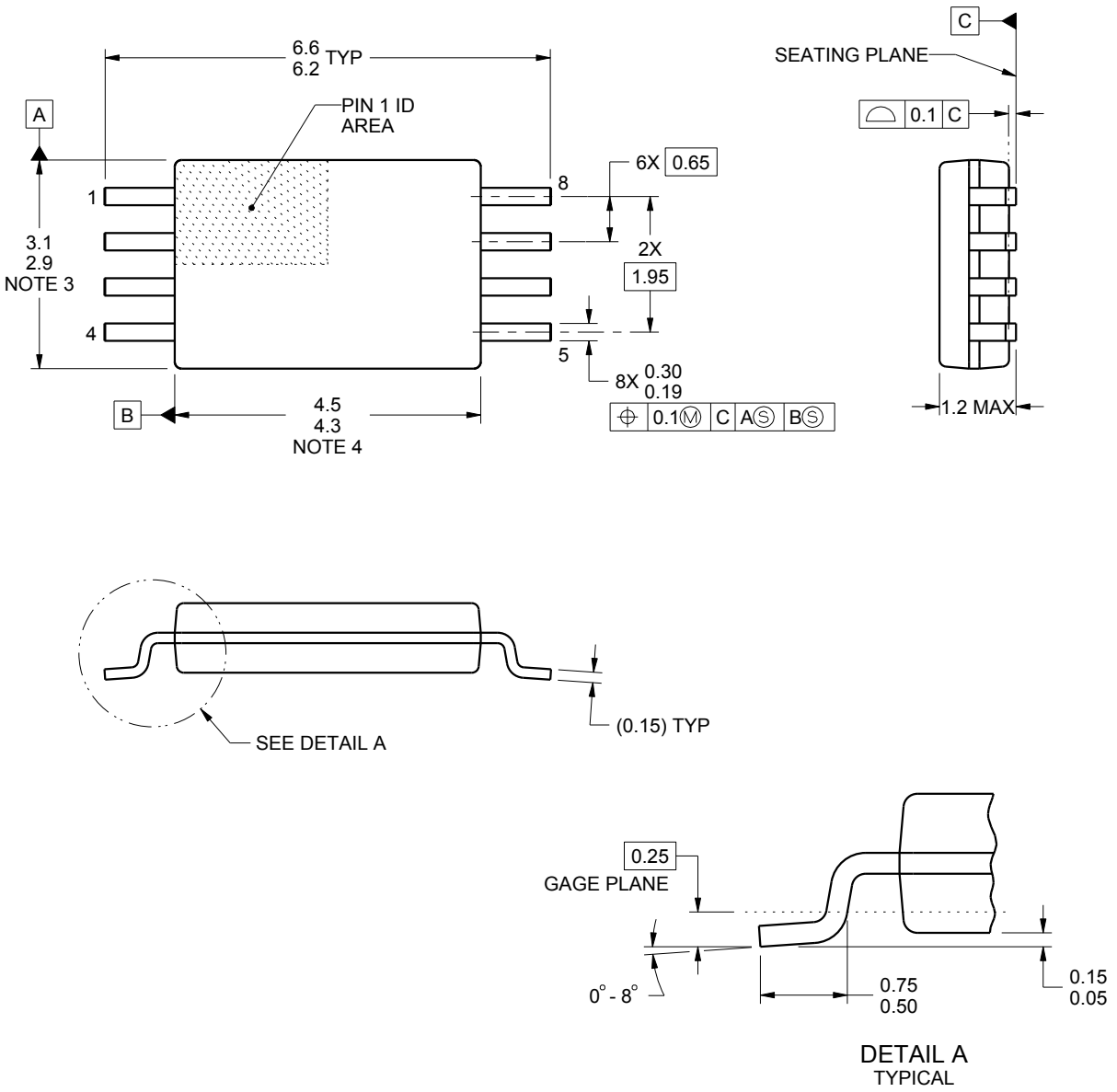
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS2370PW	PW	TSSOP	8	150	530	10.2	3600	3.5
TPS2370PW.A	PW	TSSOP	8	150	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0008A

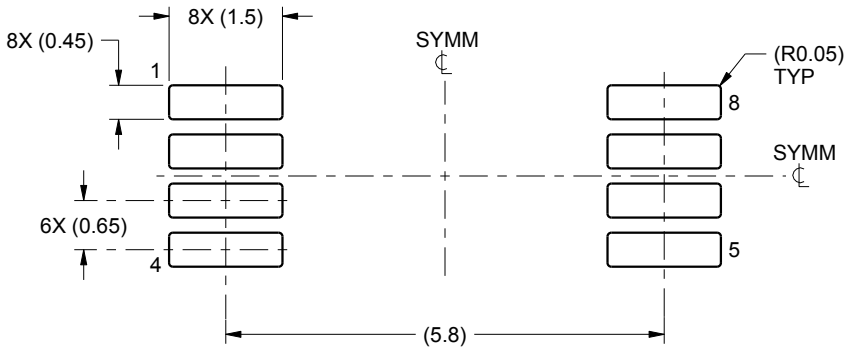
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

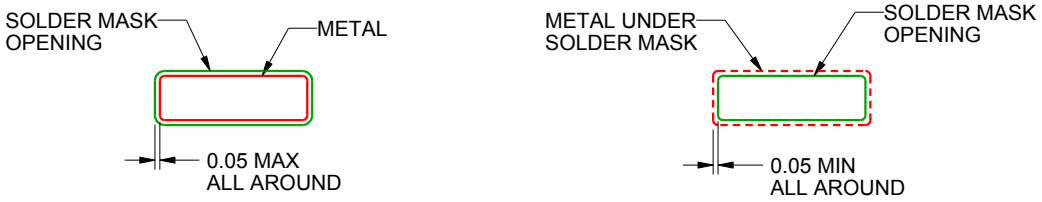


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

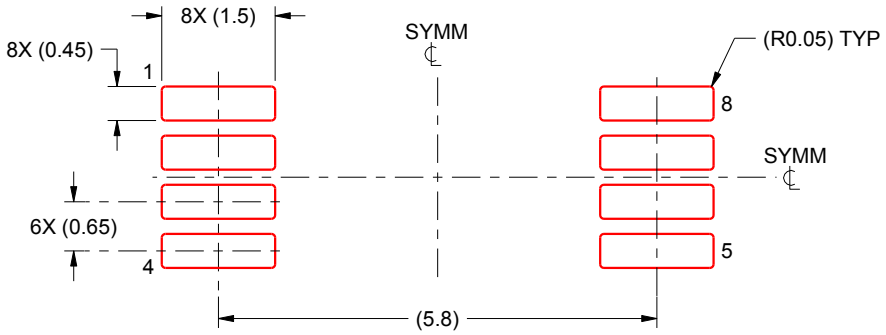


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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