

Ordering Information

Device Set Order ID	Package Type	Package	Operating Temperature
AD1882JCPZ*	QFN	48-Lead QFN, 7x7 mm	0°C to 70°C
*Lead-free (Pb Free) and RoHS compliant			

Revision History

Revision	Date	Description
A	February 27, 2009	Initial release

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High Definition Audio SoundMAX Codec

The AD1882 is available in a 48-lead RoHS compliant lead frame chip scale package in both reels and trays. See the Ordering Information table on the previous page.

The diagram illustrates the internal architecture of the HD Audio Interface. On the left, the "HD Audio Interface" block connects to several internal components:

- Digital PCBeep**: A small rectangular block at the top.
- DAC0, DAC1, DAC2**: Three Digital-to-Analog Converters arranged vertically.
- ADC0, ADC1**: Two Analog-to-Digital Converters at the bottom.

In the center, there are six circular summing junctions (Σ) stacked vertically. The inputs to these junctions include signals from the DACs, the Digital PCBeep, and feedback loops from the outputs. Specifically, the top four junctions receive inputs from DAC0, DAC1, and DAC2. The fifth junction receives input from DAC0 and DAC1. The sixth junction receives input from DAC0.

On the right side, the outputs are connected to various ports:

- Port F**, **Port D**, **Port G**, **MONO OUT**, **Port A**, **Port C**, **Port E**, **PCBeep**, **Port B**, and **CD IN**.

Some output paths include additional processing blocks such as inverters (triangles) or HP filters (circles labeled "HP"). For example, the signal to Port A passes through an HP filter before reaching the port.

- ◆ 2 stereo headphone amplifiers
- ◆ Microsoft Vista Premium logo for notebook and desktop
- ◆ 95 dB audio outputs, 90 dB audio inputs
- ◆ Internal 32-bit arithmetic for greater accuracy
- ◆ Impedance and presence detection on all jack pins
- ◆ Digital synthesis PCBeep
- ◆ C/LFE channel swapping
- ◆ 2 General-Purpose I/O (GPIO) Digital pins
- ◆ Advanced power management modes
- ◆ EAPD control for internal speakers
- ◆ 48-lead, Pb-free QFN package
- ◆ Six 96 kHz DACs
 - 3 independent stereo DAC pairs
 - Independent 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz sample rates
 - 16-, 20-, and 24-bit PCM resolution
 - Selectable stereo mixer on outputs
- ◆ Four 96 kHz ADCs
 - 2 independent stereo ADC pairs
 - Simultaneous record of up to 4 channels
 - Independent 8 kHz, 11.025 kHz, 16 kHz, 22.05 kHz, 32 kHz, 44.1 kHz, 48 kHz, 88.2 kHz, and 96 kHz sample rates
 - 16-, 20-, and 24-bit resolution
- ◆ S/PDIF Output
 - Supports 44.1 kHz, 48, kHz 88.2 kHz, and 96 kHz sample rates
 - 16-, 20-, and 24-bit data widths; PCM and AC3 formats
 - Digital PCM gain control
- ◆ Dedicated Auxiliary Pins
 - Stereo CD input w/GND sense
 - Mono out pin for internal speakers or telephony
 - Analog PCBeep input pin

Contents

1	High Definition Audio SoundMAX Codec	7
1.1	Jack Configuration	7
1.2	Specifications	8
1.2.1	HD Audio Link Specifications	12
1.2.2	Absolute Maximum Ratings	13
1.2.3	Environmental Conditions	13
1.3	Pin Configuration and Functional Descriptions	14
1.4	HD Audio Widgets	17
1.5	HD Audio Parameters	19
1.6	Package Dimensions	20

Figures

Figure 1.	AD1882 Pinout	14
Figure 2.	Package Dimensions	20

Tables

Table 1.	Typical Desktop Configuration with Discreet Jacks	7
Table 2.	Typical Desktop Configuration with 5.1 on 3 Jacks	7
Table 3.	Typical Notebook Configuration	8
Table 4.	Test Conditions	8
Table 5.	Performance	8
Table 6.	AD1882 General Specifications	9
Table 7.	Power-Down States	12
Table 8.	Absolute Maximum Ratings	13
Table 9.	Pin Descriptions	15
Table 10.	HD Audio Widgets	17
Table 11.	Root and Function Node Parameters	19
Table 12.	Subsystem ID	19
Table 13.	Default Configuration Bytes	19

High Definition Audio SoundMAX Codec

This data sheet provides a general overview of the AD1882 SoundMAX codec's architecture and functionality. Additional information on the AD1882 is available in the *AD1882 Programmers Reference Manual*. Please contact your local Conexant sales representative for more information.

1.1 Jack Configuration

Use the guidelines shown in [Tables 1](#) through [3](#) when selecting ports for particular functions.

Table 1. *Typical Desktop Configuration with Discreet Jacks*

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In
Port D	Rear Panel Line-Out/Headphone
Port E	Rear Panel Microphone
Port F	Rear Panel Surround
Port G	Rear Panel C/LFE

Table 2. *Typical Desktop Configuration with 5.1 on 3 Jacks*

Port	Function
Port A	Front Panel Headphone
Port B	Front Panel Microphone
Port C	Rear Panel Line-In/Surround
Port D	Rear Panel Line-Out/Headphone
Port E	Rear Panel Microphone / C/LFE

Table 3. Typical Notebook Configuration

Port	Function
Port A	Headphone
Port B	Microphone
Port C	Internal Microphone
Port D	Internal Stereo Speakers
Port E	Docking Station Line-In/Microphone

1.2 Specifications

Table 4. Test Conditions

Parameter	Test Condition
Temperature	25°C
Digital Supply	3.3 V
Analog Supply	3.3 V
MIC_BIAS_IN (via Low-Pass Filter)	5.0 V
Sample Rate f_s	48 kHz
Input Signal (Frequency Sine Wave)	1008 Hz
Amplitude for THD + N	−3.0 dB Full Scale
Analog Output Pass Band	20 Hz to 20 kHz
DAC	10 k Ω Output Load: Line Out Tests 32 Ω Output Load: Headphone Tests
ADC	0 dB Gain

Table 5. Performance

Parameter	Min	Typ	Max	Unit
Line-Out Drive (10 k Ω Loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		−85		dB
Dynamic Range (−60 dB in Ref to f_s A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Headphone Drive (32 Ω Loads—DAC to Pin)				
Total Harmonic Distortion (THD + N)		−83		dB
Dynamic Range (−60 dB in Ref to f_s A-Weighted)		95		dB
Signal-to-Noise Ratio		95		dB
Input Ports (Pin to ADC, Mic Boost = 0 dB)				
Total Harmonic Distortion (THD + N)		−81		dB
Dynamic Range (−60 dB in Ref to f_s A-Weighted)		90		dB
Signal-to-Noise Ratio		90		dB

Table 6. AD1882 General Specifications (1 of 3)

Parameter	Min	Typ	Max	Unit
Digital Decimation and Interpolation Filters—$f_s = 8 \text{ kHz to } 192 \text{ kHz}^{(1)}$				
Pass Band	0		$0.4 f_s$	Hz
Pass-Band Ripple			± 0.005	dB
Stop Band	$0.6 f_s$			Hz
Stop-Band Rejection			-100	dB
Group Delay		+20		$1/f_s$
Group Delay Variation Over Pass Band		0		μs
Analog-to-Digital Converters				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage) ⁽²⁾			± 10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			± 0.5	dB
ADC Offset Error ⁽¹⁾			± 5	mV
ADC Crosstalk ⁽¹⁾				
Line Inputs (Input L, Ground R, Read R; Input R, Ground L, Read L)		-85		dB
Line Inputs to Other		-100	-80	dB
Digital to Analog Converters				
Resolution		24		Bits
Gain Error (Full-Scale Span Relative to Nominal Input Voltage) ⁽¹⁾			± 10	%
Interchannel Gain Mismatch (Difference of Gain Errors)			± 0.5	dB
Total Audible Out-of-Band Energy (Measured from $0.6 \times f_s$ to 100 kHz) ⁽¹⁾		-85		dB
DAC Crosstalk (Input L, Zero R, Read R_OUT; Input R, Zero L, Read L_OUT) ⁽¹⁾		-95		dB
DAC Volumes				
Step Size (DAC-0, DAC-1, DAC-2)		1.5		dB
Output Gain/Attenuation Range	-58.5		0	dB
Mute Attenuation of 0 dB Fundamental ⁽¹⁾		-80		dB
ADC Volumes				
Step Size (ADCSEL-0, ADCSEL-1)		1.5		dB
PGA Gain/Attenuation Range	-58.5		+22.5	dB
Mute Attenuation of 0 dB Fundamental ⁽¹⁾		-80		dB

Table 6. AD1882 General Specifications (2 of 3)

Parameter		Min	Typ	Max	Unit
Analog Mixer					
Signal-to-Noise Ratio (SNR) Input to Output			95		dB
CD to Port D Output			95		dB
Port B, C, or E to Port D Output			95		dB
Port A to Port D Output			95		dB
Port D to Port A Output			95		dB
Step Size: All Mixer Inputs			1.5		dB
Input Gain/Attenuation Range: All Mixer Inputs		-34.5		+12.0	dB
Analog Line Level Outputs					
Full-Scale Output Voltage		1.0	1.0		V _{rms} ⁽²⁾
Ports C, E, F, and G Mono Out		2.83			V p-p
	Output Impedance ⁽¹⁾			300	Ω
	External Load Impedance ⁽¹⁾	10			kΩ
	Output Capacitance ⁽¹⁾		15		pF
	External Load Capacitance ⁽¹⁾			1000	pF
Analog HP Drive Outputs					
Full-Scale Output Voltage		1.0			V _{rms} ⁽³⁾
Ports A and D		2.83			V p-p
	Output Impedance ⁽¹⁾			0.5	Ω
	External Load Impedance ⁽¹⁾	32			Ω
	Output Capacitance ⁽¹⁾		15		pF
	External Load Capacitance ⁽¹⁾			1000	pF
Analog Inputs					
CD, Port D (When Used as Input)			1 2.83		V _{rms} ⁽³⁾ V p-p
Microphone Boost Amplifier, Ports B, C, or E (When Used as Inputs)	Boost = 0 dB		1 2.83		V _{rms} ⁽³⁾ V p-p
	Boost = 10 dB		0.316 0.894		V _{rms} ⁽³⁾ V p-p
	Boost = 20 dB		0.1 0.283		V _{rms} ⁽³⁾ V p-p
	Boost = 30 dB		0.032 0.089		V _{rms} ⁽³⁾ V p-p
Input Impedance ⁽¹⁾			20		V _{rms} ⁽³⁾ V p-p
Input Capacitance ⁽¹⁾			5	7.5	pF

Table 6. AD1882 General Specifications (3 of 3)

Parameter		Min	Typ	Max	Unit
Digital GPIO Pins: GPIO_0, GPIO_1/EAPD					
Input Signal High (V_{IH})		$DV_{IO} \times 0.60$		DV_{IO}	V
Input Signal Low (V_{IL})		0		$DV_{IO} \times 0.24$	V
Input Leakage Current (Signal High, (I_{IH}))			150		nA
Input Leakage Current (Signal Low, (I_{IL}))			50		μ A
Output Signal High (V_{OH})	$I_{OUT} = -500 \mu$ A	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	$I_{OUT} = +1500 \mu$ A	0		$DV_{IO} \times 0.10$	V
S/PDIF_OUT					
Output Signal High (V_{OH})	$I_{OUT} = -500 \mu$ A	$DV_{IO} \times 0.72$		DV_{IO}	V
Output Signal Low (V_{OL})	$I_{OUT} = +1500 \mu$ A	0		$DV_{IO} \times 0.10$	V
Power Supply					
Analog (AV_{DD}) 3.3 V $\pm$ 5%					
Power Supply Range		3.13	3.30	3.46	V
Power Dissipation			116		mW
Supply Current			35		mA
Digital (DV_{DD}) 3.3 V $\pm$ 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			162		mW
Supply Current			49		mA
Digital I/O (DV_{IO}) 3.3 V $\pm$ 10%					
Power Supply Range		2.97	3.30	3.63	V
Power Dissipation			3.96		mW
Supply Current			1.20		mA
Power Supply Rejection (100 mV p-p Signal @ 1 kHz) ⁽¹⁾			80		dB
FOOTNOTES:					
⁽¹⁾ Guaranteed but not tested.					
⁽²⁾ Measurements reflect ADC.					
⁽³⁾ RMS values assume sine wave input.					

1.2.1 HD Audio Link Specifications

HD Audio signals comply with the High Definition Audio specifications. Please refer to these specifications at www.intel.com/standards/hdaudio.

Table 7. Power-Down States

Parameter	ID _{VDD} Typ	IA _{VDD} Typ	Unit
Function Node In D0, All Nodes Active	49	35	mA
Function Node in D3	16	0.7	mA
Codec in $\overline{\text{RESET}}$	3	3	mA
Individual block power savings			
DAC Pair Powered Down Saves (Each)	6	6	mA
ADC Pair Powered Down Saves (Each)	5	4.4	mA
Mixer Power Control (and Associated Amps) Saves	0	3	mA
MIC_BIAS Powered Down Saves ⁽¹⁾	0	1.0	mA
FOOTNOTES: ⁽¹⁾ Powering down the MIC_BIAS powers down all port MIC_BIAS pins. This disables all microphone bias circuits set to 100% or 50%, setting them to the high-Z state. The 0 Ω and high-Z states remain unaffected by the MIC_BIAS power state.			

1.2.2 Absolute Maximum Ratings

Stresses greater than those listed below may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 8. Absolute Maximum Ratings

Power Supplies	Rating
Digital (DV _{DD})	−0.30 V to +3.65 V
Digital I/O (DV _{IO})	−0.30 V to +3.65 V
Analog (AV _{DD})	−0.30 V to +3.65 V
Input Current (Except Supply Pins)	±10.0 mA
Analog Input Voltage (Signal Pins)	−0.30 V to AV _{DD} + 0.3 V
Digital Input Voltage (Signal Pins)	−0.30 V to DV _{IO} + 0.3 V
Ambient Temperature (Operating)	0°C to +70°C
Storage Temperature	−65°C to +150°C



Electrostatic Discharge Device (ESD)

Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

1.2.3 Environmental Conditions

Ambient Temperature Rating:

$$T_{AMB} = T_{CASE} - (PD \times \theta_{CA})$$

T_{CASE} = case temperature in °C

PD = power dissipation in W

θ_{CA} = thermal resistance (case-to-ambient)

θ_{JA} = thermal resistance (junction-to-ambient)

θ_{JC} = thermal resistance (junction-to-case)

All measurements per EIA-JESD51 with 2S2P test board per EIA-JESD51-7.

Package	θ _{JA}	θ _{JC}	θ _{CA}	Unit
QFN	47	15	32	°C/W

1.3 Pin Configuration and Functional Descriptions

Figure 1. AD1882 Pinout

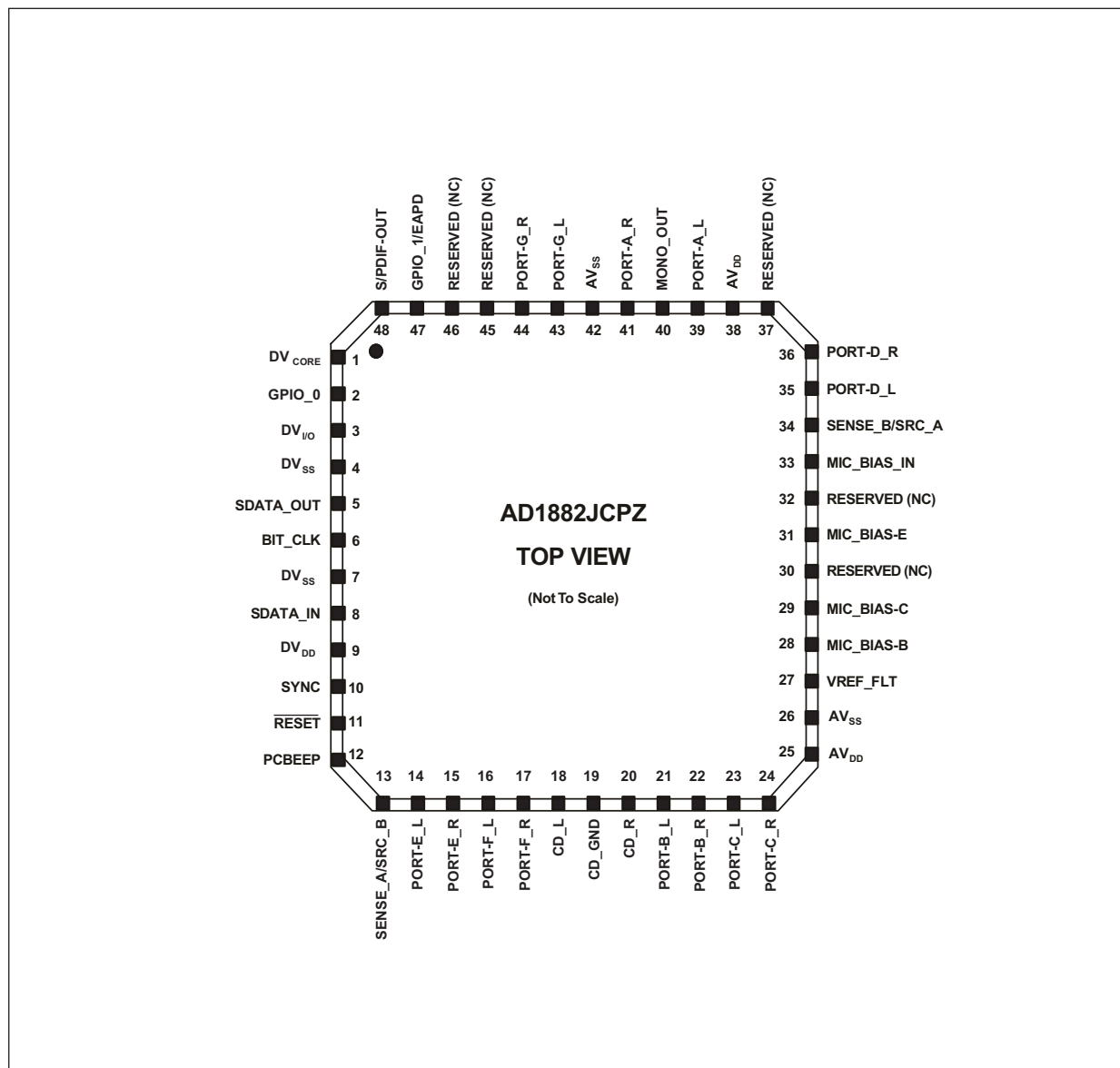


Table 9. Pin Descriptions (1 of 2)

Mnemonic	Pin No.	Function	Description
Digital Interface			
SDATA_OUT	5	I	Link Serial Data Output. AD1882 input stream. Clocked on both edges of the BIT_CLK.
BIT_CLK	6	I	Link Bit Clock. 24.000 MHz serial data clock.
SDATA_IN	8	I/O	Link Serial Data Input. AD1882 output stream Clocked only on one edge of BIT_CLK.
SYNC	10	I	Link Frame Sync.
RESET	11	I	Link Reset. AD1882 master hardware reset
Digital I/O			
GPIO_0	2	I/O	General-Purpose Input/Output Pin. Digital signal used to control external circuitry.
GPIO_1/EAPD	47	I/O	General-Purpose Input/Output Pin/EAPD Pin. Digital signal used to control external circuitry. Defaults to high-Z. When used as EAPD: high-Z = amp-on, DV _{SS} = amp off.
SPDIF_OUT	48	O	S/PDIF_OUT. Supports S/PDIF output.
JACK SENSE and EAPD			
SENSE_A/SRC_B	13	I/O	JACK SENSE A-D Input/Sense B Drive.
SENSE_B/SRC_A	34	I/O	JACK SENSE E-H Input/Sense A Drive.
Analog I/O			
PCBEEP	12	LI	Monaural Input from System for Analog PCBeep.
PORT-E_L	14	LI, MIC, LO, SWAP	Auxiliary Input/Output Left Channel.
PORT-E_R	15	LI, MIC, LO, SWAP	Auxiliary Input/Output Right Channel.
PORT-F_L	16	I/O	Auxiliary Input/Output Left Channel.
PORT-F_R	17	I/O	Auxiliary Input/Output Right Channel.
CD_L	18	LI	CD Audio Left Channel.
CD_GND	19	LI	CD Audio Analog Ground Reference (for Differential CD Input). Must be connected to AGND via 0.1 mF capacitor if not in use as CD_GND.
CD_R	20	LI	CD Audio Right Channel.
PORT-B_L	21	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-B_R	22	LI, MIC, HP, LO	Front Panel Stereo MIC/Line-In.
PORT-C_L	23	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.
PORT-C_R	24	LI, MIC, LO	Rear Panel Stereo MIC/Line-In.

Table 9. Pin Descriptions (2 of 2)

Mnemonic	Pin No.	Function	Description
Analog I/O (continued)			
PORT-D_L	35	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-D_R	36	LI, HP, LO	Rear Panel Headphone/Line-Out.
PORT-A_L	39	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
MONO_OUT	40	LO	Monaural Output to Internal Speaker or Telephony Subsystem Speakerphone.
PORT-A_R	41	LI, MIC, HP, LO	Front Panel Headphone/Line-Out.
PORT-G_L	43	LO, SWAP	Rear Panel C/LFE Output.
PORT-G_R	44	LO, SWAP	Rear Panel C/LFE Output.
Filter/Reference			
MIC_BIAS-B	28	O	Switchable Microphone Bias. For use with Port B (Pins 21, 22).
MIC_BIAS-C	29	O	Switchable Microphone Bias. For use with Port C (Pins 23, 24).
MIC_BIAS-E	31	O	Switchable Microphone Bias. For use with Port E (Pins 14, 15).
DV _{CORE}	1	O	CAUTION: DO NOT APPLY 3.3 V TO THIS PIN! Filter connection for internal core voltage regulator. This pin must be connected to filter caps: 10 μ F, 1.0 μ F, and 0.1 μ F connected in parallel between Pin 1 and DV _{SS} (Pin 4).
VREF_FLT	27	O	Voltage Reference Filter. This pin must be connected to filter caps: 1.0 μ F and 0.1 μ F connected in parallel between Pin 27 and AV _{SS} (Pins 26, 42).
Power And Ground			
DV _{I/O} (3.3V)	3	I	Connect to the I/O Voltage Used for the HD Audio Controller Signals.
DV _{SS}	4, 7	I	Digital Supply Return (Ground).
DV _{DD} (3.3 V)	9	I	Digital Supply Voltage 3.3 V. This is regulated down to DV _{CORE} on Pin 1 to supply the internal digital core internal to the AD1882.
AV _{DD} (3.3 V)	25, 38	I	CAUTION: DO NOT APPLY 5.0 V TO THESE PINS! Analog supply voltage 3.3 V ONLY. Note: AV _{DD} supplies should be well regulated and filtered as supply noise degrades audio performance.
MIC_BIAS_IN	33	I	Source Power for Microphone Bias Boost Circuitry.
AV _{SS}	26, 42	I	Analog Supply Return (Ground). AV _{SS} should be connected to DV _{SS} using a conductive trace under, or close to, the AD1882.

1.4 HD Audio Widgets

In [Table 10](#) below, node IDs that are not shown are reserved for future use.

Table 10. HD Audio Widgets (1 of 2)

Node ID	Name	Type ID	Type	Description
00	ROOT	x	Root	Device identification
01	FUNCTION	x	Function	Designates this device as an audio codec
02	S/PDIF DAC	0	Audio Output	S/PDIF digital stream output interface
03	DAC_0	0	Audio Output	Headphone/surround side (7.1) channel digital/audio converters
04	DAC_1	0	Audio Output	Stereo front channel digital/audio converters
05	DAC_2	0	Audio Output	Stereo C/LFE channel digital/audio converters
08	ADC_0	1	Audio Input	Stereo record channel 1 audio/digital converters
09	ADC_1	1	Audio Input	Stereo record channel 2 audio/digital converters
0B	S/PDIF Mix Selector	3	Audio Selector	Selects which ADC drives the S/PDIF mixer
0C	ADC Selector 0	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_0
0D	ADC Selector 1	3	Audio Selector	Selects and amplifies/attenuates the input to ADC_1
10	Digital Beep	7	Beep Generator	Internal digital PCBeep signal
11	Port A (Headphone)	4	Pin Complex	Front panel headphone/microphone jack
12	Port D (Front L/R)	4	Pin Complex	Rear panel front/headphone jack
13	Mono Out	4	Pin Complex	Monaural output pin (internal speakers or telephony system)
14	Port B (Front Mic)	4	Pin Complex	Front panel microphone/headphone jack
15	Port C (Line In)	4	Pin Complex	Rear panel line-in jack
16	Port F (Surr Back)	4	Pin Complex	Rear panel surround-rear (5.1) jack
17	Port E (Rear Mic)	4	Pin Complex	Rear panel mic jack
18	CD In	4	Pin Complex	Analog CD input
19	Mixer Power-Down	5	Power Widget	Powers down the analog mixer and associated amps
1A	Analog PCBeep	4	Pin Complex	External analog PCBeep signal input
1B	S/PDIF Out	4	Pin Complex	S/PDIF output pin
1D	S/PDIF Mixer	2	Audio Mixer	Mixes the selected ADC with the digital stream to drive S/PDIF out
1E	Mono Out Mixer	2	Audio Mixer	Selects which source drives the mono out signal
20	Analog Mixer	2	Audio Mixer	Mixes individually gainable analog inputs

Table 10. HD Audio Widgets (2 of 2)

Node ID	Name	Type ID	Type	Description
21	Mixer Output Atten	3	Audio Selector	Attenuates the mixer output to drive the Port mixers
22	Port A Mixer	2	Audio Mixer	Mixes the Port A selected DAC and mixer output amps to drive Port A
23	VREF Power-Down	F	Vendor Defined	Powers down the internal and external VREF circuitry
24	Port G (C/LFE)	4	Pin Complex	Rear panel C/LFE jack
26	Port E Mixer	2	Audio Mixer	Mixes DAC_1 and mixer output amps to drive Port E
27	Port G Mixer	2	Audio Mixer	Mixes DAC_1 and mixer output amps to drive Port G
29	Port D Mixer	2	Audio Mixer	Mixes DAC_0 and mixer output amps to drive Port D
2A	Port F Mixer	2	Audio Mixer	Mixes DAC_2 and mixer output amps to drive Port F
2C	Port C Mixer	2	Audio Mixer	Mixes the Port C selected DAC and mixer output amps to drive Port C
2D	Stereo Mix Down	2	Audio Mixer	Mixes the stereo L/R channels to drive mono output
2F	BIAS Power-Down	F	Vendor Defined	Powers down the internal MIC_BIAS_FILT and all MIC_BIAS pins
37	Port A Out Selector	3	Audio Selector	Selects the Port A DAC (0, 1)
39	Port B Boost	3	Audio Selector	Microphone boost amp for Port B
3A	Port C Boost	3	Audio Selector	Microphone boost amp for Port C
3C	Port E Boost	3	Audio Selector	Microphone boost amp for Port E

1.5 HD Audio Parameters

The SSID value is set on codec power-up only. SSID is not reset by link or soft reset in order to preserve modifications by BIOS control.

Table 11. Root and Function Node Parameters

Node ID	Name	Vendor ID 00	Revision ID 02 ⁽¹⁾	03	Sub Node Count 04	Func. Group Type 05	Audio F.G. Caps 08	GPIO Caps 11
00	ROOT	0x11D4 1882	0x0010 0300		0x0001 0001			
01	FUNCTION				0x0002 003B	0x0000 0001	0x0001 0C0C	0x4000 0002
FOOTNOTES: ⁽¹⁾ Subject to change with silicon stepping.								

Table 12. Subsystem ID

Node ID	Name	Type	Value	31:16 SSID	15:8 SKU	7:0 ASM ID
0x01	FUNCTION	Function	0xBF D2 0000	0xBF D2	0x00	0x00
GENERAL NOTES: 1. The default SSID is over-written by platform BIOS after power on. It is preserved across HD Audio link reset and verb reset.						

In [Table 13](#), default configuration values are set on codec power-up only. Default configuration values are not reset by link or soft reset to preserve modifications by BIOS control.

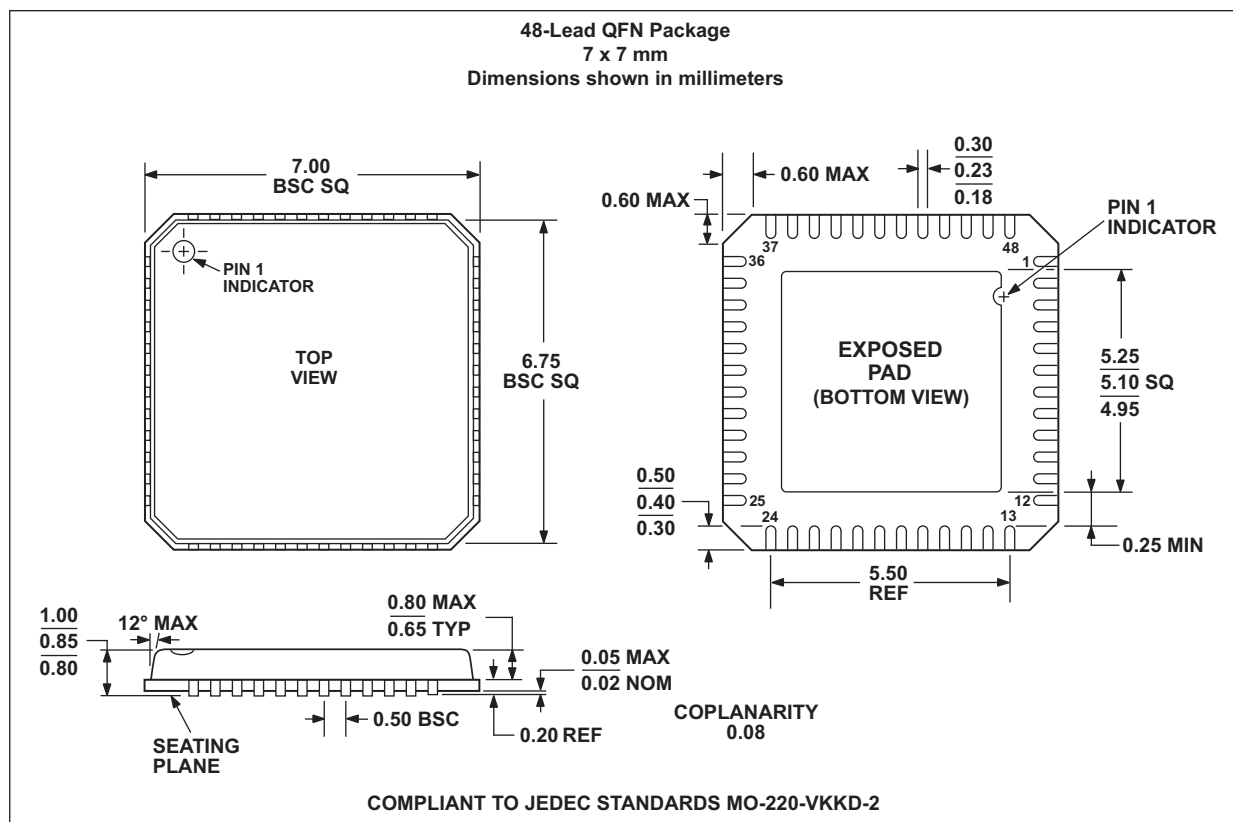
Table 13. Default Configuration Bytes

Name	Value	31:30	29:28	27:24	23:20	19:16	15:12	8	7:4	3:0
		Connectivity	Location		Def. Device	Conn Type	Color	Misc.	Def Assn	Sequence
			Chasis	Position				JD Over Ride		
Port A (Headphone)	0221401F	Jack	External	Front	HP Out	1/8" Jack	Green	0	1	F
Port D (Front L/R)	01014010	Jack	External	Rear	Line Out	1/8" Jack	Green	0	1	0
Mono Out	901701F0	Fixed	Internal	N/A	Speaker	Other Analog	Unknown	1	F	0
Port B (Front Mic)	02A190F0	Jack	External	Front	Mic In	1/8" Jack	Pink	0	F	0
Port C (Line In)	01813021	Jack	External	Rear	Line In	1/8" Jack	Blue	0	2	1
Port F (Surr Back)	01011012	Jack	External	Rear	Line Out	1/8" Jack	Black	0	1	2
Port E (Rear Mic)	01A19020	Jack	External	Rear	Mic In	1/8" Jack	Pink	0	2	0
CD IN	9933012E	Fixed	Internal	Special 3	CD	ATAPI	Unknown	1	2	E
Analog PCBeep	90F701F0	Fixed	Internal	N/A	Other	Other Analog	Unknown	1	F	0
S/PDIF Out	014511F0	Jack	External	Rear	SPDIF Out	Optical	Black	1	F	0
Port G (C/LFE)	01016011	Jack	External	Rear	Line Out	1/8" Jack	Orange	0	1	1

1.6 Package Dimensions

Figure 2 provides the package dimensions, shown in millimeters

Figure 2. Package Dimensions



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