

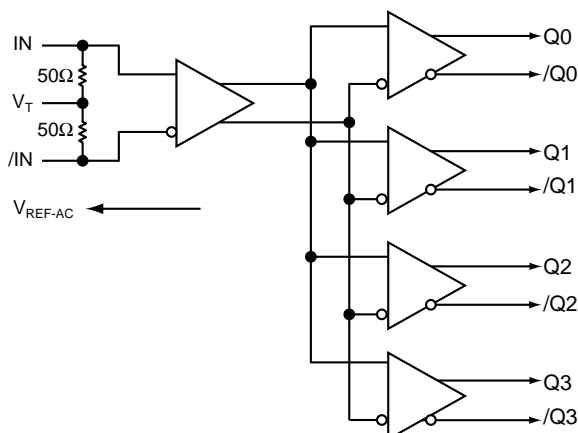
## FEATURES

- Precision 1:4, LVPECL fanout buffer
- Guaranteed AC performance over temperature/ voltage:
  - >4GHz  $f_{MAX}$  (clock)
  - <100ps  $t_r / t_f$  Times
  - <300ps  $t_{pd}$
  - <15ps max skew
- Low jitter performance
  - <10ps<sub>pp</sub> total jitter (clock)
  - <1ps<sub>rms</sub> random jitter (data)
  - <10ps<sub>pp</sub> deterministic jitter (data)
- Accepts an input signal as low as 100mV
- Unique input termination and VT pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML
- 100k LVPECL compatible 800mV swing output
- Power supply 2.5V ±5% and 3.3V ±10%
- -40°C to +85°C temperature range
- Available in 16-pin (3mm × 3mm) MLF™ package

## APPLICATIONS

- All SONET and All GigE clock distribution
- Fibre Channel clock and data distribution
- Backplane distribution
- High-end, low skew, multiprocessor synchronous clock distribution

## FUNCTIONAL BLOCK DIAGRAM



## DESCRIPTION

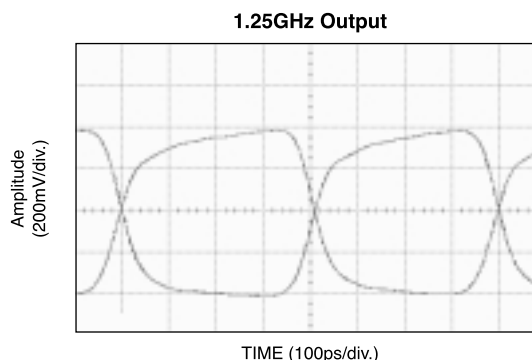
The SY58021U is a 2.5V/3.3V precision, high-speed, fully differential 1:4 LVPECL fanout buffer. Optimized to provide four identical output copies with less than 15ps of skew and less than 10ps<sub>pp</sub> total jitter, the SY58021U can process clock signals as fast as 4GHz.

The differential input includes Micrel's unique, 3-pin input termination architecture interfaces to differential LVPECL, CML, and LVDS signals (AC- or DC-coupled) as small as 100mV without any level-shifting or termination resistor networks in the signal path. For AC-coupled input interface applications, an on-board output reference voltage ( $V_{REF-AC}$ ) is provided to bias the VT pin. The outputs are 100k LVPECL compatible, with extremely fast rise/fall times guaranteed to be less than 100ps.

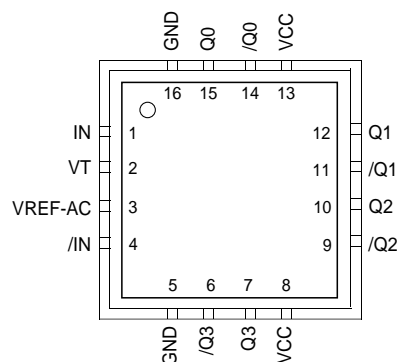
The SY58021U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (-40°C to +85°C). For applications that require faster rise/fall times, or greater bandwidth, consider the SY58022U 1:4 fanout buffer with 400mV LVPECL output swing, or the SY58020U 1:4 CML fanout buffer. The SY58021U is part of Micrel's high-speed, Precision Edge® product line.

All support documentation can be found on Micrel's web site at [www.micrel.com](http://www.micrel.com).

## TYPICAL PERFORMANCE



## PACKAGE/ORDERING INFORMATION



16-Pin MLF™ (MLF-16)

Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58021UMI	MLF-16	Industrial	021U	Sn-Pb
SY58021UMITR <sup>(2)</sup>	MLF-16	Industrial	021U	Sn-Pb
SY58021UMG	MLF-16	Industrial	021U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58021UMGTR <sup>(2)</sup>	MLF-16	Industrial	021U with Pb-Free bar-line indicator	Pb-Free NiPdAu

## Notes:

1. Contact factory for die availability. Dice are guaranteed at  $T_A = 25^\circ\text{C}$ , DC electricals only.
2. Tape and Reel.

## PIN DESCRIPTION

Pin Number	Pin Name	Pin Function
1, 4	IN, /IN	Differential Input: This input pair receives the signal to be buffered. Each pin of this pair internally terminates with 50Ω to the VT pin. Note that this input will default to an indeterminate state if left open. See "Input Interface Applications" section.
2	VT	Input Termination Center-Tap: Each input terminates to this pin. The $V_T$ pin provides a center-tap for each input (IN, /IN) to the termination network for maximum interface flexibility. See "Input Interface Applications" section.
3	VREF-AC	Reference Output Voltage: This output biases to $V_{CC} - 1.2\text{V}$ . It is used when AC-coupling to differential inputs. Connect $V_{REF-AC}$ directly to the VT pin. Bypass with 0.01μF low ESR capacitor to $V_{CC}$ . See "Input Interface Applications" section.
8, 13	VCC	Positive Power Supply: Bypass with 0.1μF//0.01μF low ESR capacitors as close to the $V_{CC}$ pins as possible.
5, 16	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the ground pin.
14, 15 11, 12 9, 10 6, 7	/Q0, Q0, /Q1, Q1, /Q2, Q2, /Q3, Q3	LVPECL Differential Output Pairs: Differential buffered output copy of the input signal. The output swing is typically 800mV. Proper termination is 50Ω to $V_{CC} - 2\text{V}$ at the receiving end. Unused output pairs may be left floating with no impact on jitter or skew. See "LVPECL Output Termination" section.

**Absolute Maximum Ratings<sup>(1)</sup>**

Power Supply Voltage ( $V_{CC}$ )	–0.5V to +4.0V
Input Voltage ( $V_{IN}$ )	–0.5V to $V_{CC}$
LVPECL Output Current ( $I_{OUT}$ )	
Continuous	50mA
Surge	100mA
Source or sink current on VT pin	
$V_T$ Current	±100mA
Source or sink current on IN, /IN	
Input Current	±50mA
Source or sink current on $V_{REF-AC}$ <sup>(4)</sup>	
$V_{REF}$ Current	±1.5mA
Soldering, (20 seconds)	260°C
Storage Temperature Range ( $T_S$ )	–65°C to +150°C

**Operating Ratings<sup>(2)</sup>**

Power Supply Voltage ( $V_{CC}$ )	+2.375V to +3.60V
Operating Temperature Range ( $T_A$ )	–40°C to +85°C
Package Thermal Resistance	
MLF™ ( $\theta_{JA}$ )	
Still-Air	60°C/W
500 lpm	54°C/W
MLF™ ( $\psi_{JB}$ )	
Junction-to-Board Resistance <sup>(3)</sup>	33°C/W

**INPUT DC ELECTRICAL CHARACTERISTICS<sup>(5)</sup>** $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ 

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{CC}$	Power Supply Voltage	$V_{CC} = 2.5\text{V}$ $V_{CC} = 3.3\text{V}$	2.375 3.0	2.5 3.3	2.625 3.60	V
$I_{CC}$	Power Supply Current	No load, $V_{CC} = \text{max.}$		125	160	mA
$V_{IH}$	Input HIGH Voltage	IN, /IN, <b>Note 6</b>	$V_{CC}-1.6$		$V_{CC}$	V
$V_{IL}$	Input LOW Voltage	IN, /IN	0		$V_{IH}-0.1$	V
$V_{IN}$	Input Voltage Swing	IN, /IN; see Figure 1a.	0.1		1.7	V
$V_{DIFF\_IN}$	Differential Input Voltage Swing	IN, /IN; see Figure 1b.	0.2		3.4	V
$R_{IN}$	IN-to- $V_T$ Resistance		40	50	60	$\Omega$
$V_{T\ IN}$	IN-to- $V_T$ Voltage				1.28	V
$V_{REF-AC}$	Output Reference Voltage		$V_{CC}-1.30$	$V_{CC}-1.2$	$V_{CC}-1.1$	V

**LVPECL OUTPUT DC ELECTRICAL CHARACTERISTICS<sup>(5)</sup>** $V_{CC} = 3.3\text{V} \pm 10\%$  or  $2.5 \pm 5\%$ ;  $R_L = 50\Omega$  to  $V_{CC}-2\text{V}$ ;  $T_A = -40^\circ\text{C}$  to  $85^\circ\text{C}$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$V_{OH}$	Output HIGH Voltage		$V_{CC}-1.145$		$V_{CC}-0.895$	V
$V_{OL}$	Output LOW Voltage		$V_{CC}-1.945$		$V_{CC}-1.695$	V
$V_{OUT}$	Output Voltage Differential Swing	see Figure 1a.	550	780	1050	mV
$V_{DIFF\_OUT}$	Differential Output Voltage Swing	see Figure 1b.	1100	1560	2100	mV

**Notes:**

1. Permanent device damage may occur if ratings in the “Absolute Maximum Ratings” section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device’s most negative potential on the PCB.
4. Due to the limited drive capability, use for input of the same package only.
5. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
6.  $V_{IH}$  (min.) not lower than 1.2V.

**AC ELECTRICAL CHARACTERISTICS**

$V_{CC} = 2.5V \pm 5\%$  or  $3.3V \pm 10\%$ ;  $R_L = 50\Omega$  to  $V_{CC}-2V$ ;  $T_A = -40^\circ C$  to  $+85^\circ C$ , unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
$f_{MAX}$	Maximum Operating Frequency	$V_{OUT} \geq 400mV$ Clock	4			GHz
		NRZ Data		5		Gbps
$t_{pd}$	Propagation Delay		150	220	300	ps
$t_{CHAN}$	Channel-to-Channel Skew	<b>Note 7</b>		4	15	ps
$t_{SKEW}$	Part-to-Part Skew	<b>Note 8</b>			50	ps
$t_{JITTER}$	Clock Cycle-to-Cycle Jitter	<b>Note 9</b>			1	ps <sub>RMS</sub>
	Total Jitter	<b>Note 10</b>			10	ps <sub>PP</sub>
	Data Random Jitter	<b>Note 11</b> 2.5Gbps – 3.2Gbps			1	ps <sub>RMS</sub>
	Deterministic Jitter	<b>Note 12</b> 2.5Gbps – 3.2Gbps			10	ps <sub>PP</sub>
$t_r, t_f$	Output Rise/Fall Time 20% to 80%	At full swing.	35	75	110	ps

**Notes:**

7. Skew is measured between outputs of the same bank under identical transitions.
8. Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
9. Cycle-to-cycle jitter definition: the variation of periods between adjacent cycles,  $T_n - T_{n-1}$  where T is the time between rising edges of the output signal.
10. Total jitter definition: with an ideal clock input of frequency  $\leq f_{MAX}$ , no more than one output edge in  $10^{12}$  output edges will deviate by more than the specified peak-to-peak jitter value.
11. Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps/3.2Gbps.
12. Deterministic jitter is measured at 2.5Gbps/3.2Gbps with both K28.5 and  $2^{23}-1$  PRBS pattern

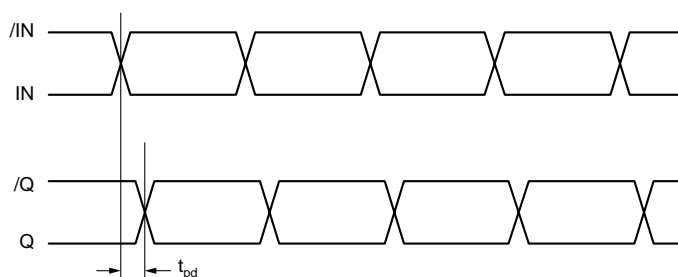
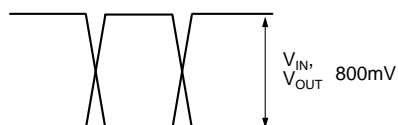
**TIMING DIAGRAM****SINGLE-ENDED AND DIFFERENTIAL SWINGS**

Figure 1a. Single-Ended Voltage Swing

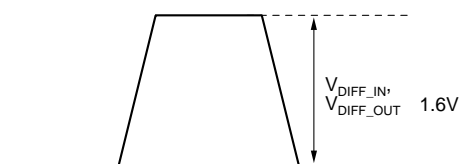
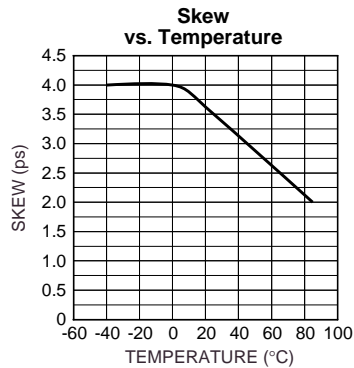
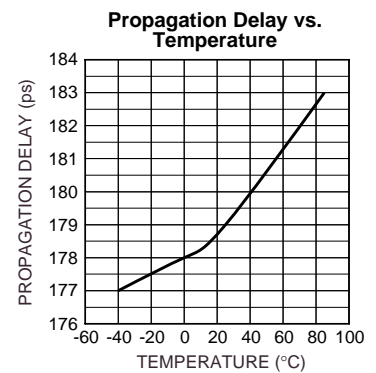
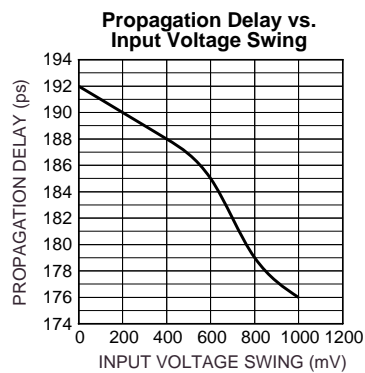
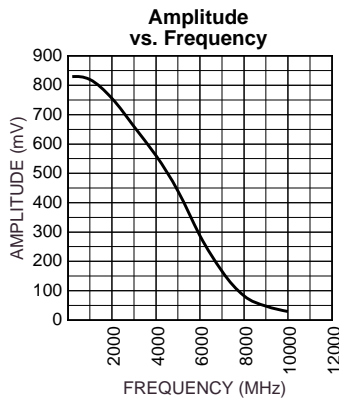


Figure 1b. Differential Voltage Swing

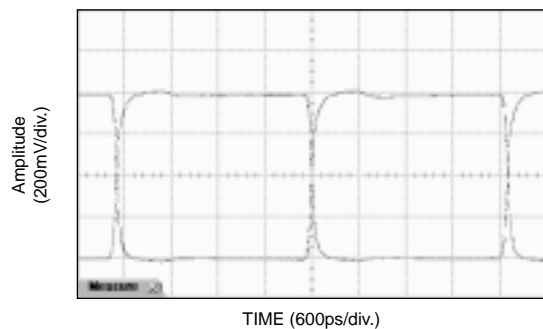
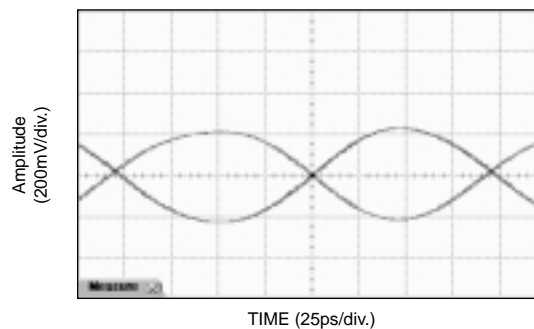
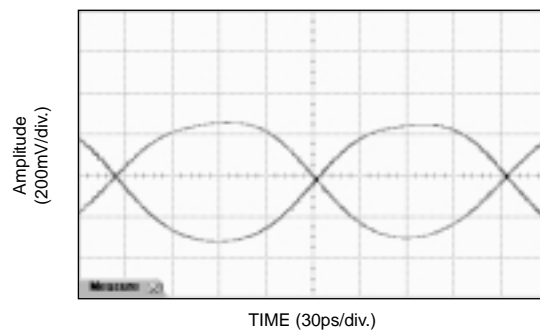
**TYPICAL OPERATING CHARACTERISTICS**

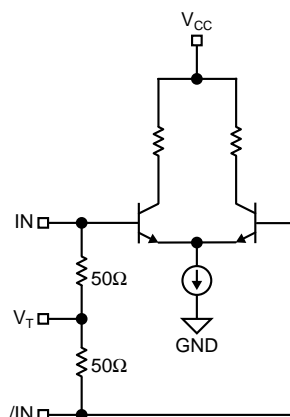
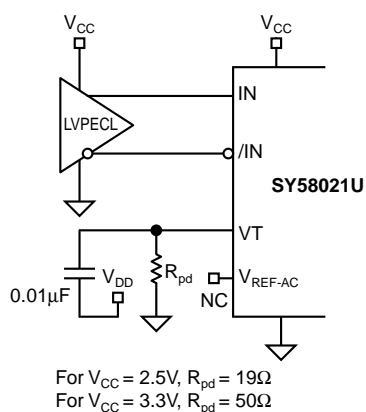
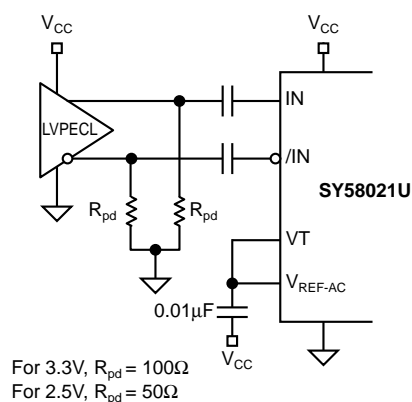
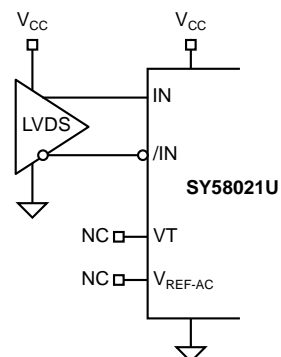
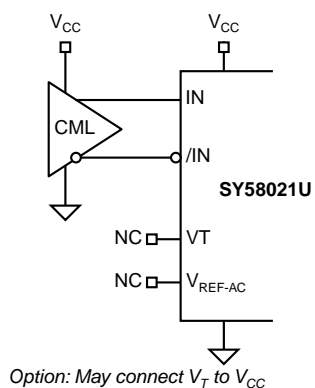
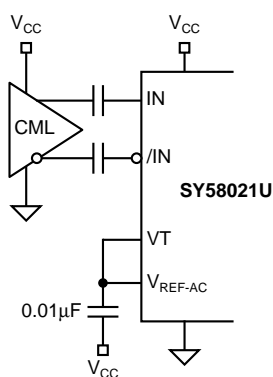
$V_{CC} = 2.5V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.



**FUNCTIONAL CHARACTERISTICS**

$V_{CC} = 2.5V$ ,  $GND = 0$ ,  $V_{IN} = 100mV$ ,  $T_A = 25^\circ C$ , unless otherwise stated.

**200MHz Output****5GHz Output****4GHz Output**

**INPUT STAGE****Figure 2. Simplified Differential Input Buffer****INPUT INTERFACE APPLICATIONS****Figure 3a. LVPECL  
Input Interface****Figure 3b. AC-Coupled LVPECL  
Input Interface****Figure 3c. LVDS  
Input Interface****Figure 3d. DC-Coupled CML  
Input Interface****Figure 3e. AC-Coupled CML  
Input Interface**

## LVPECL OUTPUT

LVPECL output have very low output impedance (open emitter), and small signal swing which results in low EMI. LVPECL is ideal for driving 50Ω and 100Ω controlled

impedance transmission lines. There are several techniques in terminating the LVPECL output, as shown in Figures 4 through 6.

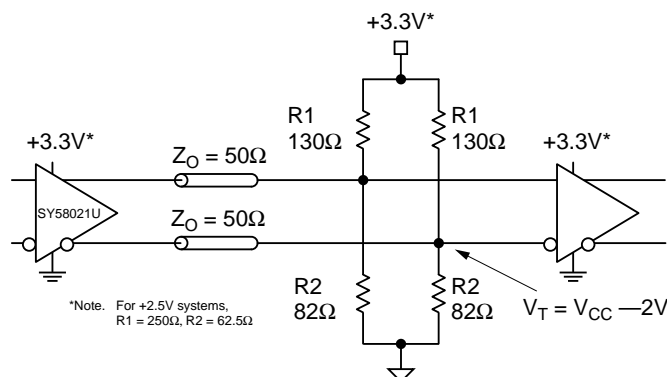


Figure 4. Parallel Termination-Thevenin Equivalent

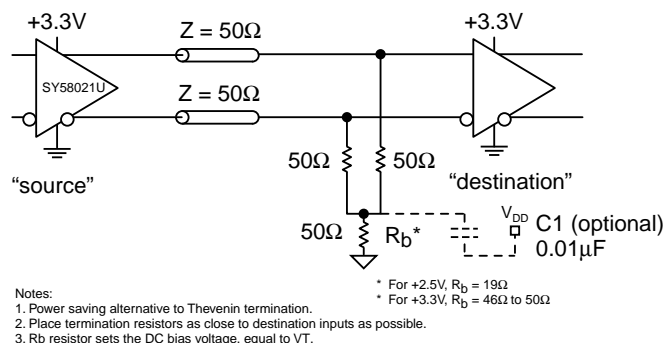


Figure 5. Parallel Termination (3-Resistor)

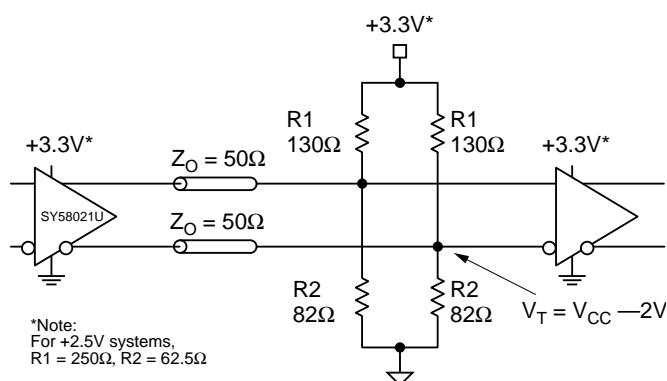
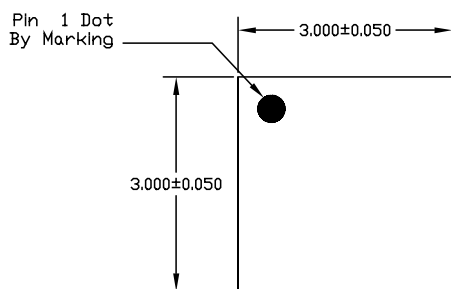


Figure 6. Terminating Unused I/O

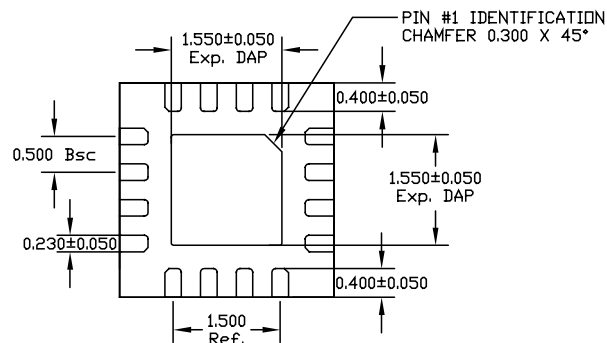
## RELATED MICREL PRODUCTS AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58020U	6GHz, 1:4 CML Fanout Buffer/Translator Internal I/O Terminations	<a href="http://www.micrel.com/product-info/products/sy58020u.shtml">http://www.micrel.com/product-info/products/sy58020u.shtml</a>
SY58021U	4GHz, 1:4 LVPECL Fanout Buffer/Translator with Internal Termination	<a href="http://www.micrel.com/product-info/products/sy58021u.shtml">http://www.micrel.com/product-info/products/sy58021u.shtml</a>
SY58022U	5.5GHz, 1:4 Fanout Buffer/Translator w/400mV LVPECL Outputs and Internal Terminations	<a href="http://www.micrel.com/product-info/products/sy58022u.shtml">http://www.micrel.com/product-info/products/sy58022u.shtml</a>
	16-MLF™ Manufacturing Guidelines Exposed Pad Application Note	<a href="http://www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf">www.amkor.com/products/notes_papers/MLF_AppNote_0902.pdf</a>
M-0317	HBW Solutions	<a href="http://www.micrel.com/product-info/as/solutions.shtml">http://www.micrel.com/product-info/as/solutions.shtml</a>

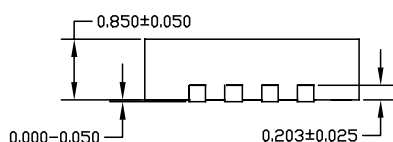


**16 LEAD *MicroLeadFrame*™ (MLF-16)**

TOP VIEW



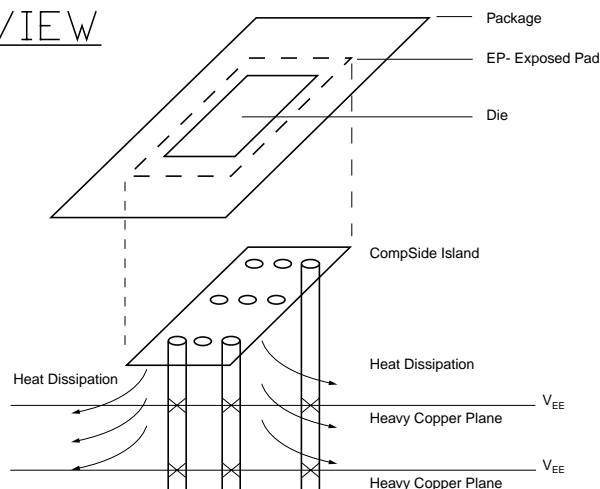
BOTTOM VIEW



SIDE VIEW

## NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 16-Pin MLF™ Package**  
**(Always solder, or equivalent, the exposed pad to the PCB)**

**Package Notes:**

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

**MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA**

TEL + 1 (408) 944-0800 FAX + 1 (408) 474-1000 WEB <http://www.micrel.com>

The information furnished by Micrel in this data sheet is believed to be accurate and reliable. However, no responsibility is assumed by Micrel for its use. Micrel reserves the right to change circuitry and specifications at any time without notification to the customer.

Micrel Products are not designed or authorized for use as components in life support appliances, devices or systems where malfunction of a product can reasonably be expected to result in personal injury. Life support devices or systems are devices or systems that (a) are intended for surgical implant into the body or (b) support or sustain life, and whose failure to perform can be reasonably expected to result in a significant injury to the user. A Purchaser's use or sale of Micrel Products for use in life support appliances, devices or systems is at Purchaser's own risk and Purchaser agrees to fully indemnify Micrel for any damages resulting from such use or sale.

© 2005 Micrel, Incorporated.