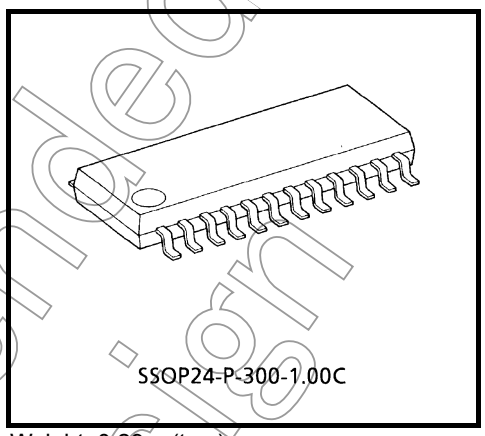
TOSHIBA Intelligent Power Device Silicon Monolithic Power MOS Integrated Circuit

TPD7203F

Power MOSFET Gate Driver for 3-Phase DC Motor

The TPD7203F is a power MOSFET gate driver for 3-phase full-bridge circuits that use a charge pump system. The inclusion of a charge pump circuit for high-side drive inside the IC makes it easy to configure a 3-phase full-bridge circuit.

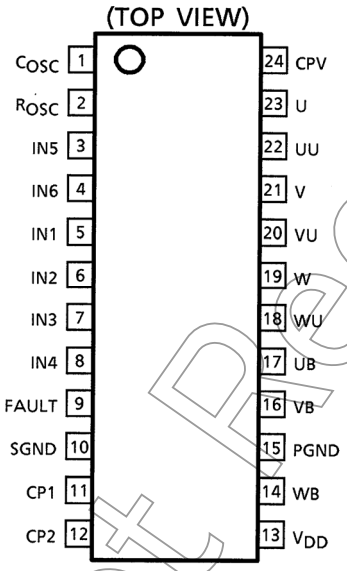


Weight: 0.29 g (typ.)

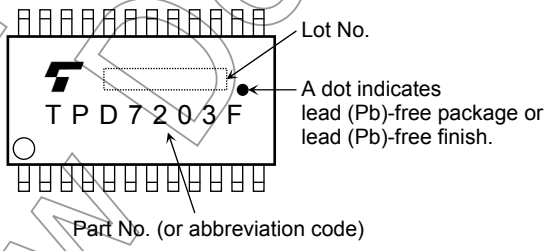
Features

- Power MOSFET gate driver for 3-phase DC motor
- Built-in power MOSFET protection and diagnosis function: low-voltage protection
- Built-in charge pump circuit
- Package: SSOP-24 (300 mil) with embossed-tape packing

Pin Assignment



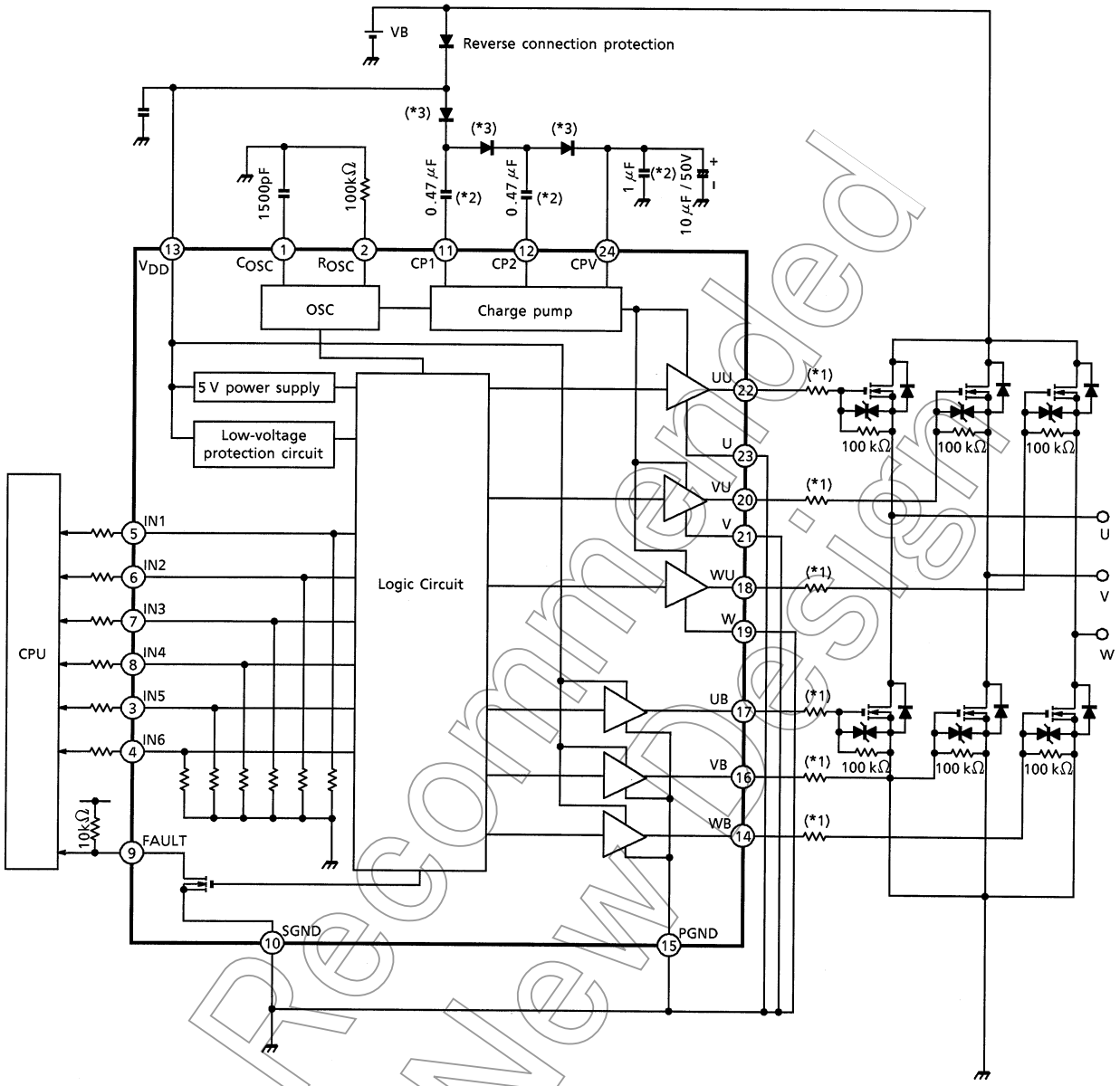
Marking



Due to its MOS structure, this product is sensitive to static electricity. Handle with care.

Not Recommended for New Design

Block Diagram / Application Circuit



*1: Optimum conditions depend on the switching loss, EMI, etc., of the external MOSFET.

*2: This is a laminated ceramic capacitor.

*3: High-speed diode trr = 100 ns max (Recommended: CRH01)

Note: For details on selecting external parts, see "Method for selecting external parts" described later.

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Pin Description

Pin No.	Symbol	Pin Description
1	C_{OSC}	This pin sets the oscillation frequency for the charge pump drive. Connect a 1500 pF (recommended) capacitor.
2	R_{OSC}	This pin sets the oscillation frequency for the charge pump drive. Connect a 100 kΩ (recommended) resistor.
3	IN5	Input pin: it controls the power MOSFET connected to VB. **B**uilt-in pull-down resistor (100 kΩ typ.)
4	IN6	Input pin: it controls the power MOSFET connected to WB. **B**uilt-in pull-down resistor (100 kΩ typ.)
5	IN1	Input pin: it controls the power MOSFET connected to UU. **B**uilt-in pull-down resistor (100 kΩ typ.)
6	IN2	Input pin: it controls the power MOSFET connected to VU. **B**uilt-in pull-down resistor (100 kΩ typ.)
7	IN3	Input pin: it controls the power MOSFET connected to WU. **B**uilt-in pull-down resistor (100 kΩ typ.)
8	IN4	Input pin: it controls the power MOSFET connected to UB. **B**uilt-in pull-down resistor (100 kΩ typ.)
9	FAULT	Diagnosis output pin: when low-voltage 6 V (typ.) is detected, output "H". Circuit configuration is N-ch open drain.
10	SGND	Signal block GND pin
11	CP1	Capacitor pin for charge pump Connect a 0.47 μF (recommended) laminated ceramic capacitor.
12	CP2	Capacitor pin for charge pump Connect a 0.47 μF (recommended) laminated ceramic capacitor.
13	V_{DD}	Power supply pin: when low voltage (6 V typ.) is detected, all outputs are shut down.
14	WB	Drives the power MOSFET connected to the low side of the W phase.
15	PGND	Power block GND pin
16	VB	Drives the power MOSFET connected to the low side of the V phase.
17	UB	Drives the power MOSFET connected to the low side of the U phase.
18	WU	Drives the power MOSFET connected to the high side of the W phase.
19	W	W phase output pin
20	VU	Drives the power MOSFET connected to the high side of the V phase.
21	V	V phase output pin
22	UU	Drives the power MOSFET connected to the high side of the U phase.
23	U	U phase output pin
24	CPV	Final stage capacitor for the charge pump Connect 1 μF (recommended) laminated ceramic capacitor and 10 μF (recommended) aluminum electrolytic capacitor in parallel.

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Truth Table
(All outputs go to low for input in high-side/low-side arm shorting mode)

Mode No.	Input						Output						Remarks
	In1 (UU)	In2 (VU)	In3 (WU)	In4 (UB)	In5 (VB)	In6 (WB)	Out UU	Out VU	Out WU	Out UB	Out VB	Out WB	
01	L	L	L	L	L	L	L	L	L	L	L	L	
02	H	L	L	L	L	L	H	L	L	L	L	L	
03	L	H	L	L	L	L	L	H	L	L	L	L	
04	L	L	H	L	L	L	L	L	H	L	L	L	
05	L	L	L	H	L	L	L	L	L	H	L	L	
06	L	L	L	L	H	L	L	L	L	L	H	L	
07	L	L	L	L	L	H	L	L	L	L	L	H	
08	H	L	L	H	L	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
09	H	L	L	L	H	L	H	L	L	L	H	L	120° square wave conducting normal mode
10	H	L	L	L	L	H	H	L	L	L	L	H	120° square wave conducting normal mode
11	L	H	L	H	L	L	L	H	L	H	L	L	120° square wave conducting normal mode
12	L	H	L	L	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
13	L	H	L	L	L	H	L	H	L	L	L	H	120° square wave conducting normal mode
14	L	L	H	H	L	L	L	L	H	H	L	L	120° square wave conducting normal mode
15	L	L	H	L	H	L	L	L	H	L	H	L	120° square wave conducting normal mode
16	L	L	H	L	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
17	H	H	L	L	L	L	H	H	L	L	L	L	
18	L	H	H	L	L	L	L	H	H	L	L	L	
19	H	L	H	L	L	L	H	L	H	L	L	L	
20	L	L	L	H	H	L	L	L	L	H	H	L	
21	L	L	L	L	H	H	L	L	L	L	H	H	
22	L	L	L	H	L	H	L	L	L	H	L	H	
23	H	H	L	H	L	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
24	H	H	L	L	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
25	H	H	L	L	L	H	H	H	L	L	L	H	
26	L	H	H	H	L	L	L	H	H	H	L	L	
27	L	H	H	L	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
28	L	H	H	L	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
29	H	L	H	H	L	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
30	H	L	H	L	H	L	H	L	H	L	H	L	

*: High-side/low-side arm shorting mode is disabled by the internal logic. (FAULT is kept low.) When undervoltage (6 V typ.) is detected, all outputs are pulled low regardless of input signals. At this time, FAULT output goes high (open-drain, high-impedance).

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Mode No.	Input						Output						Remarks
	In1 (UU)	In2 (VU)	In3 (WU)	In4 (UB)	In5 (VB)	In6 (WB)	Out UU	Out VU	Out WU	Out UB	Out VB	Out WB	
31	H	L	H	L	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
32	H	L	L	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
33	H	L	L	L	H	H	H	L	L	L	H	H	
34	H	L	L	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
35	L	H	L	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
36	L	H	L	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
37	L	H	L	H	L	H	L	H	L	H	L	H	
38	L	L	H	H	H	L	L	L	H	H	H	L	
39	L	L	H	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
40	L	L	H	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
41	H	H	H	L	L	L	H	H	H	L	L	L	
42	L	L	L	H	H	H	L	L	L	H	H	H	
43	H	H	L	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
44	H	H	L	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
45	H	H	L	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
46	L	H	H	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
47	L	H	H	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
48	L	H	H	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
49	H	L	H	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
50	H	L	H	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
51	H	L	H	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
53	H	H	H	L	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
54	H	H	H	L	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
55	H	L	L	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
56	L	H	L	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
57	L	L	H	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
58	H	H	H	H	H	L	L	L	L	L	L	L	High-side/low-side arm shorting mode *
59	H	H	H	L	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
60	H	H	H	H	L	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
61	H	H	L	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
62	L	H	H	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
63	H	L	H	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *
64	H	H	H	H	H	H	L	L	L	L	L	L	High-side/low-side arm shorting mode *

*: High-side/low-side arm shorting mode is disabled by the internal logic. (FAULT is kept low.) When undervoltage (6 V typ.) is detected, all outputs are pulled low regardless of input signals. At this time, FAULT output goes high (open-drain, high-impedance).

Not Recommended for New Design

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit	Remarks
Power supply voltage	V_{DD}	− 0.5 ~ 30	V	
Output current	I_{SOURCE}	1	A	Pulse width ≤10μs
	I_{SINK}	1		
Input voltage	V_{IN}	− 0.5 ~ 7.0	V	
Fault pin voltage	V_{FAULT}	30	V	
U, V and pin negative voltage	U (−) V (−) W (−)	− 0.5	V	Negative voltage that can be applied to U, V and W pins (Reference to SGND pin)
PGND pin negative voltage	PGND(−)	− 0.5	V	Negative voltage that can be applied to PGND pin (reference to SGND pin)
Fault pin current	I_{FAULT}	5	mA	
Power dissipation	P_D	0.8	W	
		1.2 Note		
Operating temperature	T_{opr}	− 40 ~ 125	°C	
Storage temperature	T_{stg}	− 40 ~ 150	°C	

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings and the operating ranges.
Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/Derating Concept and Methods) and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Resistance

Characteristic	Symbol	Rating	Unit
Junction to ambient thermal resistance	$R_{th\ (j\text{-}a)}$	156.3	°C / W
		104.2 Note	

Note: When the device is mounted on a 60 mm × 60 mm × 1.6 mm glass epoxy PCB

Not Recommended for New Design

Electrical Characteristics
(Unless otherwise specified, T_a = –40 ~ 125°C)

Characteristic		Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit	Remarks
Operating supply voltage		V_{DD}	—	—	7	13.5	18	V	
Supply current		$I_{DD(1)}$	1	V_{DD} = 13.5 V	—	—	10	mA	Oscillation circuit stops
		$I_{DD(2)}$	2	V_{DD} = 13.5 V, V_{IN1} ~ V_{IN6} = 0 V	—	—	100		When oscillation circuit is operating f = 20 kHz, mean current
Input voltage		V_{IH}	2	V_{DD} = 7 ~ 18 V, I_O = 0 A	3.5	—	—	V	IN1- IN6 high-level input voltage
		V_{IL}			—	—	1.5		IIN1-IN6 low-level input voltage
Input current		I_{IH}	2	V_{DD} = 7 ~ 18 V, V_{IN} = 5 V, I_O = 0 A	—	—	1	mA	IN1-IN6 input current
		I_{IL}		V_{DD} = 7 ~ 18 V, V_{IN} = 0 V, I_O = 0 A	– 10	—	10	μA	
Output voltage	High side	V_{OH}	2	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0 A	V_{CPV} – 2	—	V_{CPV}	V	V_{CPV} denotes CPV pin voltage. (reference to SGND pin)
		V_{OL}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0 A	—	—	0.1		UU pin voltage (reference to U pin) VU pin voltage (reference to V pin) WU pin voltage (reference to W pin)
	Low side	V_{OH}		V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0 A	11.5	—	13.5		UB pin voltage (reference to PGND pin) VB pin voltage (reference to PGND pin) WB pin voltage (reference to PGND pin)
		V_{OL}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0 A	—	—	0.1		
Charge pump voltage		V_{CPV}	2	V_{DD} = 13.5 V	30	—	35	V	CPV pin voltage (reference to SGND pin)
Active clamp voltage (low side)		V_{CLAMP}	—	V_{IN} = 5 V, I_O = 10 mA	—	18	—	V	UB, VB and WB pins clamp voltage (reference to PGND pin)
Output ON resistance		R_{SOURCE}	2	V_{DD} = 13.5 V, V_{IN} = 5 V, I_O = 0.5 A	—	7	10	Ω	UU, VU, WU, UB, VB and WB output resistance pulse width≤10 μs
		R_{SINK}		V_{DD} = 13.5 V, V_{IN} = 0 V, I_O = 0.5 A	—	4.5	10		

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Characteristic		Symbol	Test Circuit	Condition	Min	Typ.	Max	Unit	Remarks
Low-voltage protection	Detection	$V_{SD\ (L)}$	3	—	5.5	6	6.5	V	Low voltage detection voltage and hysteresis (V_{DD} voltage detected)
	Hysteresis	$\Delta V_{SD\ (L)}$			—	0.5	—		
Switching time	Turn-on delay time	$t_{d\ (ON)}$	4	V_{DD} = 7 to 18 V, C_{OUT} = 0.047μF, R_G = 47Ω	—	—	4	μs	UU, VU, WU, UB, VB and WB switching time
	Turn-on time	t_{ON}			—	—	6		
	Turn-off delay time	$t_{d\ (OFF)}$			—	—	4		
	Turn-off time	t_{OFF}			—	—	6		
Oscillating frequency		f_{osc}	2	V_{DD} = 7 ~ 18 V, R_{OSC} = 100 kΩ, C_{OSC} = 1500 pF	—	20	—	kHz	f_{OSC} calculation formula $f_{OSC} \approx 3 / \{C_{OSC} (R_{OSC} + 2\ k)\}$ (Hz)
Fault pin voltage		V_{FAULT}	2	I_{FAULT} = 1 mA	—	—	0.8	V	FAULT pin low-level voltage (open - drain)
Fault delay time		t_{ON}	3	R_{FAULT} = 5.1 kΩ, V_{FAULT} = 5 V (External power supply)	—	1	—	μs	Time from low voltage / overvoltage detection or restoration to FAULT output inversion
		t_{OFF}			—	1	—		

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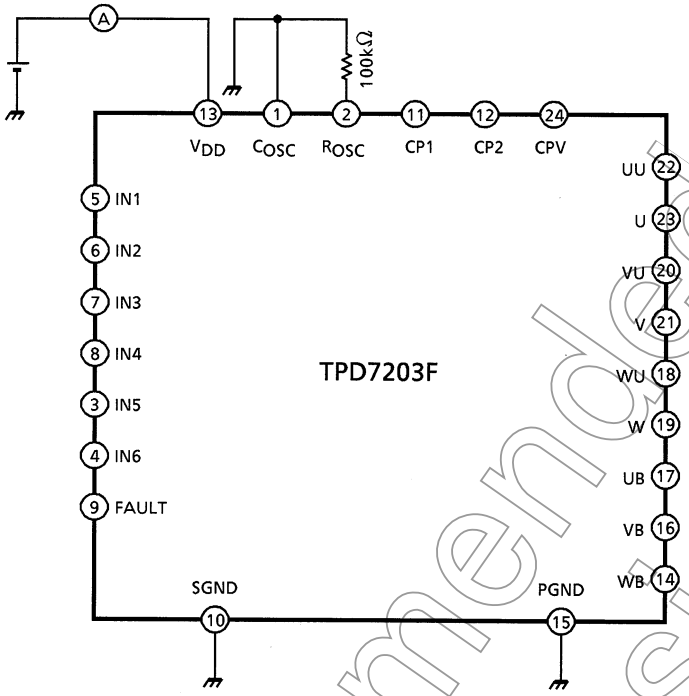
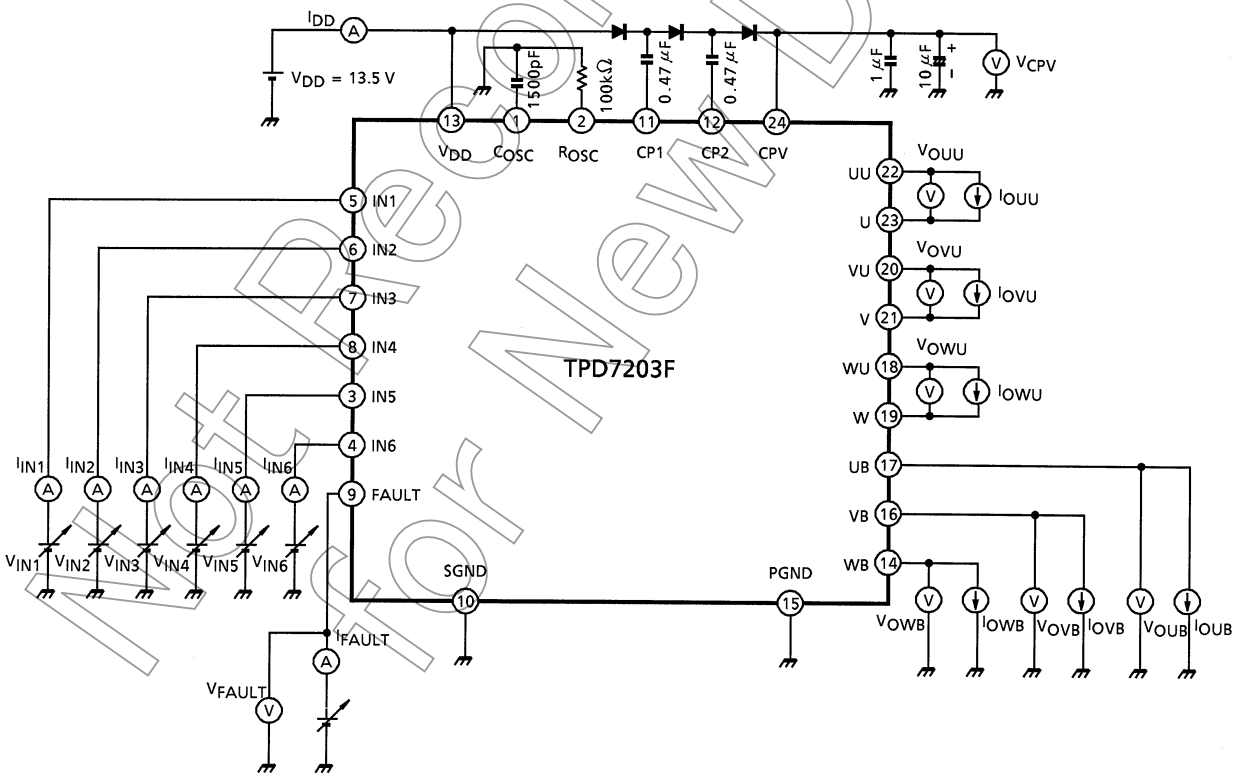
Test Circuit 1 $I_{DD(1)}$



Testing Circuit 2 $I_{DD(2)}$, V_{IH}, V_{IL}, I_{IH}, I_{IL}, V_{OH}, V_{OL}, V_{CPV}, V_{FAULT}



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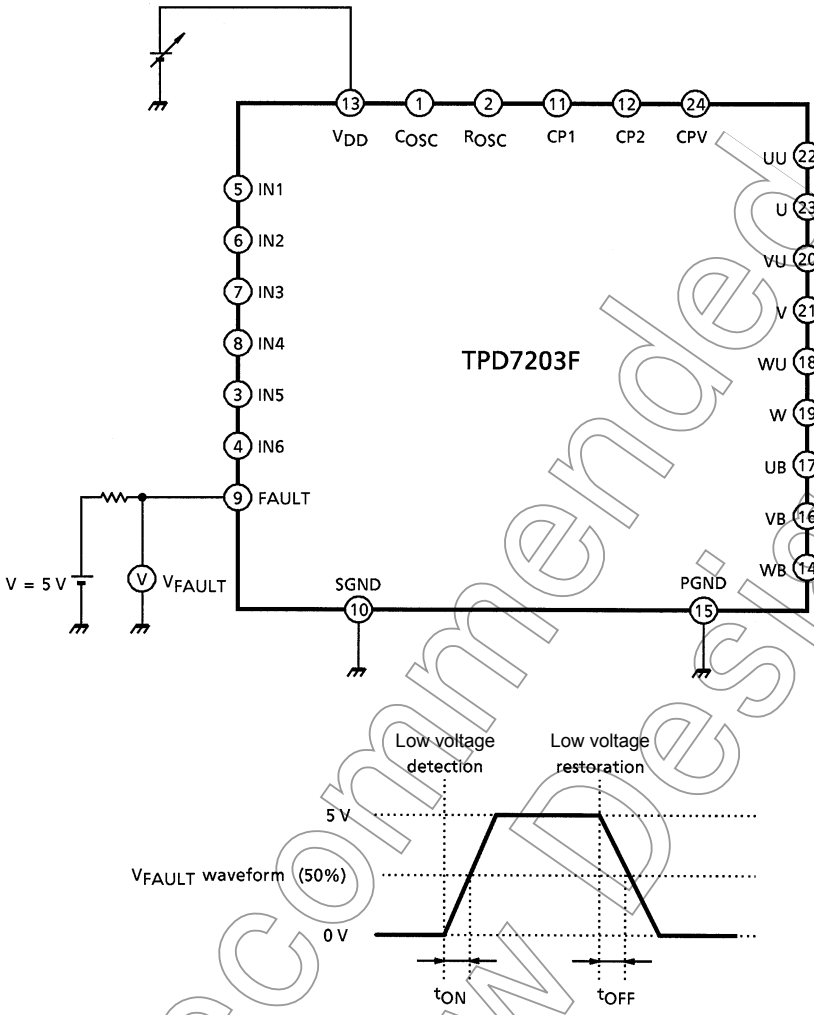
Testing Circuit 3 $V_{SD(L)}$, ΔV_{SD}, $V_{SD(H)}$, $\Delta V_{SD(H)}$, **FAULT delay time** t_{ON}, t_{OFF}



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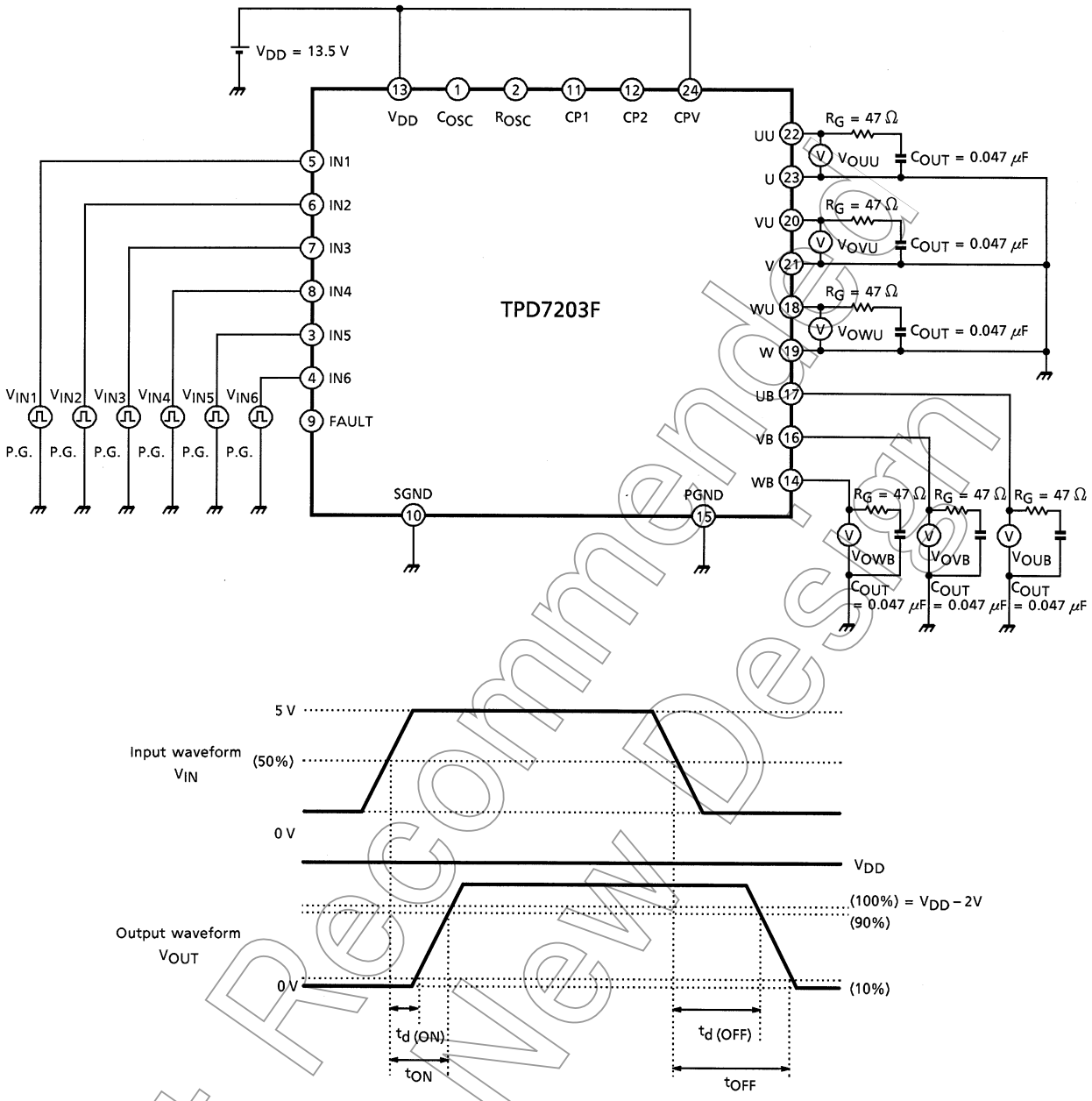
Testing Circuit 4 $t_{d(ON)}$, t_{ON}, $t_{d(OFF)}$, t_{OFF}



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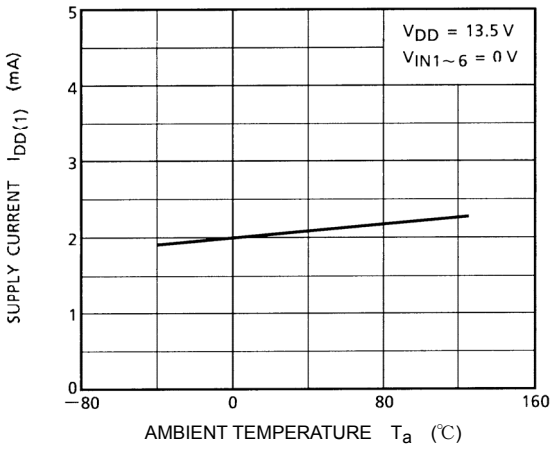
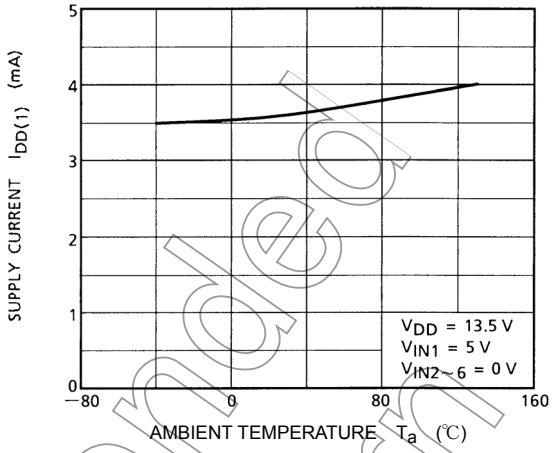
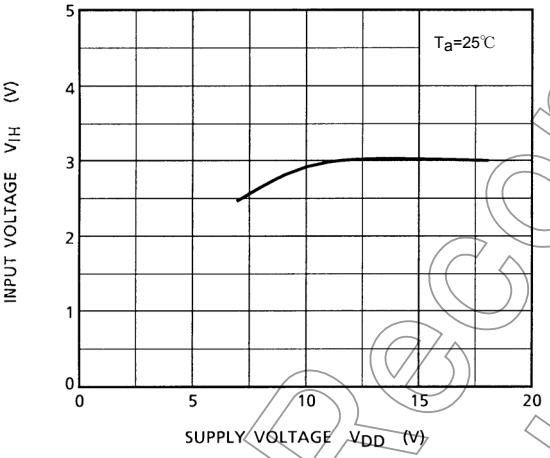
$I_{DD(1)}$ – T_a



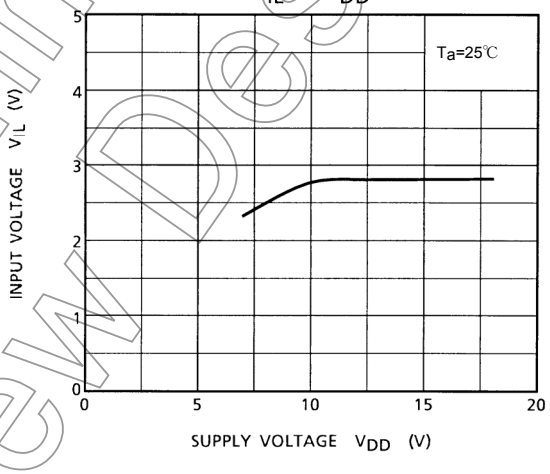
$I_{DD(1)}$ – T_a



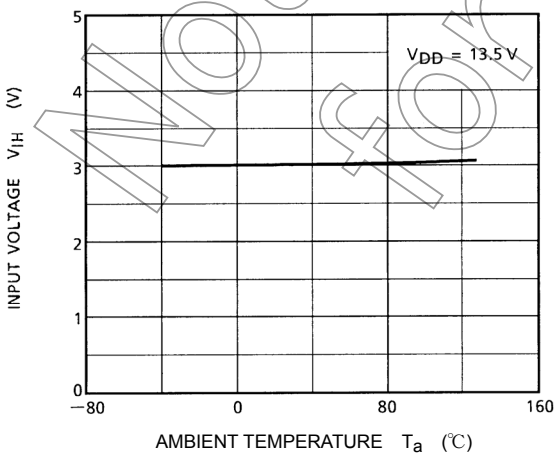
V_{IH} – V_{DD}



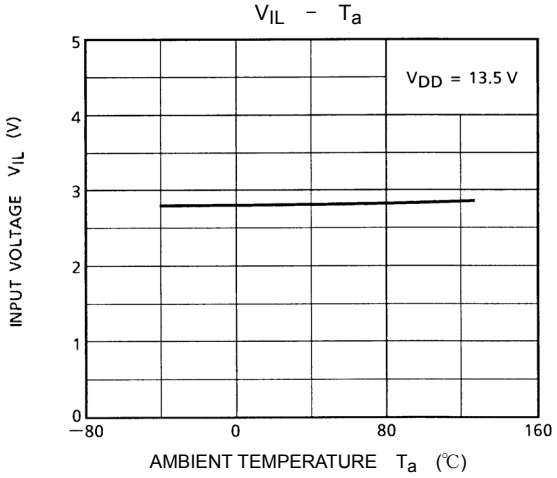
V_{IL} – V_{DD}



V_{IH} – T_a

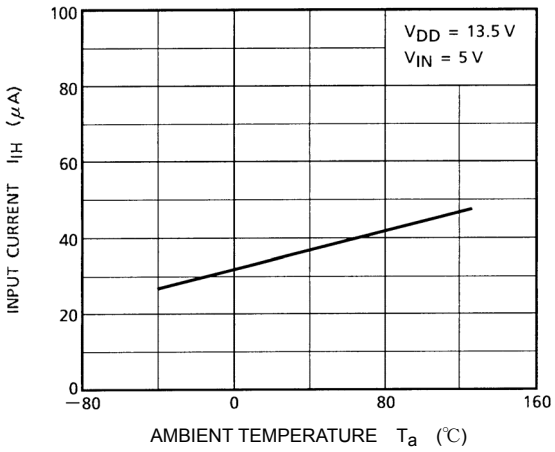


V_{IL} – T_a

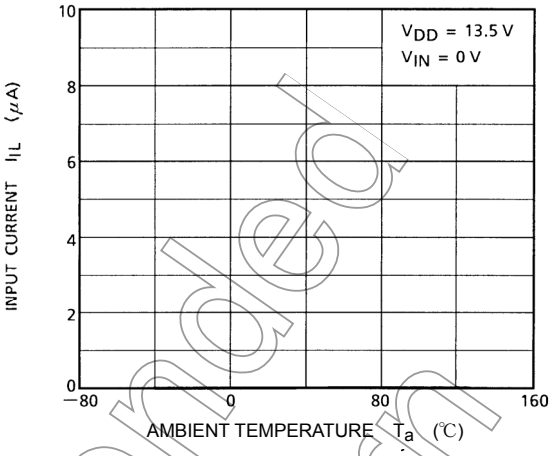


Not Recommended for New Design

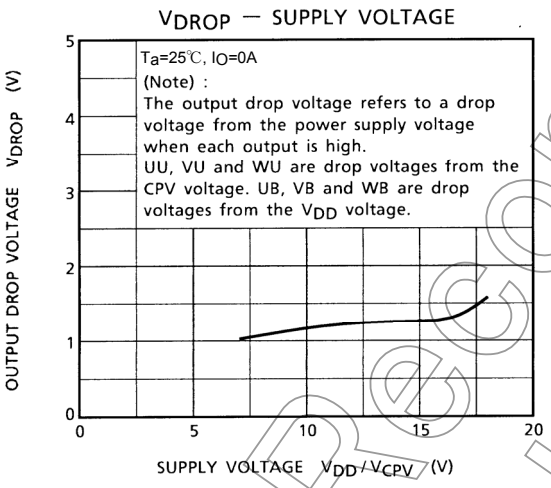
I_{IH} – T_a



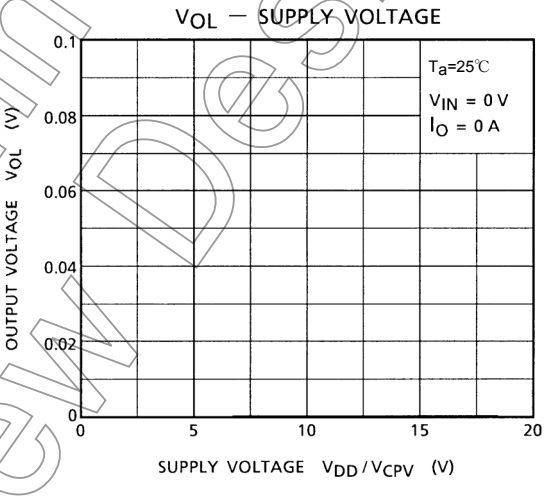
I_{IL} – T_a



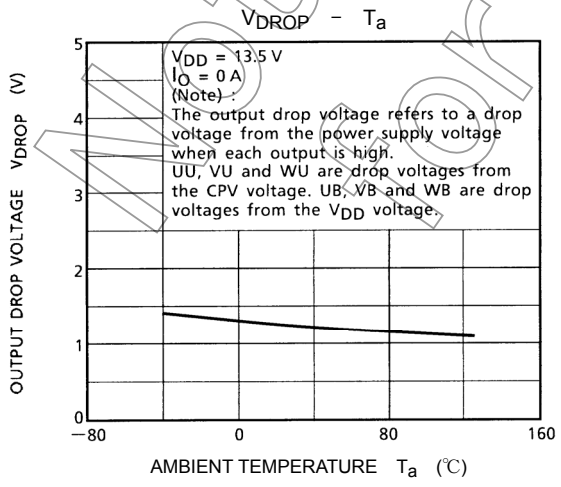
V_{DROP} — SUPPLY VOLTAGE



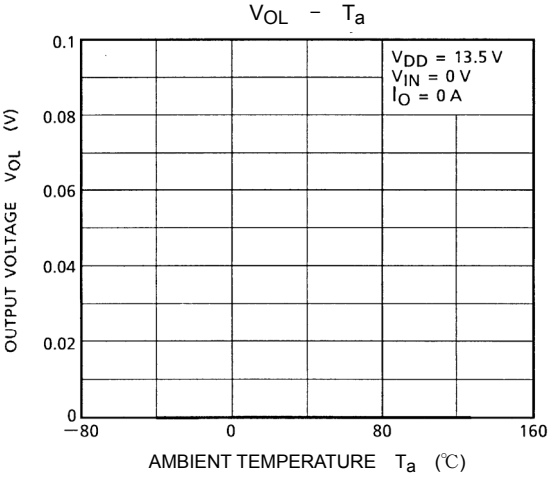
V_{OL} — SUPPLY VOLTAGE



V_{DROP} – T_a



V_{OL} – T_a



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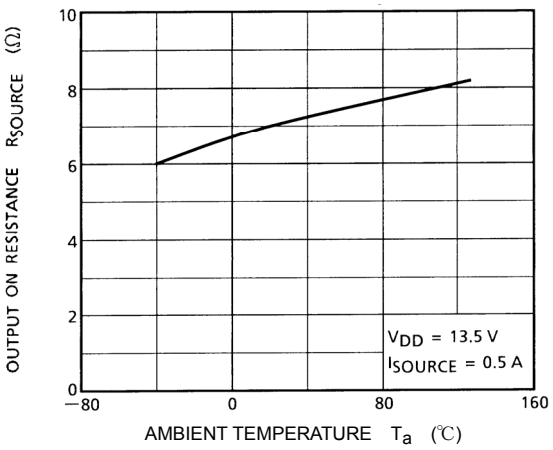
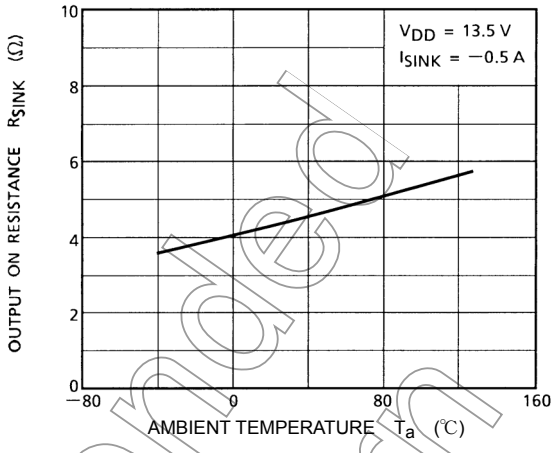
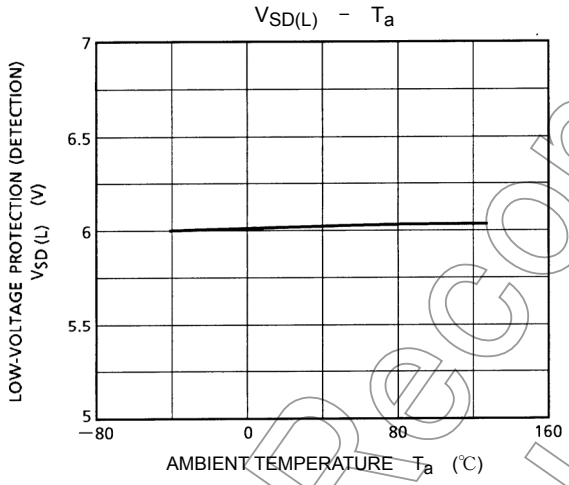
R_{SOURCE} – T_a



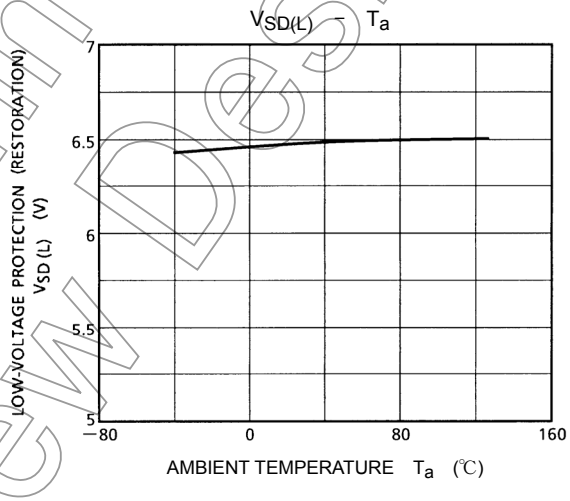
R_{SINK} – T_a



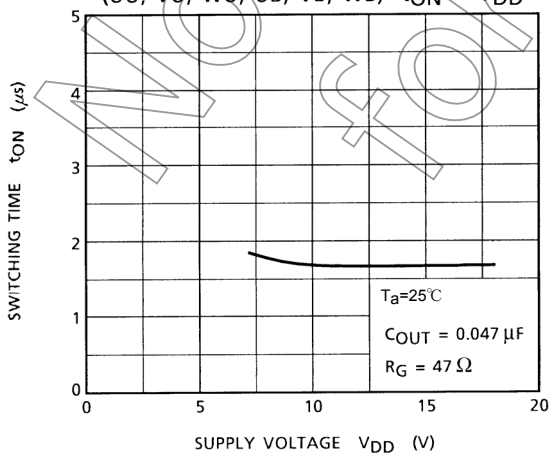
$V_{SD(L)}$ – T_a



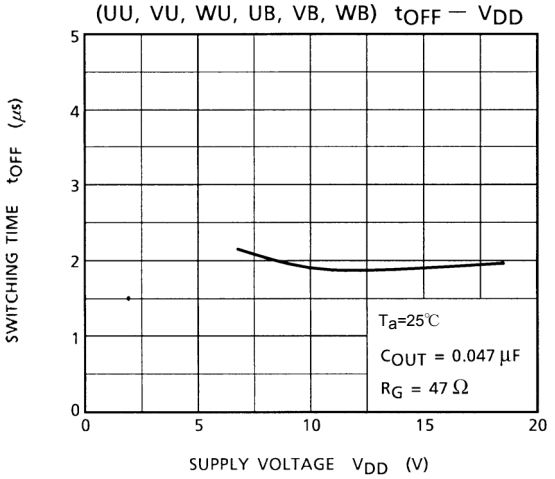
$V_{SD(L)}$ – T_a



SWITCHING TIME
(UU, VU, WU, UB, VB, WB) t_{ON} – V_{DD}



SWITCHING TIME
(UU, VU, WU, UB, VB, WB) t_{OFF} – V_{DD}



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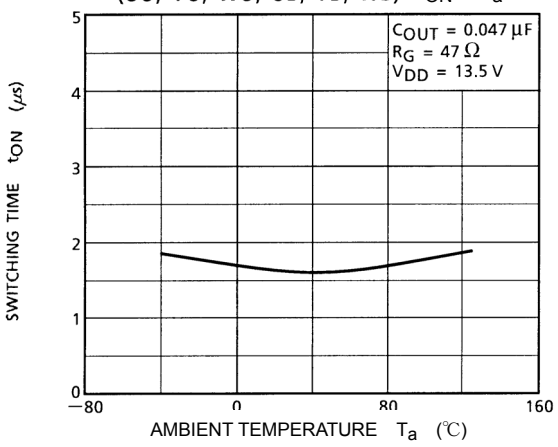
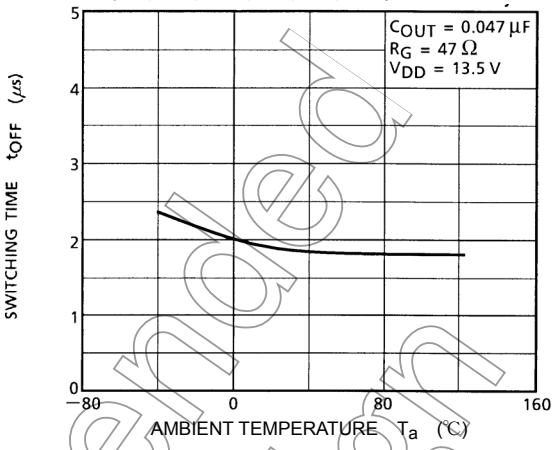
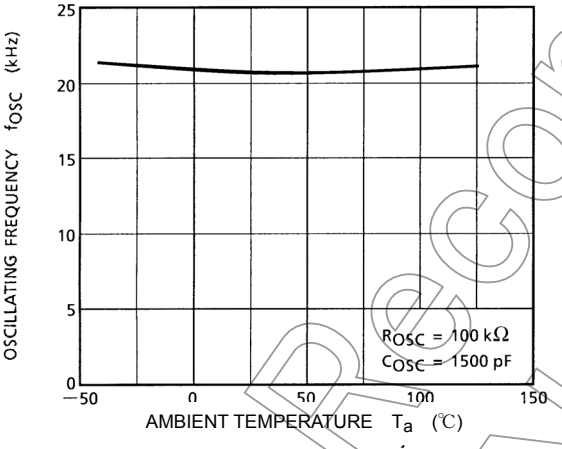
SWITCHING TIME
(UU, VU, WU, UB, VB, WB) t_{ON} – Ta



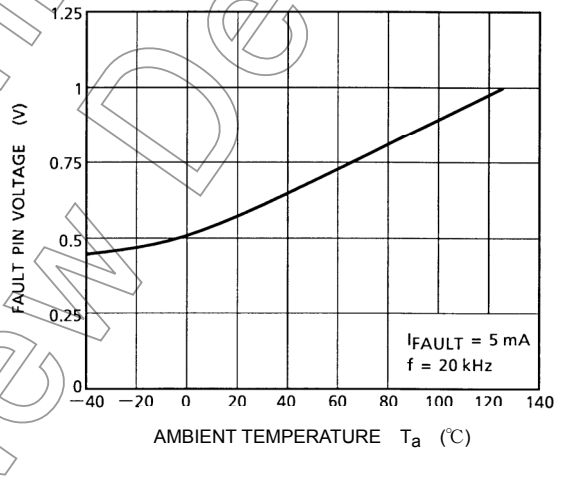
SWITCHING TIME
(UU, VU, WU, UB, VB, WB) t_{OFF} – Ta



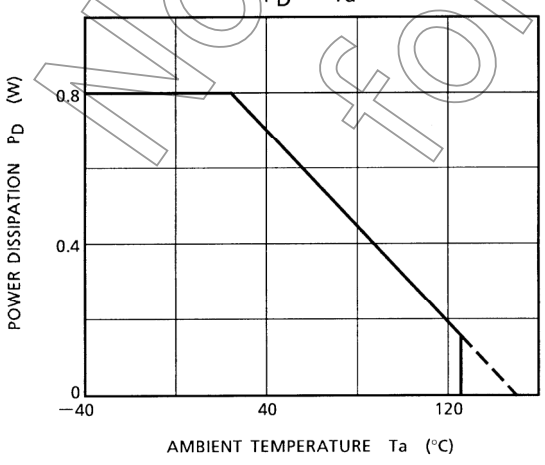
f_{OSC} – Ta



V_{FAULT} – Ta



P_D – Ta



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Method for Selecting External Parts

Pin No.	Pin Name	Type	Recommended Value / Recommended Product	Description
1	C_{OSC}	Capacitor	1500 pF (ceramic)	Sets the charge pump oscillation frequency.
2	R_{OSC}	Resistor	100 kΩ	Sets the charge pump oscillation frequency.
11 12	CP1 CP2	Capacitor	0.47 μF (laminated ceramic)	Capacitor for the charge pump: The greater this capacitance, the larger the charging current to the capacitor and the greater the loss in the IC.
24	CPV	Capacitor	1 μF (laminated ceramic) and 10 μF (aluminum electrolytic) connected in parallel	The greater this capacitance, the larger the current supply capacity of the charge pump (CPV pin) but the greater the loss in the IC. Take care not to exceed the allowable loss.
11 12 24	CP1 CP2 CPV	High-speed iode	t_{rr} = 100 ns (max) CRH01 (t_{rr} = 35 ns max) recommended	Diode for the charge pump. An electric charge equal to the diode's Q_{rr} component goes out of the capacitor's charged electricity. Therefore, use a high-speed diode. Diode for the charge pump : An electric charge equal to the Q_{rr} component of the diode goes out of the electrical charge of the capacitor. Therefore use a high-speed diode.
22 20 18 17 16 14	UU VU WU UB VB WB	Resistor	—	Gate resistor for external power MOSFET. Choose the optimum value by considering the switching loss and EMI of the power MOSFET.

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Usage Precautions

Note 1: Feeding the charge pump voltage to external devices

Current can be taken out of the final stage (CPV pin) of the charge pump and fed to external devices without causing any problem. In this case, because the charge pump voltage drops, increase the capacitance of the capacitor connected to the CPV pin. However, this will cause the charging current to the capacitor and, hence, loss in the IC to increase. Therefore be careful not to exceed the allowable loss.

Note 2: Heat sink design

Because this IC contains a charge pump function, loss in it affects external capacitor capacitance and diode characteristics. It is recommended that the junction temperature, T_j, be judged from the on-voltage of the FAULT pin (open-drain). When V_{DD} is within the range of operating power supply voltages, the FAULT pin outputs a low. For details about on-voltage characteristics, see T_j-V_{FAULT} characteristic curves.

Note 3: Dead time setting

For arm-shorting input logic, all outputs (UU, VU, WU, UB, VB and WB) are pulled low. When operating in forward or reverse mode, take into account the IC output switching time and the switching time (including temperature characteristic) of the external power MOSFET when setting the dead time. The dead time required for only the IC, not including the external power MOSFET, is 4μs (within all operating power supply voltages and all operating temperatures).

Note 4: Shorting between outputs, short-circuit of outputs and V_{DD} pin or short-circuit of outputs and GND pin may cause the IC to break down. Therefore, pay careful attention to the design of output lines and V_{DD} and GND lines.

Note 5: Precautions on dry packing

After unpacking dry or moisture-proof packing, make sure the device is mounted in place within 48 hours at a temperature and humidity of 30°C and 60% RH or less. Because the device is emboss-taped and cannot be processed by baking, always be sure to use it within the said allowable time after unpacking. Standard tape packing quantity: 2000 devices / reel (EL1).

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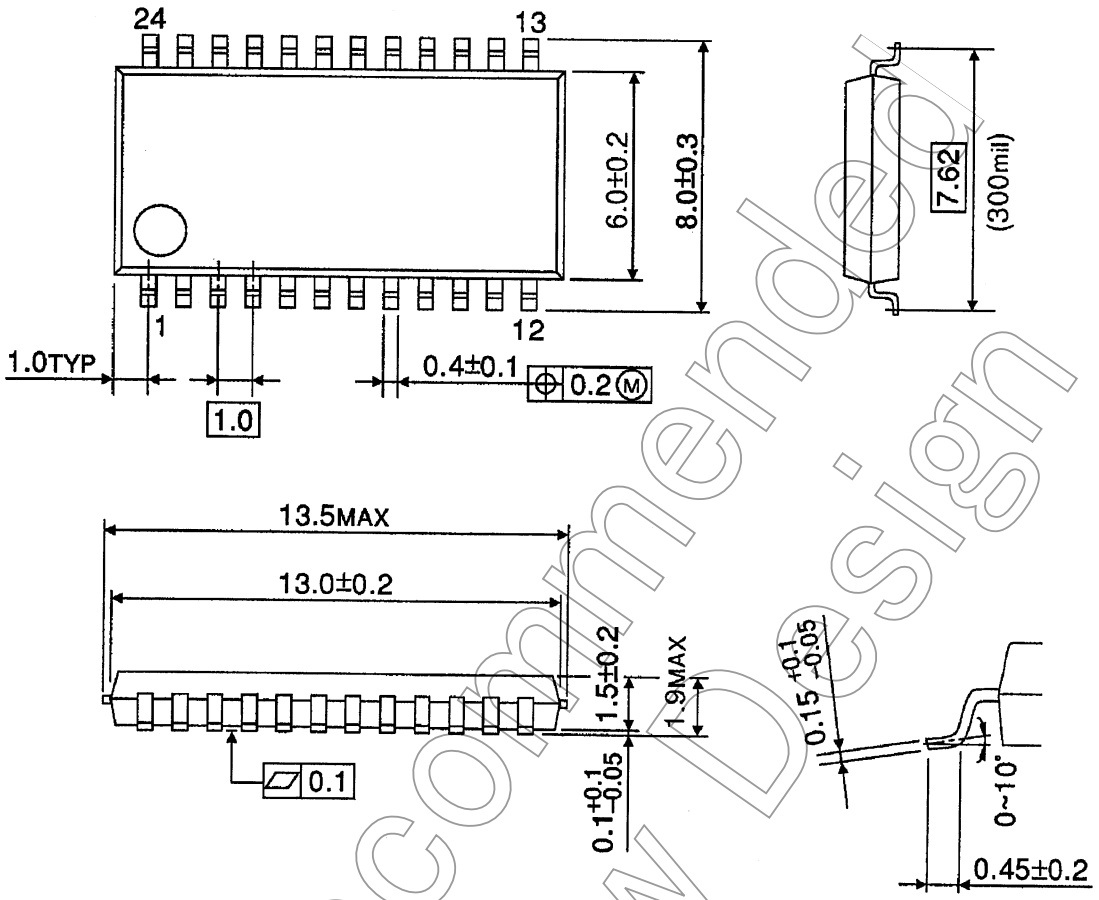
Package Dimensions

Unit: mm



Weight: 0.29 g (typ.)

Not Recommended for New Design

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20070701-EN

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