

FDMA1024NZ

Dual N-Channel PowerTrench® MOSFET

20 V, 5.0 A, 54 mΩ

Features

- Max $r_{DS(on)}$ = 54 mΩ at $V_{GS} = 4.5$ V, $I_D = 5.0$ A
- Max $r_{DS(on)}$ = 66 mΩ at $V_{GS} = 2.5$ V, $I_D = 4.2$ A
- Max $r_{DS(on)}$ = 82 mΩ at $V_{GS} = 1.8$ V, $I_D = 2.3$ A
- Max $r_{DS(on)}$ = 114 mΩ at $V_{GS} = 1.5$ V, $I_D = 2.0$ A
- HBM ESD protection level = 1.6 kV (Note 3)
- Low profile - 0.8 mm maximum - in the new package MicroFET 2x2 mm
- RoHS Compliant
- Free from halogenated compounds and antimony oxides



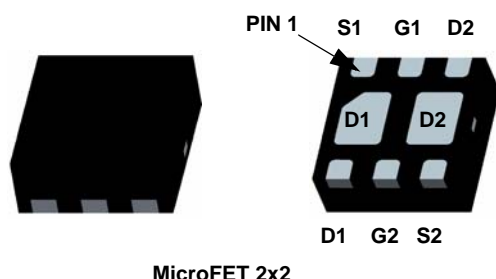
General Description

This device is designed specifically as a single package solution for dual switching requirements in cellular handset and other ultra-portable applications. It features two independent N-Channel MOSFETs with low on-state resistance for minimum conduction losses.

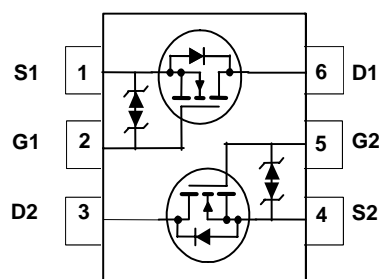
The MicroFET 2X2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Applications

- Baseband Switch
- Loadswitch
- DC-DC Conversion



MicroFET 2x2



MOSFET Maximum Ratings $T_A = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Ratings	Units
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	±8	V
I_D	Drain Current -Continuous (Note 1a)	5.0	A
	-Pulsed	6.0	
P_D	Power Dissipation (Note 1a)	1.4	W
	Power Dissipation (Note 1b)	0.7	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Thermal Characteristics

$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	86 (Single Operation)	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	173 (Single Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1c)	69 (Dual Operation)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1d)	151 (Dual Operation)	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
024	FDMA1024NZ	MicroFET 2X2	7 "	8 mm	3000 units

Electrical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
--------	-----------	-----------------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		19		mV/ $^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 16\text{ V}$, $V_{GS} = 0\text{ V}$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 8\text{ V}$, $V_{DS} = 0\text{ V}$			± 10	μA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\text{ }\mu\text{A}$	0.4	0.7	1.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, referenced to $25\text{ }^{\circ}\text{C}$		-3		mV/ $^{\circ}\text{C}$
$r_{DS(on)}$	Static Drain to Source On-Resistance	$V_{GS} = 4.5\text{ V}$, $I_D = 5.0\text{ A}$		37	54	m Ω
		$V_{GS} = 2.5\text{ V}$, $I_D = 4.2\text{ A}$		43	66	
		$V_{GS} = 1.8\text{ V}$, $I_D = 2.3\text{ A}$		52	82	
		$V_{GS} = 1.5\text{ V}$, $I_D = 2.0\text{ A}$		67	114	
		$V_{GS} = 4.5\text{ V}$, $I_D = 5.0\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$		51	75	
g_{FS}	Forward Transconductance	$V_{DD} = 5\text{ V}$, $I_D = 5.0\text{ A}$		16		S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 10\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$		375	500	pF
C_{oss}	Output Capacitance			70	95	pF
C_{rss}	Reverse Transfer Capacitance			40	65	pF
R_G	Gate Resistance	$f = 1\text{ MHz}$		4.3		Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 10\text{ V}$, $I_D = 5.0\text{ A}$ $V_{GS} = 4.5\text{ V}$, $R_{GEN} = 6\text{ }\Omega$		5.3	11	ns
t_r	Rise Time			2.2	10	ns
$t_{d(off)}$	Turn-Off Delay Time			18	33	ns
t_f	Fall Time			2.3	10	ns
Q_g	Total Gate Charge	$V_{GS} = 4.5\text{ V}$, $V_{DD} = 10\text{ V}$, $I_D = 5.0\text{ A}$		5.2	7.3	nC
Q_{gs}	Gate to Source Gate Charge			0.6		nC
Q_{gd}	Gate to Drain "Miller" Charge			0.9		nC

Drain-Source Diode Characteristics

I_S	Maximum Continuous Source-Drain Diode Forward Current				1.1	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 1.1\text{ A}$ (Note 2)		0.7	1.2	V
t_{rr}	Reverse Recovery Time	$I_F = 5.0\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$		19	35	ns
Q_{rr}	Reverse Recovery Charge			5	10	nC

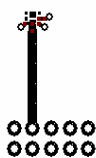
Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.

- (a) $R_{\theta JA} = 86^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For single operation.
- (b) $R_{\theta JA} = 173^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper. For single operation.
- (c) $R_{\theta JA} = 69^{\circ}\text{C/W}$ when mounted on a 1 in² pad of 2 oz copper, 1.5 " x 1.5 " x 0.062 " thick PCB. For dual operation.
- (d) $R_{\theta JA} = 151^{\circ}\text{C/W}$ when mounted on a minimum pad of 2 oz copper. For dual operation.



a) 86°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 173°C/W when mounted on a minimum pad of 2 oz copper.



c) 69°C/W when mounted on a 1 in² pad of 2 oz copper.



d) 151°C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test : Pulse Width < 300 us, Duty Cycle < 2.0 %

3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

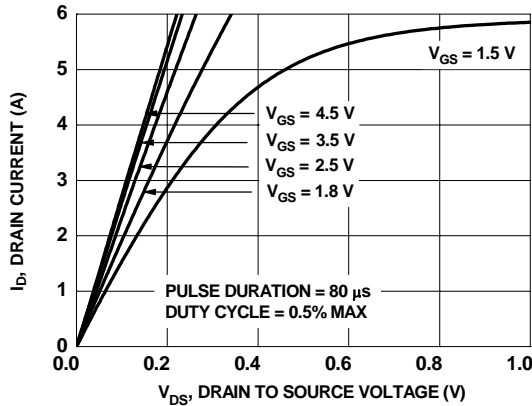


Figure 1. On-Region Characteristics

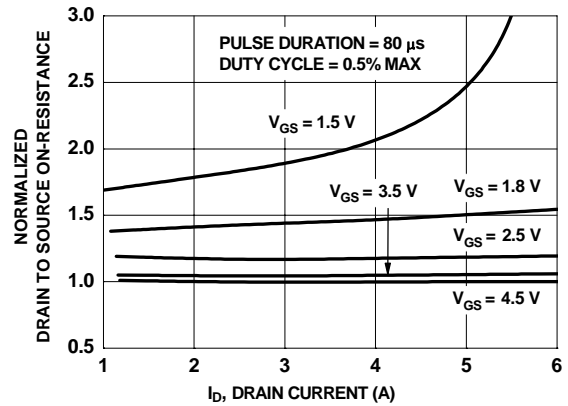


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

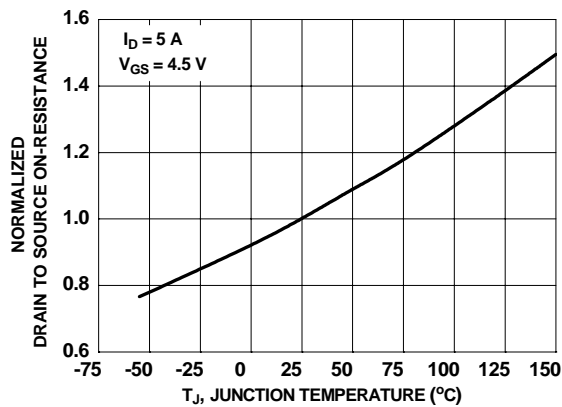


Figure 3. Normalized On-Resistance vs Junction Temperature

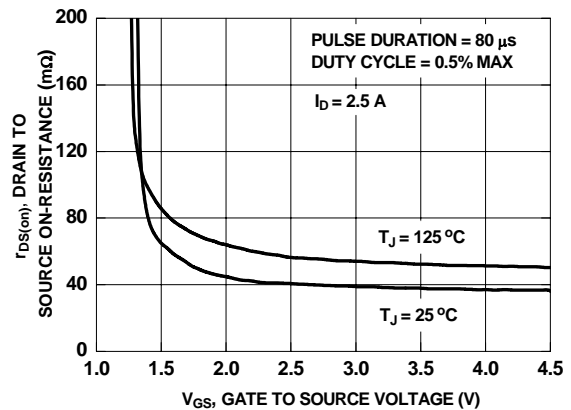


Figure 4. On-Resistance vs Gate to Source Voltage

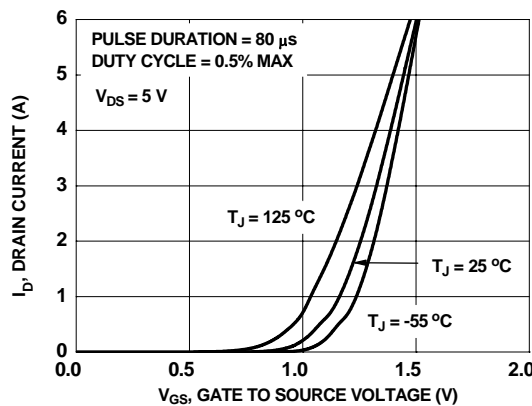


Figure 5. Transfer Characteristics

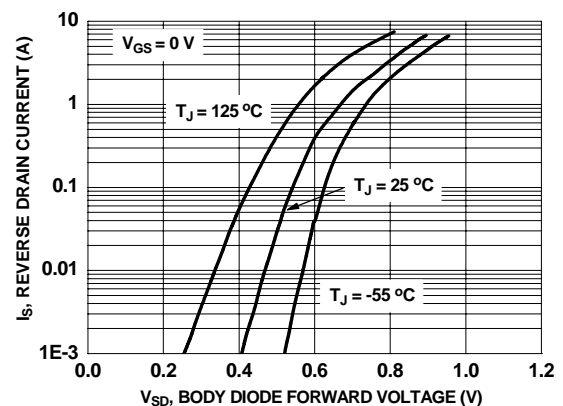


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

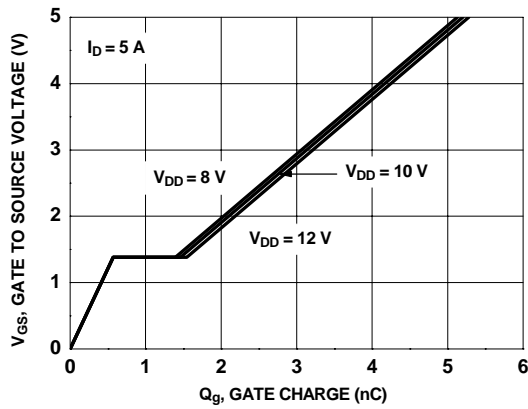


Figure 7. Gate Charge Characteristics

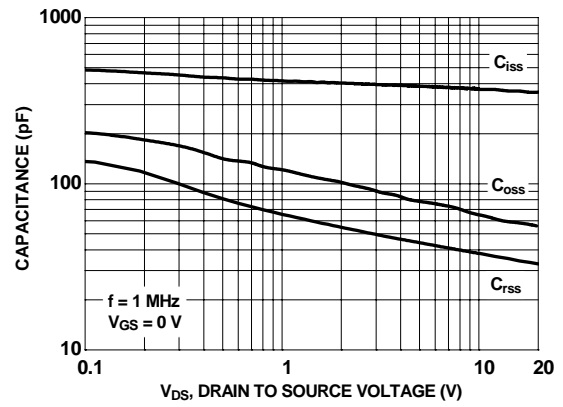


Figure 8. Capacitance vs Drain to Source Voltage

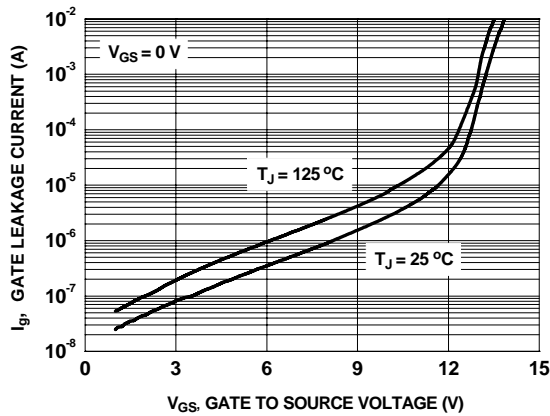


Figure 9. Gate Leakage Current vs Gate to Source Voltage

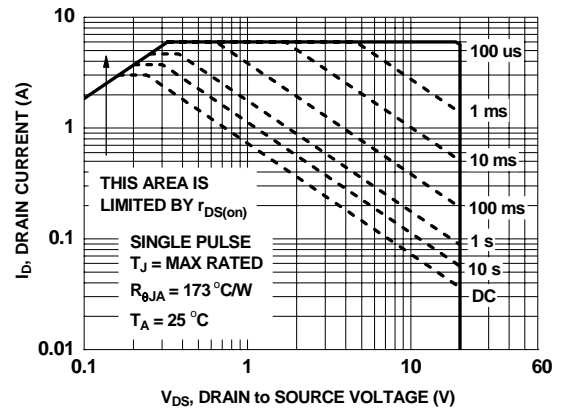


Figure 10. Forward Bias Safe Operating Area

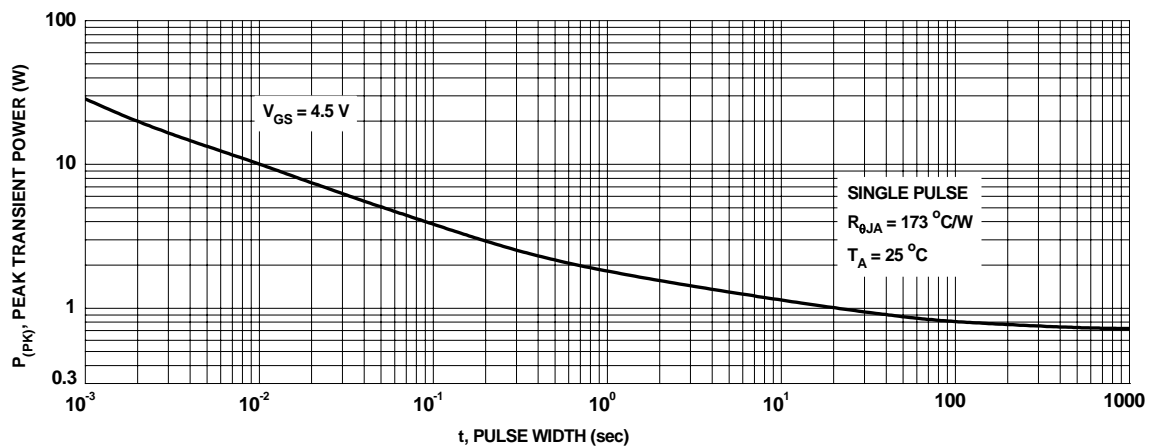
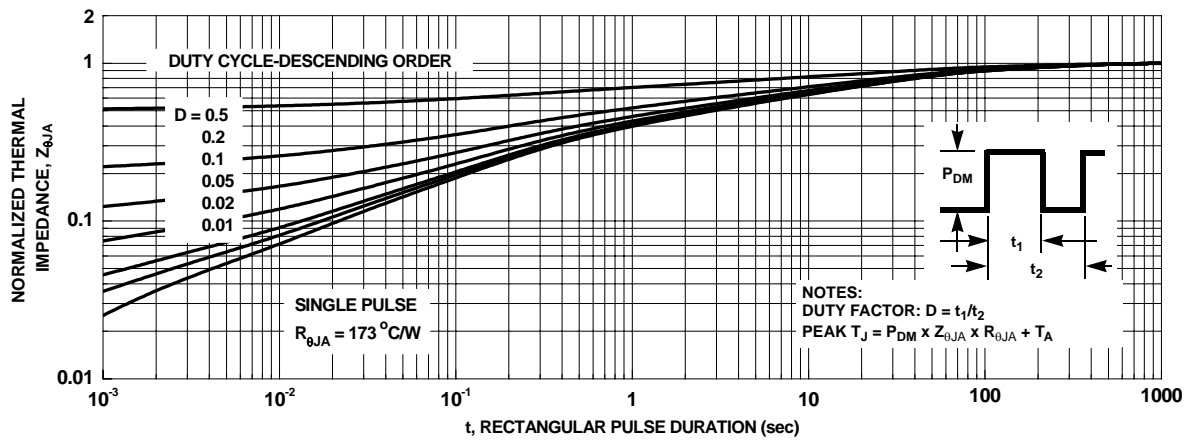
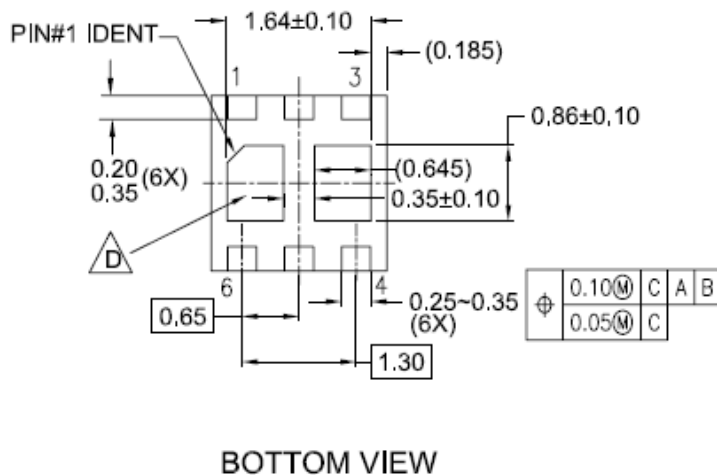
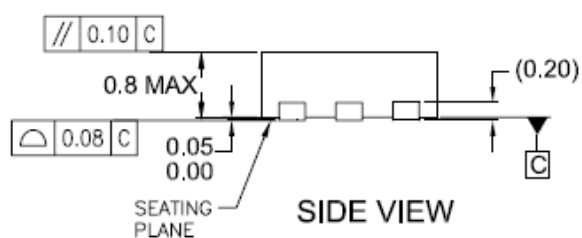
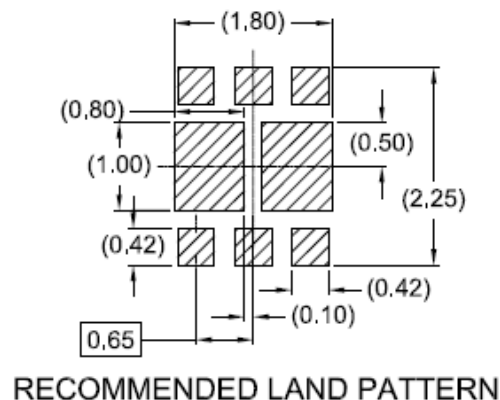
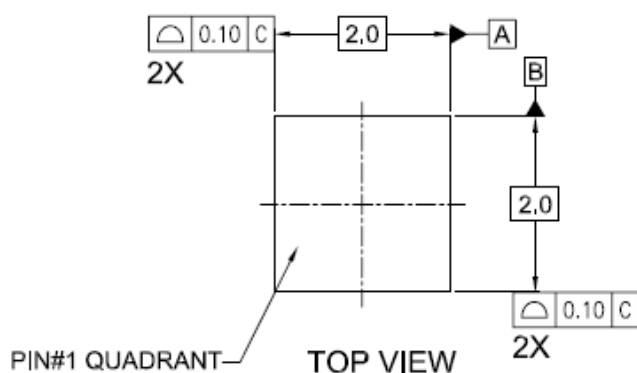


Figure 11. Single Pulse Maximum Power Dissipation

Typical Characteristics $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted



Dimensional Outline and Pad Layout









NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-229, VARIATION VCCC EXCEPT AS NOTED.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 1994
- D. NON-JEDEC DUAL DAP
- E. DRAWING FILE NAME : MLP06J rev3

TRADEMARKS

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

Auto-SPM™	F-PFST™	PowerTrench®	The Power Franchise®
Build it Now™	FRFET®	PowerXS™	the power®
CorePLUSTM	Global Power ResourceSM	Programmable Active Droop™	franchise
CorePOWER™	Green FPS™	QFET®	TinyBoost™
CROSSVOLT™	Green FPS™ e-Series™	QST™	TinyBuck™
CTL™	Gmax™	Quiet Series™	TinyLogic®
Current Transfer Logic™	GTO™	RapidConfigure™	TINYOPTO™
EcoSPARK®	IntelliMAX™	 TM	TinyPower™
EfficientMax™	ISOPLANAR™	Saving our world, 1mW /W /kW at a time™	TinyPWM™
EZSWITCH™ *	MegaBuck™	SmartMax™	TinyWire™
 TM*	MICROCOUPLER™	SMART START™	TriFault Detect™
 ®	MicroFET™	SPM®	TRUECURRENT™*
Fairchild®	MicroPak™	STEALTH™	µSerDes™
Fairchild Semiconductor®	MillerDrive™	SuperFET™	 SerDes™
FACT Quiet Series™	MotionMax™	SuperSOT™-3	UHC®
FACT®	Motion-SPM™	SuperSOT™-6	Ultra FRFET™
FAST®	OPTOLOGIC®	SuperSOT™-8	UniFET™
FastvCore™	OPTOPLANAR®	SupreMOS™	VCX™
FETBench™	 ®	SyncFET™	VisualMax™
FlashWriter® *	PDP SPM™	Sync-Lock™	XS™
FPS™	Power-SPM™	 SYSTEM GENERAL®*	

*Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

DISCLAIMER

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

LIFE SUPPORT POLICY

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

ANTI-COUNTERFEITING POLICY

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, www.Fairchildsemi.com, under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufactures of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed application, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address and warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

PRODUCT STATUS DEFINITIONS

Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. 140