



PI74FCT16646T PI74FCT162646T PI74FCT162H646T

Fast CMOS 16-Bit Registered Transceivers

Product Features

Common Features:

- PI74FCT16646T, PI74FCT162646T, and PI74FCT162H646 are high-speed, low power devices with high current drive
- $V_{CC} = 5V \pm 10\%$
- Hysteresis on all inputs
- Packages available:
 - 56-pin 240 mil wide plastic TSSOP (A)
 - 56-pin 173 mil wide plastic TVSOP (JEDEC TSSOP K)
 - 56-pin 300 mil wide plastic SSOP (V)

PI74FCT16646T Features:

- High output drive: $I_{OH} = -32mA$; $I_{OL} = 64mA$
- Power off disable outputs permit “live insertion”
- Typical V_{OLP} (Output Ground Bounce) $< 1.0V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162646T Features:

- Balanced output drivers: $\pm 24mA$
- Reduced system switching noise
- Typical V_{OLP} (Output Ground Bounce) $< 0.6V$ at $V_{CC} = 5V$, $T_A = 25^\circ C$

PI74FCT162H646T Features:

- Bus Hold retains last active bus state during Three-state
- Eliminates the need for external pull-up resistors

Product Description

Pericom Semiconductor's PI74FCT series of logic circuits are produced in the Company's advanced 0.6 micron CMOS technology, achieving industry leading speed grades.

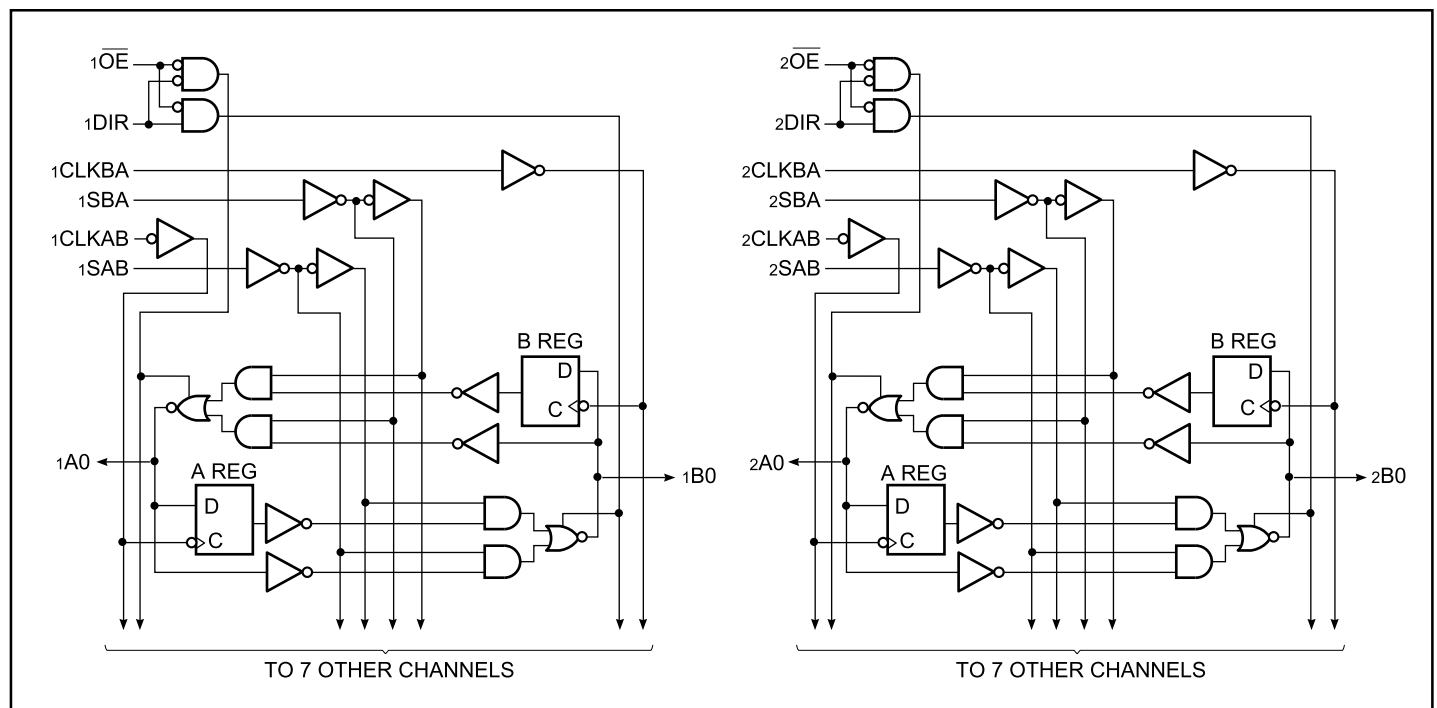
The PI74FCT16646T, PI74FCT162646T, and PI74FCT162H646 are 16-bit registered transceivers organized as two independent 8-bit bus transceivers designed with 3-state D-type flip-flops and control circuitry arranged for multiplexed transmission of data directly from the data bus or from the internal storage registers. Each 8-bit transceiver utilizes the enable control (xOE) and direction pins (xDIR) to control the transceiver functions. The Select (xSAB and xSBA) control pins are used to select either real-time or stored data transfer. The circuitry used for select control will eliminate the typical decoding glitch that occurs in a multiplexer during the transition between real-time and stored data. A low input level selects real-time data and a high selects stored data.

The PI74FCT16646T output buffers are designed with a Power-Off disable allowing “live insertion” of boards when used as backplane drivers.

The PI74FCT162646T has $\pm 24mA$ balanced output drivers. It is designed with current limiting resistors at its outputs to control the output edge rate resulting in lower ground bounce and undershoot. This eliminates the need for external terminating resistors for most interface applications.

The PI74FCT162H646T has “Bus Hold” which retains the input's last state whenever the input goes to high-impedance preventing “floating” inputs and eliminating the need for pull-up/down resistors.

Logic Block Diagram



Truth Table

Function/Operation	Inputs						DATA I/O ⁽²⁾	
	x $\overline{\text{OE}}$	xDIR	xCLKAB	xCLKBA	xSAB	xSBA	xAx	xBx
Isolation	H	X	H or L	H or L	X	X	Input	Input
Store A and B Data	H	X	↑	↑	X	X		
Real Time B Data to A Bus	L	L	X	X	X	L	Output	Input
Stored B Data to A Bus	L	L	X	H or L	X	H		
Real Time A Data to B Bus	L	H	X	X	L	X	Input	Output
Stored A Data to B Bus	L	H	H or L	X	H	X		

Notes:

1. The data output functions may be enabled or disabled by various signals at the x $\overline{\text{OE}}$ or xDIR inputs.

Data input functions are always enabled, i.e., data at the bus pins will be stored on every low-to-high transition on the clock inputs.

2. Select control = L: clocks can occur simultaneously.

Select control = H: clocks must be staggered to load both registers.

H = High Voltage Level; L = Low Voltage Level; X = Don't Care; ↑ = LOW-to-HIGH transition

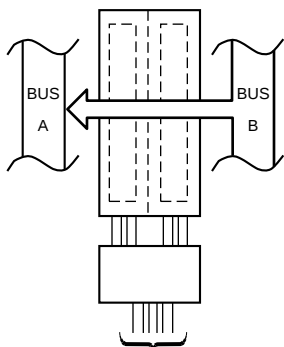
Product Pin Configuration

1DIR	1	56	1 $\overline{\text{OE}}$
1CLKAB	2	55	1CLKBA
1SAB	3	54	1SBA
GND	4	53	GND
1A0	5	52	1B0
1A1	6	51	1B1
VCC	7	50	VCC
1A2	8	49	1B2
1A3	9	48	1B3
1A4	10	47	1B4
GND	11	46	GND
1A5	12	45	1B5
1A6	13	44	1B6
1A7	14	43	1B7
2A0	15	42	2B0
2A1	16	41	2B1
2A2	17	40	2B2
GND	18	39	GND
2A3	19	38	2B3
2A4	20	37	2B4
2A5	21	36	2B5
VCC	22	35	VCC
2A6	23	34	2B6
2A7	24	33	2B7
GND	25	32	GND
2SAB	26	31	2SBA
2CLKAB	27	30	2CLKBA
2DIR	28	29	2 $\overline{\text{OE}}$

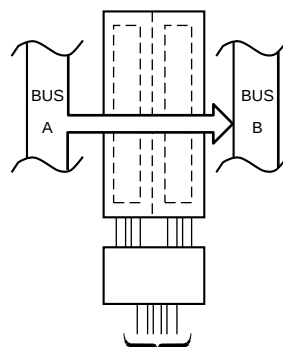
Product Pin Description

Pin Name	Description
xAx ⁽¹⁾	Data Register A Inputs Data Register B Outputs
xBx ⁽¹⁾	Data Register B Inputs Data Register A Outputs
xCLKAB, xCLKBA	Clock Pulse Inputs
SAB, SBA	Output Data Source Select Inputs
xDIR, x $\overline{\text{OE}}$	Output Enable Inputs
GND	Ground
VCC	Power

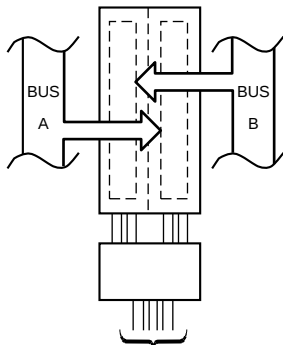
Note: 1. For the PI74FCT162H646T, these pins have "Bus Hold." All other pins are standard, outputs, or I/Os.

**REAL-TIME TRANSFER
BUS B TO A**


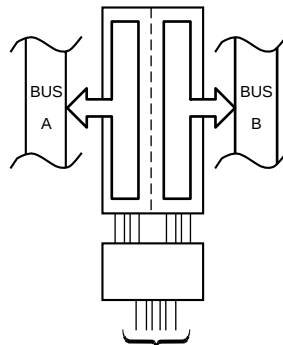
xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	X	X	L

**REAL-TIME TRANSFER
BUS A TO B**


xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L	X	X	L	X

**STORAGE FROM
A AND/OR B**


xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
H	L		X	X	X
L	L	X		X	X
X	H			X	X

**TRANSFER STORES
DATA TO A AND/OR B**


xDIR	x $\overline{\text{OE}}$	xCLKAB	xCLKBA	xSAB	xSBA
L	L	X	H or L	X	H
H	L	H or L	X	H	X

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	–65°C to +150°C
Ambient Temperature with Power Applied	–40°C to +85°C
Supply Voltage to Ground Potential (Inputs & V _{CC} Only)	–0.5V to +7.0V
Supply Voltage to Ground Potential (Outputs & D/O Only)	–0.5V to +7.0V
DC Input Voltage	–0.5V to +7.0V
DC Output Current	120mA
Power Dissipation	1.0W

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

DC Electrical Characteristics (Over the Operating Range, T_A = –40°C to +85°C, V_{CC} = 5.0V ± 10%)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
V _{IH}	Input HIGH Voltage	Guaranteed Logic HIGH Level		2.0			V
V _{IL}	Input LOW Voltage	Guaranteed Logic LOW Level				0.8	V
I _{IH}	Input HIGH Current	Standard Input, V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IH}	Input HIGH Current	Standard I/O, V _{CC} = Max.	V _{IN} = V _{CC}			1	μA
I _{IH}	Input HIGH Current	Bus Hold Input ⁽⁴⁾ , V _{CC} = Max.	V _{IN} = V _{CC}			±100	μA
I _{IH}	Input HIGH Current	Bus Hold I/O ⁽⁴⁾ , V _{CC} = Max.	V _{IN} = V _{CC}			±100	μA
I _{IL}	Input LOW Current	Standard Input, V _{CC} = Min.	V _{IN} = GND			–1	μA
I _{IL}	Input LOW Current	Standard I/O, V _{CC} = Min.	V _{IN} = GND			–1	μA
I _{IL}	Input LOW Current	Bus Hold Input ⁽⁴⁾ , V _{CC} = Min.	V _{IN} = GND			±100	μA
I _{IL}	Input LOW Current	Bus Hold I/O ⁽⁴⁾ , V _{CC} = Min.	V _{IN} = GND			±100	μA
I _{BHH}	Bus Hold	Bus Hold Input ⁽⁴⁾ , V _{CC} = Min.	V _{IN} = 2.0V	–50			μA
I _{BHL}	Sustain Current		V _{IN} = 0.8V	+50			
I _{OZH} ⁽⁵⁾	High-Impedance	V _{CC} = Max.	V _{OUT} = 2.7V			1	μA
I _{OZL} ⁽⁵⁾	Output Current (3-STATE OUTPUTS)	V _{CC} = Max.	V _{OUT} = 0.5V			–1	μA
V _{IK}	Clamp Diode Voltage	V _{CC} = Min., I _{IN} = –18mA			–0.7	–1.2	V
I _{OS}	Short Circuit Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = GND		–80	–140	–200	mA
I _O	Output Drive Current	V _{CC} = Max. ⁽³⁾ , V _{OUT} = 2.5V		–50		–180	mA
V _H	Input Hysteresis				100		mV

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at V_{CC} = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. Pins with Bus Hold are identified in the pin description.
5. This specification does not apply to bi-directional functionalities with Bus Hold.

PI74FCT16646T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -3.0mA	2.5	3.5		V
			IOH = -15.0mA	2.4	3.5		
			IOH = -32.0mA	2.0	3.0		
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL	IOL = 64mA		0.2	0.55	V
IOFF	Power Down Disable	VCC = 0V, VIN or VOUT ≤ 4.5V		—	—	±100	μA

PI74FCT162646T/162H646T Output Drive Characteristics (Over the Operating Range)

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
VOH	Output HIGH Voltage	VCC = Min., VIN = VIH or VIL	IOH = -24.0mA	2.4	3.3		V
VOL	Output LOW Voltage	VCC = Min., VIN = VIH or VIL	IOL = 24mA		0.3	0.55	V
IODL	Output LOW Current	VCC = 5V, VIN = VIH OR VIL, VOUT = 1.5V ⁽³⁾		60	115	150	mA
IODH	Output HIGH Current	VCC = 5V, VIN = VIH OR VIL, VOUT = 1.5V ⁽³⁾		-60	-115	-150	mA

Capacitance (TA = 25°C, f = 1 MHz)

Parameters ⁽⁴⁾	Description	Test Conditions	Typ.	Max.	Units
CIN	Input Capacitance	VIN = 0V	4.5	6	pF
COUT	Output Capacitance	VOUT = 0V	5.5	8	pF

Notes:

1. For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.
2. Typical values are at VCC = 5.0V, +25°C ambient and maximum loading.
3. Not more than one output should be shorted at one time. Duration of the test should not exceed one second.
4. This parameter is determined by device characterization but is not production tested.

Power Supply Characteristics

Parameters	Description	Test Conditions ⁽¹⁾		Min.	Typ. ⁽²⁾	Max.	Units
I _{CC}	Quiescent Power Supply Current	V _{CC} = Max.	V _{IN} = GND or V _{CC}		0.12	500	μA
ΔI _{CC}	Supply Current per Input @ TTL HIGH	V _{CC} = Max.	V _{IN} = 3.4V ⁽³⁾		0.5	1.5	mA
I _{CCD}	Supply Current per Input per MHz ⁽⁴⁾	V _{CC} = Max., Outputs Open xDIR = xOE = GND One Bit Toggling 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		75	120	μA/ MHz
I _C	Total Power Supply Current ⁽⁶⁾	V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (xCLKBA) 50% Duty Cycle xDIR = xOE = GND One Bit Toggling f _I = 5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		0.8	1.7 ⁽⁵⁾	mA
			V _{IN} = 3.4V V _{IN} = GND		1.3	3.2 ⁽⁵⁾	
		V _{CC} = Max., Outputs Open f _{CP} = 10 MHz (xCLKBA) 50% Duty Cycle xDIR = xOE = GND 16 Bits Toggling f _I = 2.5 MHz 50% Duty Cycle	V _{IN} = V _{CC} V _{IN} = GND		3.8	6.5 ⁽⁵⁾	
			V _{IN} = 3.4 V _{IN} = GND		8.3	20.0 ⁽⁵⁾	

Notes:

- For Max. or Min. conditions use appropriate value specified under Electrical Characteristics for the applicable device.
- Typical values are at V_{CC} = 5.0V, +25°C ambient.
- Per TTL driven input (V_{IN} = 3.4V); all other inputs at V_{CC} or GND.
- This parameter is not directly testable, but is derived for use in Total Power Supply Calculations.
- Values for these conditions are examples of the I_{CC} formula. These limits are guaranteed but not tested.
- I_C = I_{QUIESCENT} + I_{INPUTS} + I_{DYNAMIC}

$$I_C = I_{CC} + \Delta I_{CC} D_H N_T + I_{CCD} (f_{CP}/2 + f_I N_I)$$

I_{CC} = Quiescent Current
ΔI_{CC} = Power Supply Current for a TTL High Input (V_{IN} = 3.4V)
D_H = Duty Cycle for TTL Inputs High
N_T = Number of TTL Inputs at D_H
I_{CCD} = Dynamic Current Caused by an Input Transition Pair (HLH or LHL)
f_{CP} = Clock Frequency for Register Devices (Zero for Non-Register Devices)
f_I = Input Frequency
N_I = Number of Inputs at f_I
All currents are in milliamps and all frequencies are in megahertz.

PI74FCT16646T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	16646T		16646AT		16646CT		16646DT		16646ET		Units
			Com.		Com.		Com.		Com.		Com.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
tpZH tpZL	Output Enable Time xDIR or xOE to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ xDIR or xOE to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		6.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

PI74FCT162646T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	162646T		162646AT		162646CT		162646DT		162646ET		Units
			Com.		Com.		Com.		Com.		Com.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
tpZH tpZL	Output Enable Time xDIR or xOE to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ xDIR or xOE to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
tsu	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
th	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		6.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.

PI74FCT162H646T Switching Characteristics over Operating Range

Parameters	Description	Conditions ⁽¹⁾	162H646T		162H646AT		162H646CT		162H646DT		162H646ET		Units
			Com.		Com.		Com.		Com.		Com.		
			Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
tPLH tPHL	Propagation Delay Bus to Bus	CL = 50 pF RL = 500Ω	2.0	9.0	2.0	6.3	1.5	5.4	1.5	4.4	1.5	3.8	ns
tpZH tpZL	Output Enable Time xDIR or xOE to Bus		2.0	14.0	2.0	9.8	1.5	7.8	1.5	5.0	1.5	4.8	ns
tpHZ tPLZ	Output Disable Time ⁽³⁾ xDIR or xOE to Bus		2.0	9.0	2.0	6.3	1.5	6.3	1.5	4.3	1.5	4.0	ns
tPLH tPHL	Propagation Delay Clock to Bus		2.0	9.0	2.0	6.3	1.5	5.7	1.5	4.4	1.5	3.8	ns
tPLH tPHL	Propagation Delay xSBA or xSAB to Bus		2.0	11.0	2.0	7.7	1.5	6.2	1.5	5.0	1.5	4.2	ns
tsU	Setup Time HIGH or LOW, Bus to Clock		4.0	—	2.0	—	2.0	—	2.0	—	2.0	—	ns
tH	Hold Time HIGH or LOW, Bus to Clock		2.0	—	1.5	—	1.5	—	1.0	—	0.0	—	ns
tw	Clock Pulse Width HIGH or LOW ⁽³⁾		6.0	—	5.0	—	5.0	—	3.0	—	3.0	—	ns
tsk(o)	Output Skew ⁽⁴⁾		—	0.5	—	0.5	—	0.5	—	0.5	—	0.5	ns

Notes:

1. See test circuit and wave forms.
2. Minimum limits are guaranteed but not tested on Propagation Delays.
3. This parameter is guaranteed but not production tested.
4. Skew between any two outputs, of the same package, switching in the same direction. This parameter is guaranteed by design.